System control servo
BU38603 / BU38703 / BU38803

The BU38603, BU38703 and BU38803 are servo controller ICs for VCRs. They contain a high-speed, 8-bit CPU and perform the processing required for the drum, capstan, FV and PV completely in software, allowing a large reduction in the number of external components required. They also contain high-performance linear amplifiers, eliminating the need for interface ICs. Specialized hardware is included for items that require high-speed processing, to allow efficient utilization of the CPU.

●Applications
VHS VCRs and camcorders

●Features
1) CPU
499 commands (69 types)
Memory-mapped I / O
Minimum command execution time: 250ns (8MHz)
2)ROM capacity
BU38603: 16384 × 8 bit
BU38703: 24576 × 8 bit
BU38803: 32768 × 8 bit
3) RAM capacity: 512 × 8bit
4) Interrupt
Pattern generator: 1
Watch-dog timer: 1
External interrupts: 1
FG interrupts: 5
Internal interrupts: 7
Two timers, serial transmission, interrupt, VHSW, CTL interval timer (fixed) / VISS
∗ Multi-layer interrupts possible.
5) Free-running counter: 19 bit
6) PWM output: 12 bit × 2
7) Pattern generator
17 bits from FRC MSB used.
Output
Internal: 3 bit
External (PO): 5 bit
External (PIO): 6 bit
8) Programmable pre-scaler
CFG: 7 bit
CTL: 6 bit
9) Head amplifier / chroma rotary
Generated from pattern generator output.
10) Built-in AGC. Five-bits used to switch the gain control registers for the CTL amplifier.
11) CTL counter: 1 / 30 or 1 / 25
12) Data shift PLL calculation: 24 bit
13) Timer: 8 bit × 2
14) Synchronous serial input/output: 8 bit × 1
15) VH PULSE
V separeted from composite synchronous snal.
Pseudo V generated from pattern generator output.
Superimposed pseudo H synchronized with the composite synchronous signal.
16) VISS / VASS
VASS 0 / 1 discrimination
VISS discrimination threshold: 3
Aspect discrimination.
D / A CTL switching.
17) Standard I / O
Parallel I / O (PIO): 32 bit
Parallel output (PO): 6 bit
18) A / D converter: 8 bits × 8 channels
Can be masked-programmed to be parallel inputs.
19) Watch-dog timer
Setting period: 4
20) Linear circuits
DFG: amplifier / comparator
CFG: amplifier / comparator
CTL: differential amplifier / comparator
DPG: comparator

●Absolute maximum ratings (Ta = 25°C)

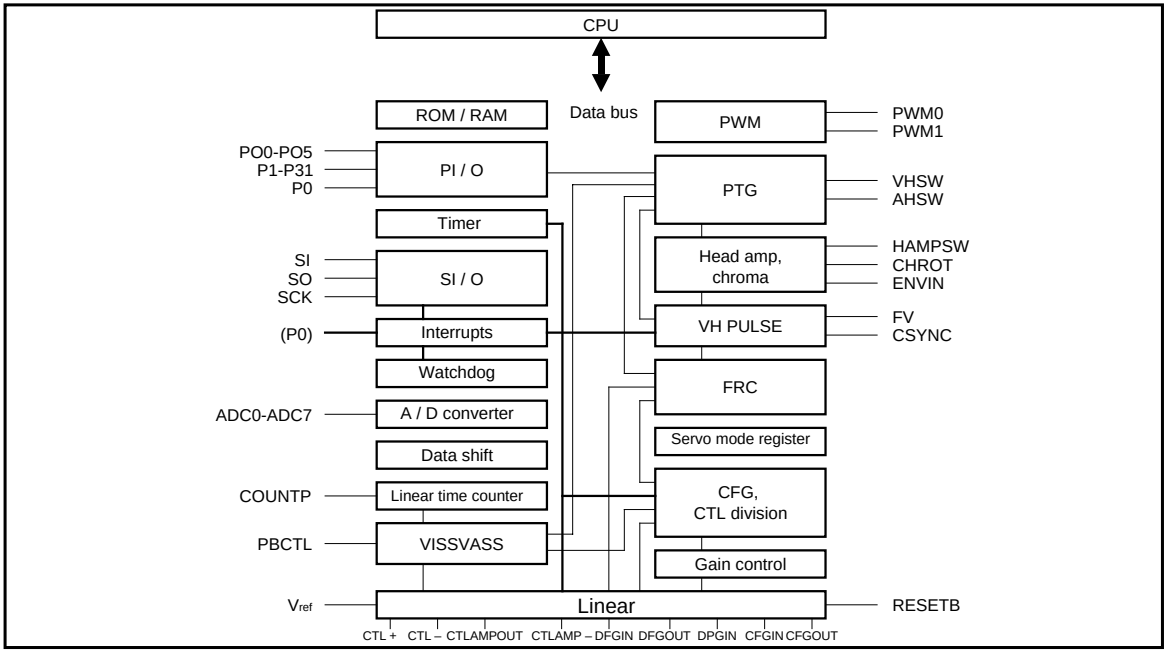
Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}, V_{DDA}, V_{DAD}	0.3 ~ 7.0*2	V
Pin applied voltage	V_{IN}	V_{SS} – 0.3 ~ V_{DD} + 0.3	V
Power dissipation	Pd	500*1	mW
Storage temperature	Tstg	– 55 ~ + 125	°C

*1 Reduced by 5mW for each increase in Ta of 1°C over 25°C.
*2 Use with V_{SS} = V_{SSA} = V_{SAD}, and V_{DD} = V_{DDA} = V_{DAD}.

●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}, V_{DDA}, V_{DDB}	4.5 ~ 5.5	V
Clock frequency	F_{CK}	8	MHz
Operating temperature	Topr	– 25 ~ + 75	°C

●Block diagram



●Pin descriptions

Pin No.	Pin name	Function
1	VSAD	A / D convertor circuit GND.
2	ADC0	Can be optionally mask – programmed to be either A / D or parallel inputs.
3	ADC1	
4	ADC2	
5	ADC3	
6	ADC4	
7	ADC5	
8	ADC6	
9	ADC7	
10	VDAD	A / D convertor circuit power supply.
11	DFGOUT	Drum FG amplifier output
12	DFGIN	Drum FG amplifier input
13	DPGIN	Drum PG comparator input
14	CFGIN	Capstan FG amplifier input
15	CFGOUT	Capstan FG amplifier output
16	VSSA	Linear circuit GND
17	V_{ref}	Internal BIAS and power-on reset pin
18	CTLAMP –	CTL amplifier – input
19	CTLAMPOUT	CTL amplifier output
20	CTL –	CTL coil – connection
21	CTL +	CTL coil + connection
22	VDDA	Linear circuit power supply
23	RESETB	Power supply reset
24	TEST	Test mode input (normally GND)
25	PO5	Parallel output
26	PO4	
27	P31	Parallel I / O
28	P30	
29	P29	
30	P28	
31	P27	Parallel I / O and pattern generator output
32	P26	
33	P25	
34	P24	
35	P23	
36	P22	
37	PO3	Parallel output and pattern generator output
38	VHSW	Pattern generator VHSW output
39	AHSW	Pattern generator AHSW output
40	HAMPSW	Head amplifier switch output

Pin No.	Pin name	Function
41	CHROT	Chroma rotary switch output
42	FV	Pseudo Vsync output
43	V_{DD}	Logic circuit power supply
44	PWM0	PWM output
45	PWM1	
46	P21	Parallel I / O
47	P20	
48	P19	
49	P18	
50	P17	
51	P16	
52	P15	
53	P14	
54	P13	
55	P12	
56	P11	
57	P10	
58	P9	
59	PO2	Parallel output
60	PO1	
61	PO0	
62	CLOCKO	For connection of oscillator
63	CLOCKI	
64	V_{SS}	Logic circuit GND
65	P8	Parallel I / O
66	P7	
67	P6	
68	P5	
69	P4	
70	P3	
71	P2	
72	P1	
73	P0	Parallel I / O and external interrupt
74	SI	Serial I / O data input
75	SO	Serial I / O data I / O
76	SCK	Serial I / O clock I / O
77	ENVIN	Envelope detector logic input
78	CSYNC	Composite signal logic input
79	COUNTP	CTL counter pulse output
80	PBCTL	CTL logic output

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5V and f_{OSC} = 8MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement circuit
[Logic block] (Logic: pins 24 to 80)							
Operating supply current	I_{DD}	—	12	19	mA	No load, when reset	Fig.1
⟨Logic I / O⟩							
Output high level voltage	V_H	4.0	4.5	—	V	I = 2mA: except pins 66 to 73 I = 1mA: 66 to 73pin	Fig.2
Output low level voltage	V_L	—	0.5	1.0	V	I = 2mA	Fig.2
Max. output low level current	I_{LL}	10.0	16.0	—	mA	66 to 73pin	Fig.2
Input high level voltage	V_{IH}	4.0	—	—	V		Fig.2
Input low level voltage	V_{IL}	—	—	1.0	V		Fig.2
Input high level current	I_H	—	0	1.0	µA	$V_{IN} = V_{DD}$	Fig.2
Input low level current	I_L	– 1.0	0	—	µA	V_{IN} = 0	Fig.2
⟨Serial I / O⟩							
Input data hold	T_{SH}	0.16	—	—	µs		—
Input data setup	T_{SS}	0.16	—	—	µs		—
Output data delay	T_D	—	—	0.3	µs	Between CLOCK and DATA	—
[Linear block] (Linear: pins 11 to 23)							
Operating supply current	I_{LI}	—	10	26	mA	No load	Fig.1
[A / D block] (A / D: pins 1 to 10)							
Operating supply current	I_{AD}	—	0.6	2.0	mA		Fig.1
Linearity error	E_L	– 3	0	3	LSB		Fig.3
Input high level voltage	V_{ADPH}	4.0	—	—	V	When P input selected	Fig.3
Input low level voltage	V_{ADPL}	—	—	1.0	V	When P input selected	Fig.3
Input high level current	I_{ADPH}	—	0	1.0	µA	When P input selected, $V_{IN} = V_{DD}$	Fig.3
Input low level current	I_{ADPL}	– 1.0	0	—	µA	When P input selected, V_{IN} = 0	Fig.3

●Measurement circuits

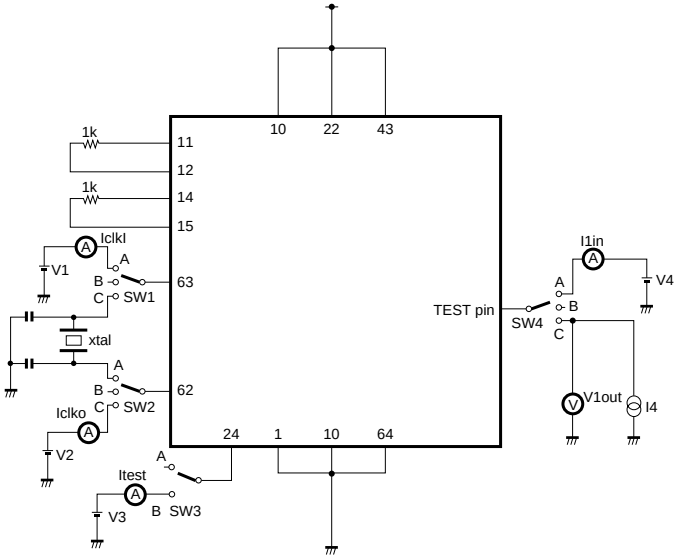


Fig.1

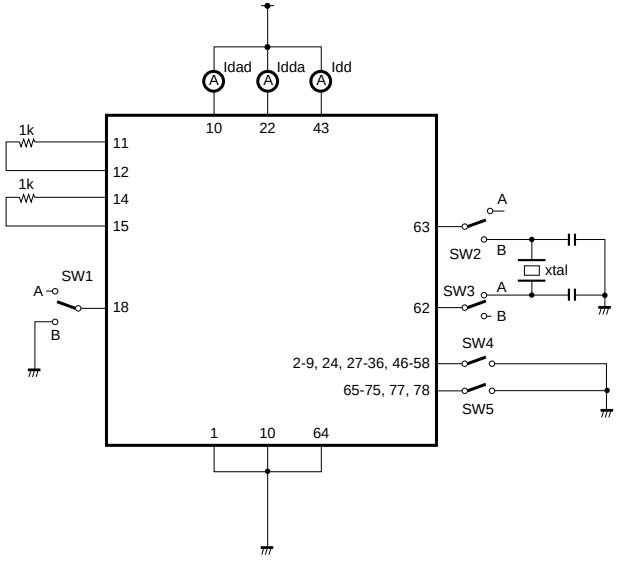


Fig.2

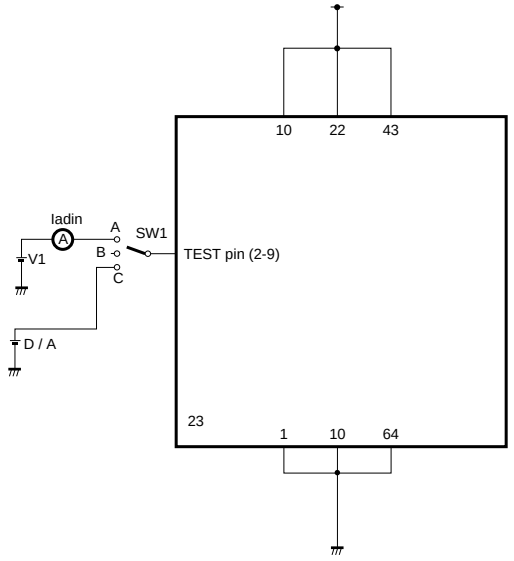


Fig.3

●Application example

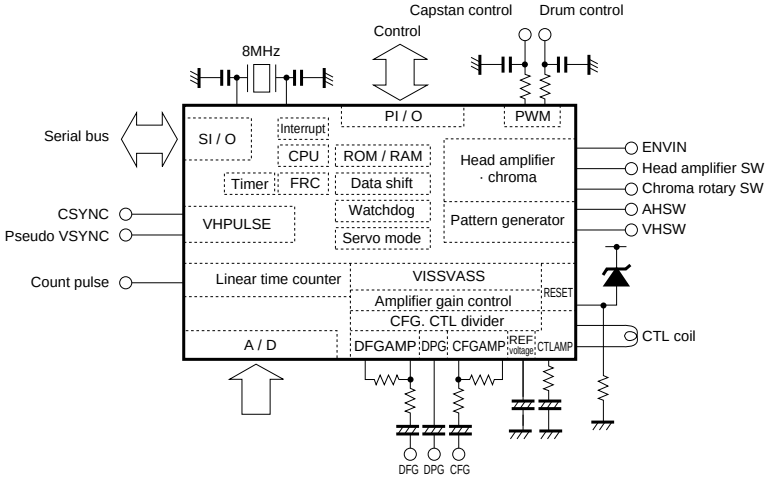


Fig.4

●Electrical characteristic curves

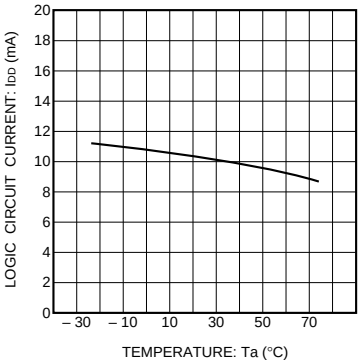


Fig. 5 Logic circuit current.

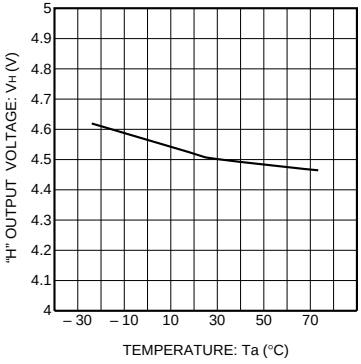


Fig. 6 Logic "H" output voltage.

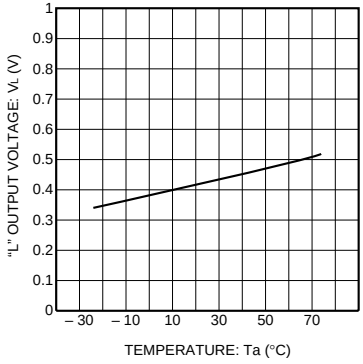


Fig. 7 Logic "L" output voltage.

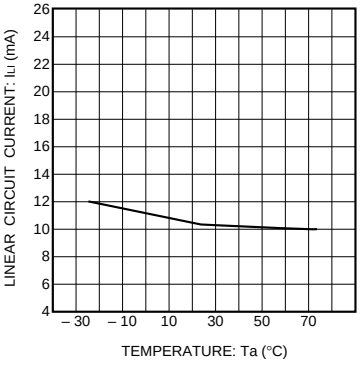


Fig. 8 Linear circuit current.

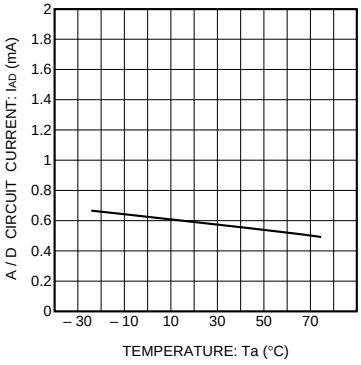
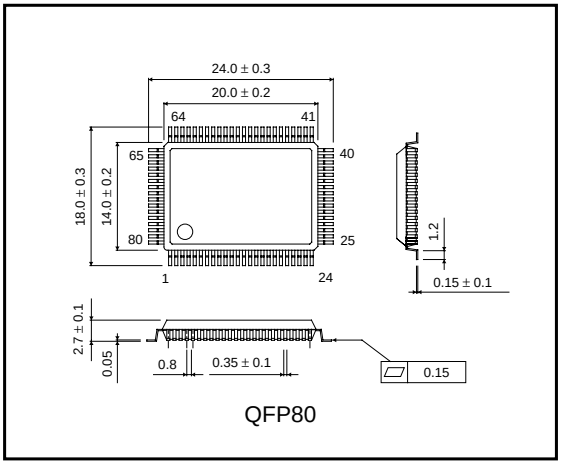


Fig. 9 A / D circuit current.

●External dimensions (Units: mm)



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