TW6816 – 4-CH Audio/Video Decoders with 66MHz PCI interface

Preliminary Data Sheet

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TW6816– 4-CH Audio/Video Decoders with 66MHz PCI Interface

Features

Video decoder

- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM support with automatic format detection
- Software selectable analog inputs allows any of 4 CVBS per one video ADC.
- Four 10-bit ADCs and analog clamping circuit for CVBS input.
- Fully programmable static gain or automatic gain control for the Y channel
- Programmable white peak control for CVBS channel
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Image enhancement with 2D peaking and CTI.
- Digital sub-carrier PLL for accurate color decoding
- Digital Horizontal PLL for synchronization processing and pixel sampling
- Advanced synchronization processing and sync detection for handling non-standard and weak signal
- Programmable hue, brightness, saturation, contrast, sharpness, Gamma control, and noise suppression
- Automatic color control and color killer
- Detection of level of copy protection according to Macrovision standard
- Programmable output cropping

Video scaler

- High quality horizontal filtered scaling with arbitrary scale down ratio
- Phase accuracy better than 1/32 pixel
- Selectable anti-alias filter

Audio Capture

- Four 10-bit ADC for Analog Sound digitizing.
- Programmable Sampling rate.

PCI

- 66MHz/33MHz PCI with M66EN interface
- PCI Rev. 2.2-3.0 compliant
- ACPI support
- Integrated Video/Audio DMA controller
- Support both selectable one real-time video and 4x switching non real-time video

Miscellaneous

- Programmable RGB and YCbCr color space conversion
- 400Kbps Two-wire MPU serial bus Master interface.
- Power-down mode
- Single 27MHz crystal for all standards
- 5V tolerant I/O
- 1.8 V power supply
- 100-pin LQFP package

Function Description

Figure 1: TW6816 Block Diagram

Video Decoder

Video Decoder Overview

The TW6816 is a multi-standard video decoder that is designed for multimedia applications. It uses the mixed-signal 1.8V CMOS technology to provide a low-power integrated solution.

The video decoder decodes the analog CVBS signals into digital YCbCr for output. It consists of analog front-end with input source selection, variable gain amplifier and analog-to-digital converters, Y/C separation circuit, multi-standard color decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC 4.43 and SECAM) and synchronization circuitry. The Y/C separation is done with highly adaptive 4H comb filter for reduced cross color and cross luminance. The advanced synchronization processing circuitry can produce stable pictures for non-standard signal as well as weak signal. A video scaler is provided to arbitrarily scale down the output video. The output of the decoder is formatted to the ITU-R 656 compatible output. It includes various control circuits like brightness, contrast, saturation, and dynamic aperture correction for best video quality.

Analog Front-end

The analog front-end converts analog video signals to the required digital format. There are four analog video channels with clamping circuits and ADCs. The Y channel has 4-input multiplexer, and a variable gain amplifier for automatic gain control (AGC). Its four inputs are identified as VINnA,VINnB,VINnC,VINnD(n=1,2,3,4).

Video Source Selection

All analog signals should be AC-coupled to these inputs.

The Y channel analog multiplexer selects one of the four inputs VINnA,VINnB,VINnC,VINnD(n=1,2,3,4).

Clamping and Automatic Gain Control

All two analog channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a level of 60 or a programmable level. The C channel restores the back porch of the digitized video to a level of 128. This operation is automatic through internal feedback loop.

The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. A programmable white peak protection logic is included to prevent saturation in the case of abnormal proportion between sync and white peak level.

Analog to Digital Converter

TW6816 contains two 10-bit pipelined ADCs that consume less power than conventional flash ADC. The output of the Clamp and AGC connects to one ADC that digitizes the composite input or the Y signal input.

Sync Processing

The sync processor of TW6816 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

Horizontal sync processing

The horizontal synchronization processing contains a sync separator, a phase-locked-loop (PLL), and the related decision logic.

The horizontal sync detector detects the presence of a horizontal sync tip by examining low-pass filtered input samples whose level is lower than a threshold. The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. From there, the PLL also provides orthogonal sampling raster for the down stream processor. The PLL has free running frequency that matches the standard raster frequency. It also has wide lock-in range for tracking any non-standard video signal.

Vertical sync processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. When the location of the detected vertical sync is inline with a horizontal sync, it indicates a frame start or the odd field start. Otherwise, it indicates an even field. The field logic can also be controlled to toggle automatically while tracking the input.

Color Decoding

Y/C separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, only notch/band-pass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter are shown in the filter curve section.

In the case of comb filter, the TW6816 separates luma (Y) and chroma(C) of a composite video signal using a proprietary 4H, 5-line adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to good Y/C separation with small cross luma and cross color at both horizontal and vertical edges.

Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

Color demodulation

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chroma signal to the base band. The mixing frequency is equal to the sub-carrier frequency for NTSC and PAL. After the mixing, a low-pass filter is used to remove carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the mixing frequency is 4.286Mhz. After the mixer and low-pass filter, it yields the FM modulated chroma. The SECAM demodulation process therefore consists of low-pass filter, FM demodulator and de-emphasis filter. The filter characteristics are shown in filter curve section. During the FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. This color-burst amplitude is calculated and compared to standard amplitude. The chroma (Cx) signals are then increased or decreased in amplitude accordingly. The range of ACC controls are –6db to +26db.

Low Color Detection and Removal

For low color amplitude signals, black and white video, or very noisy signals, the color will be "killed". The color killer uses the burst amplitude measurement to switch-off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmed hysteresis to prevent oscillation of the color killer function. Programming a low threshold value can disable the color killer function.

Automatic standard detection

The TW6816 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

Video Format support

TW6816 supports all common video formats as shown in Table 1. The video decoder needs to be programmed appropriately for each of the composite video input formats.

Table 1. Video Input Formats Supported by TW6816

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding

Notes: (1). NTSC-Japan has 0 IRE setup.

Component Processing

Luminance Processing

The TW6816 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW6816 video decoder also performs a coring function. It can force all values below a certain level, programmed in the Coring Control Register, to zero. This is useful because human eyes are sensitive to variations in nearly black images. Changing levels near black to true black, can make the image appears clearer.

Sharpness

The TW6816 also provides a sharpness control function through control registers. It provides the control in 16 steps up to +12db. The center frequency of the enhancement curve is around 3.5Mhz. It also provides a high frequency coring function to minimize the amplification of high frequency noise. The coring level is adjustable through the Coring Control register. The same function can also be used to soften the images. This can be used to provide noise reduction on noisy signal.

To further enhance the image, a programmable vertical peaking function is provided for up to +6db of enhancement. A programmable coring level can be adjusted to minimize the noise enhancement.

The Hue and Saturation

When decoding NTSC signals, TW6816 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

Color Transient Improvement

A programmable Color Transient Improvement circuit is provided to enhance the color bandwidth. Low-level noise enhancement can be suppressed by a programmable coring logic. Overshoot and undershoot are also removed by special circuit to prevent false color generation at the color edge.

Power Management

The TW6816 can be put into power-down mode in which its clock is turned off for most of the circuits. The Y and C path can be separately powered down.

Down-scaling and Cropping

The TW6816 provides two methods to reduce the amount of output video pixel data, downscaling and cropping. The downscaling provides full video image at lower resolution. Cropping provides only a portion of the video image output. All these mechanisms can be controlled independently to yield maximum flexibility in the output stream.

Down-Scaling

The TW6816 can independently reduce the output video image size in both horizontal and vertical directions using arbitrary scaling ratios up to 1/16 in each direction. The horizontal scaling employs a dynamic 6-tap 32-phase interpolation filter for luma and a 2-tap 8-phase interpolation filter for chroma because of the limited bandwidth of the chroma data. The vertical scaling uses the simple line dropping method. It is recommended to choose integer vertical scaling ratio for best result.

Downscaling is achieved by programming the horizontal scaling ratio register (HSCALE) and vertical scaling ratio register (VSCALE). When outputting unscaled video, the TW6816 will output CCIR601 compatible 720 pixels per line or any number of pixels per line as specified by the HACTIVE register. The standard output for Square Pixel mode is 640 pixels for 60 Hz system and 768 pixels for 50 Hz systems. If the number of output pixels required is smaller than 720 in CCIR601 compatible mode or the number specified by the HACTIVE register. The 12-bit HSCALE register, which is the concatenation of two 8-bit registers SCALE_HI and HSCALE_LO, is used to reduce the output pixels to the desired number.

Following is an example using pixel ratio to determine the horizontal scaling ratio. These equations should be used to determine the scaling ratio to be written into the 12-bit HSCALE register assuming HACTIVE is programmed with 720 active pixels per line:

NTSC: HSCALE = [720/$N_{pixel\_desired}$] * 256
PAL: HSCALE = [(720/$N_{pixel\_desired}$)] * 256
Where: $N_{pixel\_desired}$ is the nominal number of pixel per line.

For example, to output a CCIR601 compatible NTSC stream at SIF resolution, the HSCALE value can be found as:

HSCALE = [(720/320)] * 256 = 576 = 0x0240

However, to output a SQ compatible NTSC stream at SIF resolution, the HSCALE value should be found as:

HSCALE = [(640/320)] * 256 = 512 = 0x200

In this case, with total resolution of 768 per line, the HACTIVE should have a value of 640.

The vertical scaling determines the number of vertical lines output by the TW6816. The vertical scaling register (VSCALE) is a 12-bit register, which is the concatenation of a 4-bit register SCALE_HI and an 8-bit register VSCALE_LO. The maximum scaling ratio is 16:1. Following equations should be used to determine the scaling ratio to be written into the 12-bit VSCALE register assuming VACTIVE is programmed with 240 or 288 active lines per field.

60Hz system: VSCALE = [240/ $N_{line\_desired}$] * 256
50Hz system: VSCALE = [288/ $N_{line\_desired}$] * 256
Where: $N_{line\_desired\ is}$ the number of active lines output per field.

The scaling ratios for some popular formats are listed in Table 2.

TW6816 Cropping

Cropping allows only subsection of a video image to be output. The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are 8-bit wide, the lower 8-bits is, respectively, in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper 2-bit shares the same register CROP_HI.

The Horizontal delay register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the unscaled pixel number. The Horizontal active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the unscaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remain unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line.

For NTSC output at 13.5 MHz pixel rate, the total number of pixels is 858. The HDELAY should be set to 106 and HACTIVE set to 720. For PAL output at 13.5 MHz rate, the total number of pixels is 864. The HDELAY should be set to 108 and HACTIVE set to 720.

The Vertical delay register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. In order for the vertical cropping to work properly, the following equation should be observed.

VDELAY + VACTIVE < Total number of lines per field

Table 2 shows some popular video formats and its recommended register settings. The CCIR601 format refers to the sampling rate of 13.5 MHz. The SQ format for 60 Hz systems refers to the sampling rate of 12.27 MHz, and the SQ format for 50 Hz systems refers to the use of sampling rate of 14.75 MHz.

Scaling Ratio	Format	Total Resolution	Output Resolution	HSCALE values	VSCALE (frame)
1:1	NTSC SQ	780x525	640x480	0x0100	0x0100
	NTSC CCIR601	858x525	720x480	0x0100	0x0100
	PAL SQ	944x625	768x576	0x0100	0x0100
	PAL CCIR601	864x625	720x576	0x0100	0x0100
2:1 (CIF)	NTSC SQ	390x262	320x240	0x0200	0x0200
	NTSC CCIR601	429x262	360x240	0x0200	0x0200
	PAL SQ	472x312	384x288	0x0200	0x0200
	PAL CCIR601	432x312	360x288	0x0200	0x0200
4:1 (QCIF)	NTSC SQ	195x131	160x120	0x0400	0x0400
	NTSC CCIR601	214x131	180x120	0x0400	0x0400
	PAL SQ	236x156	192x144	0x0400	0x0400
	PAL CCIR601	216x156	180x144	0x0400	0x0400

Table 2. HSCALE and VSCALE value for some popular video formats.

Video Data Format Conversion

The decoded video from the video decoder within TW6816 is in the format of YCbCr 4:4:4.GPIO ITU-R BT656 video input data is in the format of YCbCr 4:2:2. Video data format conversion is needed to convert these video data to the selected output video format. The video data can be converted to variety of RGB video formats, and changes can be made in the byte order. TW6816 also provides gamma correction for video data in RGB format. The video stream from video decoder of TW6816 will be packed into DWORD in the selected format prior to input to the video FIFO.

GAMMA Correction

Gamma correction removal with factor 2.2 is available if one of RGB video data formats is selected. Gamma correction removal is enabled when register GAMMA is set to 1.

Byte Swapping

After color conversion, the data byte order in each DWORD can be swapped by programming the register BSWAP. Table 3 summarizes the output byte order for different BSWAP setting.

Table 3. Byte Swapping

BSWAP	**Output DWORD**			
	Byte 3	Byte 2	Byte 1	Byte 0
00	D[31:24]	D[23:16]	D[15:8]	D[7:0]
01	D[23:16]	D[31:24]	D[7:0]	D[15:8]
10	D[15:8]	D[7:0]	D[31:24]	D[23:16]
11	D[7:0]	D[15:8]	D[23:16]	D[31:24]

Color Formats

Table 4 shows the available Pixel Formats with COLORF,BSWAP and UVSWAP register settings.

Table 4. Video Data Format

Pixel Format	COLORF	BSWAP	UVSWAP	Description
RGB32	0	0	0	RGB format with alpha channel. Every pixel forms a DWORD in following byte order: Alpha, R, G, and B, where B is the least significant byte and Alpha is the most significant byte. Alpha value is always set to 0.{Alpha,R,G,B}
RGB24	1	0	0	RGB format. Four pixels are packed into three DWORDs as following: DWORD 0: B1 R0 G0 B0 DWORD 1: G2 B2 R1 G1 DWORD 2: R3 G3 B3 R2
RGB16 Dither RGB16	2 A	0	0	RGB format that packed into 16 bits per pixel. Each DWORD contains two pixels in the following format: { R1[7:3], G1[7:2], B1[7:3], R0[7:3], G0[7:2], B0[7:3] }
RGB15 Dither RGB15	3 B	0	0	RGB format that packed into 15 bits per pixel. Each DWORD contains two pixels in the following format: { 0, R1[7:3], G1[7:3], B1[7:3], 0, R0[7:3], G0[7:3], B0[7:3] }
YUY2	4	0	0	YCbCr 4:2:2 video format called as YUY2. Byte ordering (lowest first) is Y0, Cb0, Y1, Cr0, Y2, Cb2, Y3, Cr2, Y4, Cb4, Y5, Cr4. DWORD 0: Cr0 Y1 Cb0 Y0 DWORD 1: Cr2 Y3 Cb2 Y2 DWORD 2: Cr4 Y5 Cb4 Y4 . .
BtYUV(Y41P)	5	0	0	YCbCr 4:1:1 video format called as BtYUV or Y41P. DWORD 0 : Y1 Cr0 Y0 Cb0 DWORD 1 : Y3 Cr4 Y2 Cb4 DWORD 2 : Y7 Y6 Y5 Y4
Y411	6	0	0	YCbCr 4:1:1 video format called as Y411. DWORD 0 : Cr2 Y1 Y0 Cb2 DWORD 1: Y4 Cb6 Y3 Y2 DWORD 2: Y7 Y6 Cr6 Y5
UYVY	4	1	0	YCbCr 4:2:2 video format called as UYVY. DWORD 0: Y1 Cr0 Y0 Cb0 DWORD 1: Y3 Cr2 Y2 Cb2 DWORD 2: Y5 Cr4 Y4 Cb4 . .
YVYU	4	0	1	YCbCr 4:2:2 video format called as YVYU.Byte ordering (lowest first) is Y0, Cr0, Y1, Cb0, Y2, Cr2, Y3, Cb2, Y4, Cr4, Y5, Cb4. DWORD 0: Cb0 Y1 Cr0 Y0 DWORD 1: Cb2 Y3 Cr2 Y2 DWORD 2: Cb4 Y5 Cr4 Y4 .

Serial BUS Interface

If SBMODE is 1,Following Serial Bus transactions are supported. SBTRIG register initiates this Serial Bus transaction. S is START and SBDEV is SBDEV register. A is ACK, N is NAK, P is STOP.WB1-4, RB1-4 are registers. These Serial Bus transaction start after Value "1" is written into SBMODE register bit. After Serial Bus transaction is successfully completed, SBDONE register bit is set to 1.If Serial Bus transaction had any error including receiving NAK, SBERR register bit is set to 1 with SBDONE=1.RB1-4 registers are valid after receive transaction is completed and SBDONE is set to "1".

Send (Write) transaction: SBRW=0.

WDLEN=1
S – {SBDEV,0b} - A – WB1 – A - P
WDLEN=2
S – {SBDEV,0b} – A – WB1 – A – WB2 – A – P
WDLEN=3
S – {SBDEV,0b} – A – WB1 – A – WB2 – A – WB3 – A – P
WDLEN=4
S – {SBDEV,0b} – A – WB1 – A – WB2 – A – WB3 – A – WB4 – A – P

Receive (Read) transaction1: WREN=1,SBRW=1.

RDLEN=1
S – {SBDEV,0b} – A - WB1 – A – P – S – {SBDEV,1b} – A – RB1 – N – P
RDLEN=2
S – {SBDEV,0b} – A - WB1 – A – P – S – {SBDEV,1b} – A – RB1 – A
- RB2 – N – P
RDLEN=3
S – {SBDEV,0b} – A - WB1 – A – P – S – {SBDEV,1b} – A – RB1 – A
- RB2 – A – RB3 – N - P
RDLEN=4
S – {SBDEV,0b} – A - WB1 – A – P – S – {SBDEV,1b} – A – RB1 – A
- RB2 – A – RB3 – A – RB4 – N - P

Receive (Read) transaction2: WREN=0,SBRW=1.

RDLEN=1
S – {SBDEV,1b} – A - RB1 – N – P
RDLEN=2
S – {SBDEV,1b} – A - RB1 – A - RB2 – N – P
RDLEN=3
S – {SBDEV,1b} – A - RB1 – A - RB2 – A – RB3 – N - P
RDLEN=4
S – {SBDEV,1b} – A - RB1 – A - RB2 – A – RB3 – A – RB4 – N - P

Audio Processing

Audio Clock

Audio Clock is selected by ACLKSEL register.When internal apclk is selected as audio system clock,PACLKREF6816 register make audio system clock. When internal avclk is selected as audio system clock,VACLKREF6816 register make audio system clock.When ackg block amclk or ackg block asclk is selected, audio system clock(amclk or asclk) are controlled by following table.When ACPL register is set to 1,ACKN registers don't need to be set up.ACKI registers always need to be set up in this ackg block clock.

ACKN = round (F amclk / F field), it gives the Audio master Clock Per Field.

ACKI = round (F amclk / F XTI 27MHz * 2^23).

amclk (MHz)	FIELD[Hz]	ACKN dec	ACKN hex	ACKI dec	ACKI hex
256 x 48 KHz					
12.288	50	245760	3-C0-00	3817749	3A-41-15
12.288	59.94	205005	3-20-CD	3817749	3A-41-15
256 x 44.1KHz					
11.2896	50	225792	3-72-00	3507556	35-85-65
11.2896	59.94	188348	2-DF-BC	3507556	35-85-65
256 x 32 KHz					
8.192	50	163840	2-80-00	2545166	26-D6-0E
8.192	59.94	136670	2-15-DE	2545166	26-D6-0E
256 x 16 KHz					
4.096	50	81920	1-40-00	1272583	13-6B-07
4.096	59.94	68335	1-0A-EF	1272583	13-6B-07
256 x 8 KHz					
2.048	50	40960	A0-00	636291	9-B5-83
2.048	59.94	34168	85-78	636291	9-B5-83

asclk clock is made with SDIV registers by following equation.For example,if SDIV=0, asclk clock is amclk/2.asclk is half frequency clock of amclk.

Freq(asclk) = Freq(amclk) / (SDIV+1) /2

ACPL Audio PLL control
0 – PLL loop closed(optional video field locked clock mode only)
1 – PLL loop open

Analog Audio Input

All analog Audio signals should be AC-coupled to these inputs. Audio ADC digitized analog Audio Input signal and generated ADC data. Internal audio processing generates either 8bit mono sound data or 16bit mono sound data from this analog audio input process.

PCI interface

Interfacing to Serial EEPROM

PCI Configuration Header Location 0x20 contains the subsystem vendor ID and the subsystem ID. Two-wire serial interface can be used to connect an external serial EEPROM, such as 24C02 or 24C02A. When the EEPROM is connected, TW6816 uploads subsystem Vendor ID from the EEPROM after a PCI reset.

After a PCI reset, TW6816 starts a 4-byte sequential read, starting at address 0xFE. If at any time the slave EEPROM issues a NACK, the sequence is aborted and the Subsystem Vendor ID is set to 0x1797. Table 5 shows the content of EEPROM.

Table 5 Register Table in EEPROM

EEPROM device address : 0x50 (7 bits)	
Index	**Value**
0xFE	Subsystem Vendor ID [15:8]
0xFF	Subsystem Vendor ID [7:0]

DMA Controller Instructions

Video Part:

	Bit	Description	SYNCO	SYNCE	JUMP	Line Start	InLine	Dummy
DW0	31-28	Header	1100	1101	1011	1001	1010	1110
	27	IRQ						
	26-24	Data Type	All 0s	All 0s	All 0s	All 0s or 1s	All 0s	All 0s
	23-12	Starting Byte	All 0s	All 0s	All 0s			All 0s
	11-0	Byte Count	All 0s	All 0s	All 0s			All 0s
DW1	31-0	Starting Address	All 0s	All 0s				All 0s

Audio Part:

	Bit	Description	JUMP	Astart	Dummy	SYNCO	SYNCE
DW0	31-28	Header	1011	1001	1110	1100	1101
	27	IRQ					
	26-24	Data Type	All 0s	All 0s	All 0s	All 0s	All 0s
	23-12	Starting Byte	All 0s		All 0s	All 0s	All 0s
	11-0	Byte Count	All 0s		All 0s	All 0s	All 0s
DW1	31-0	Starting Address			All 0s	All 0s	All 0s

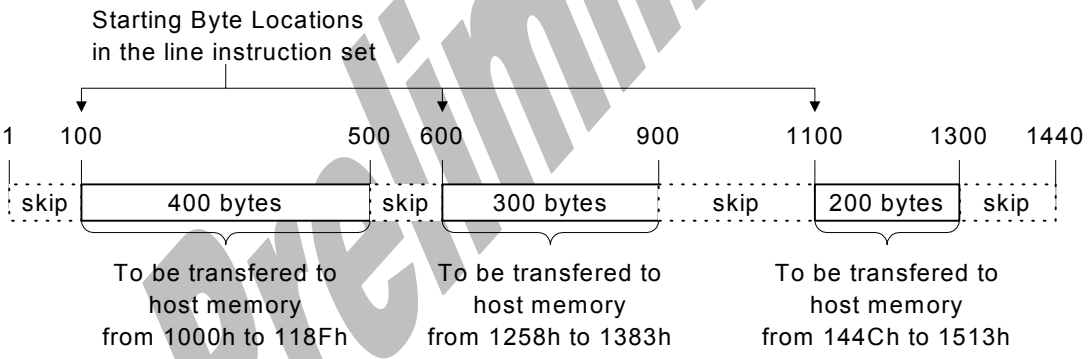
In both LineStart and Inline, Starting Byte is a byte location of the video data byte of a scan line from which the DMA operation should start. Byte Count is the number of video data byte should be transferred to the host memory. Starting Address is the host memory address to which the video data should be transferred. The difference between LineStart and InLine is that LineStart also instructs the DMA controller to operate on video data of next video line in the video FIFO. If the image is not cropped or the target memory space is big enough for video data of a scan line, LineStart alone completes a line instruction set. Otherwise, InLine is needed to transfer video data of the same scan line as the previous LineStart.The IRQ field of each instruction is used to instruct the DMA controller to generate an interrupt on PCI bus at the time when the operation of that instruction is completed. If IRQ is set to 1, an interrupt is generated and the DMAPI bit of Interrupt Status register is set to 1 after the completion of the instruction. No interrupt is generated if IRQ is set to 0.

An example of line instruction set

	Instruction	IRQ	Starting Byte	Byte Count	Starting Address
1	LineStart	0	100	400	1000h
2	InLine	0	600	300	1258h
3	InLine	1	1100	200	144Ch
1	LineStart	0	0	1440	2000h

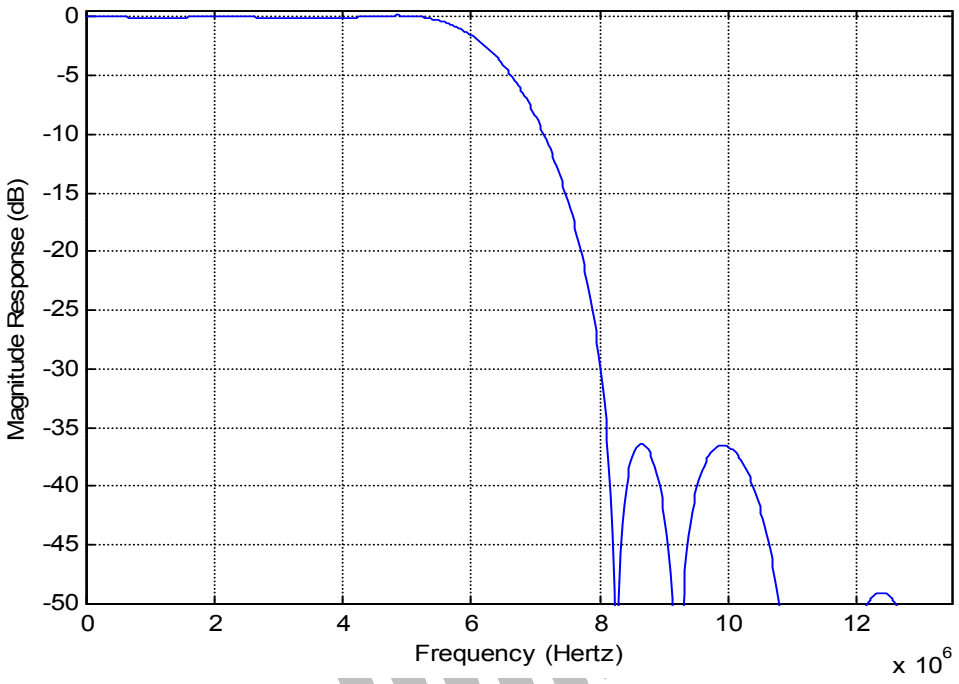
Above is an example of a line instruction set. Assuming that there are 1440 bytes of video data in a scan line. The first instruction in this line instruction set directs DMA controller to discard the first 100 bytes of data and transfer the following 400 bytes of data to host memory space starting from 1000h. After that, in the second instruction, another 100-byte data is discarded because DMA operation starts from 600-th byte of the scan line and lasts for 300 bytes to host memory from 1258h to 1383h. For the third instruction, DMA controller transfers 200 bytes of data to memory space from 144Ch to 1513h. Also, because IRQ is set to 1, an interrupt is generated after the completion of the third instruction. The last instruction shown in gray is a LineStart which is the first instruction of the next line instruction set and implies the end of this line instruction set, so the remaining 140 bytes of video data of this scan line are discarded. Figure 2 shows the result of the scan line to be transferred by the example line instruction set.

Figure 2. The result of the line instruction set shown above

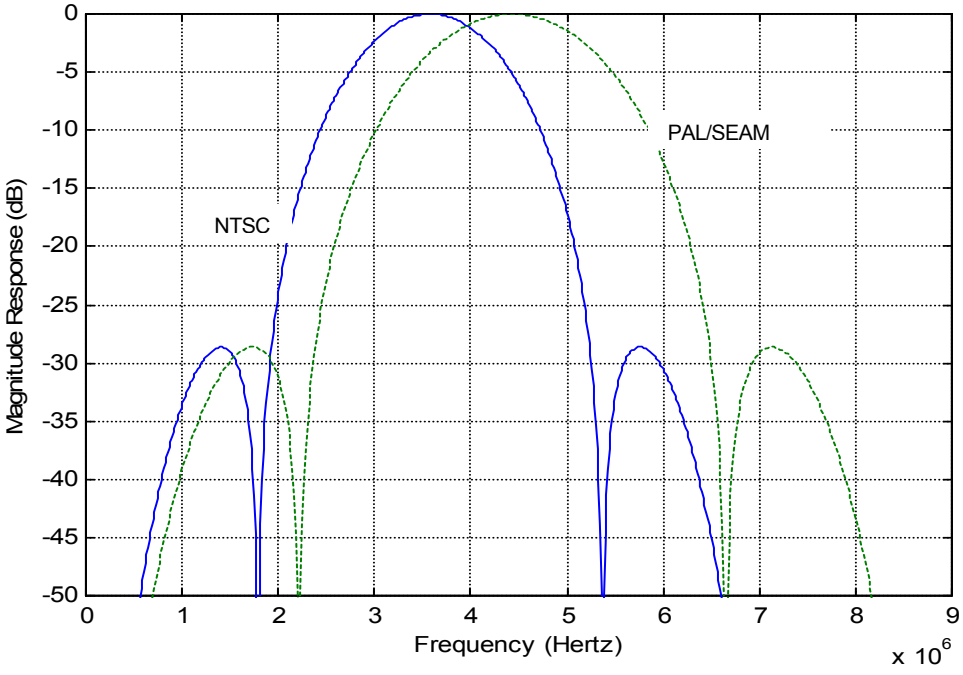


Filter Curves

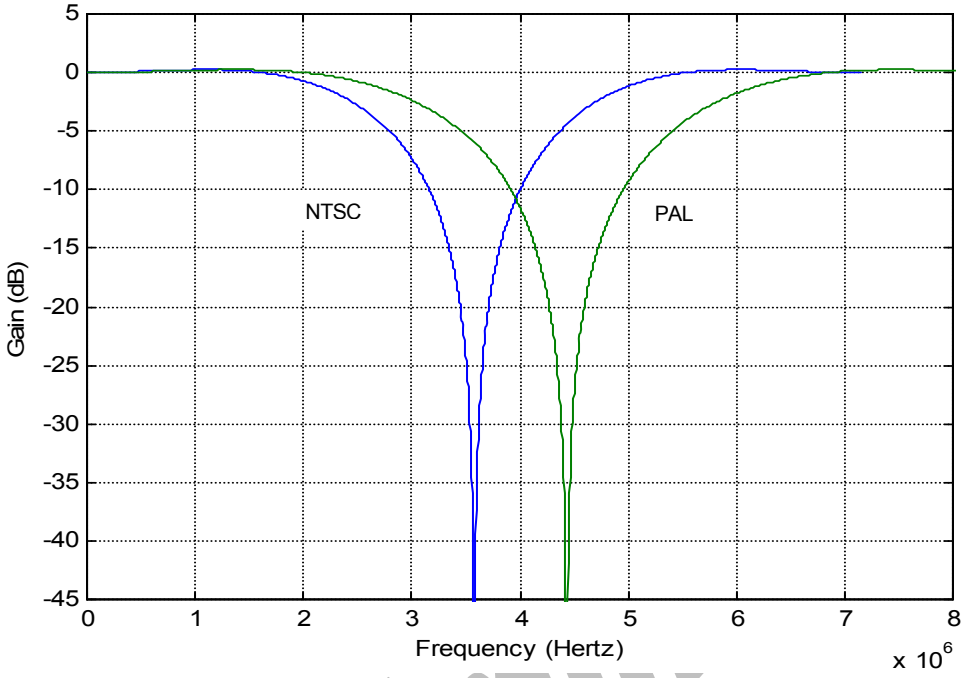
Decimation filter



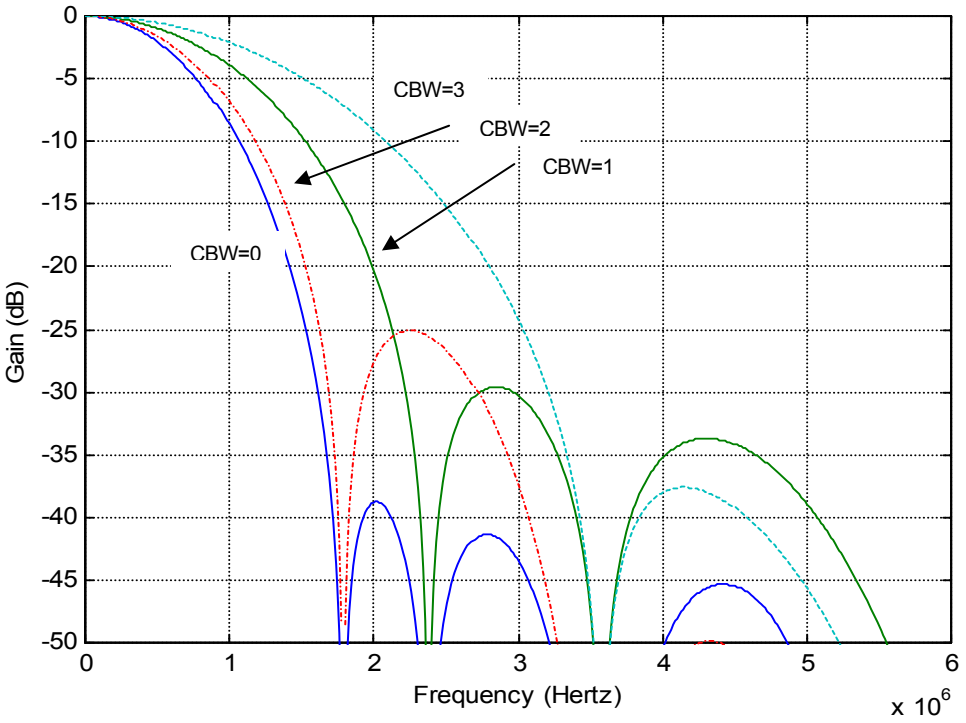
Chroma Band Pass Filter Curves



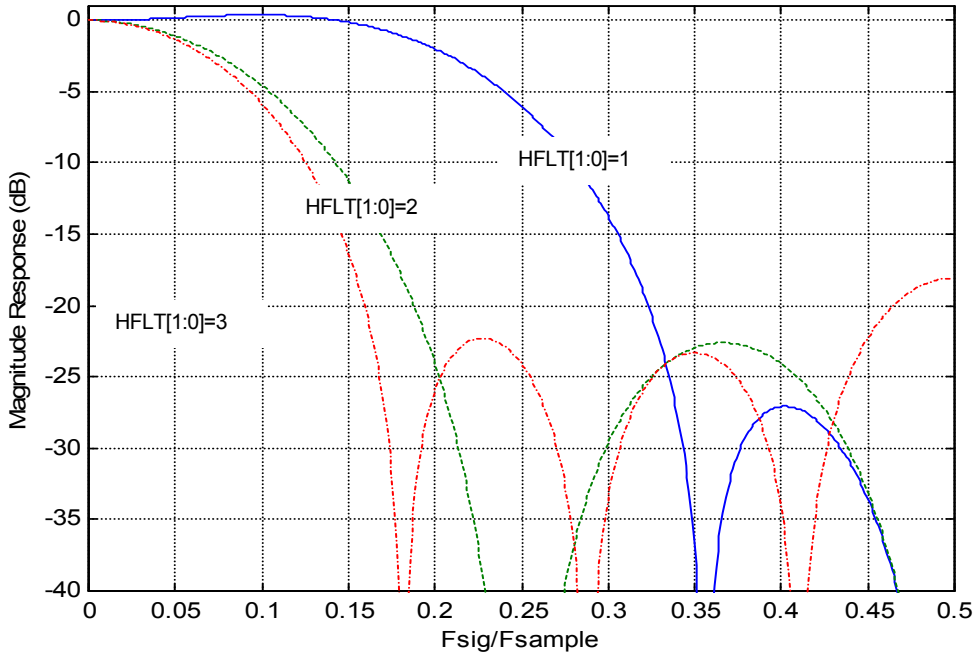
Luma Notch Filter Curve for NTSC and PAL



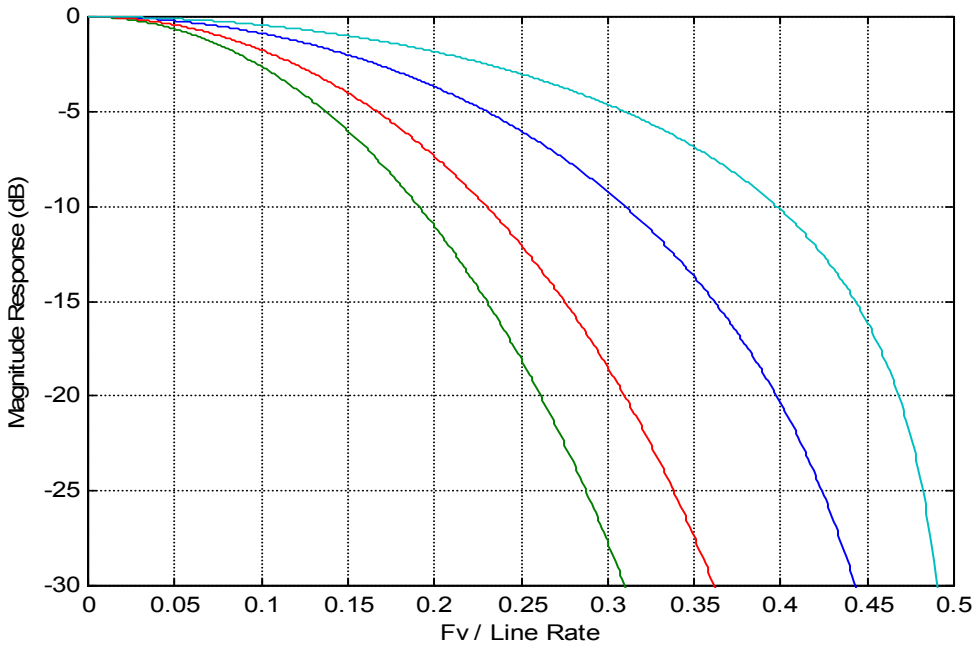
Chrominance Low-Pass Filter Curve



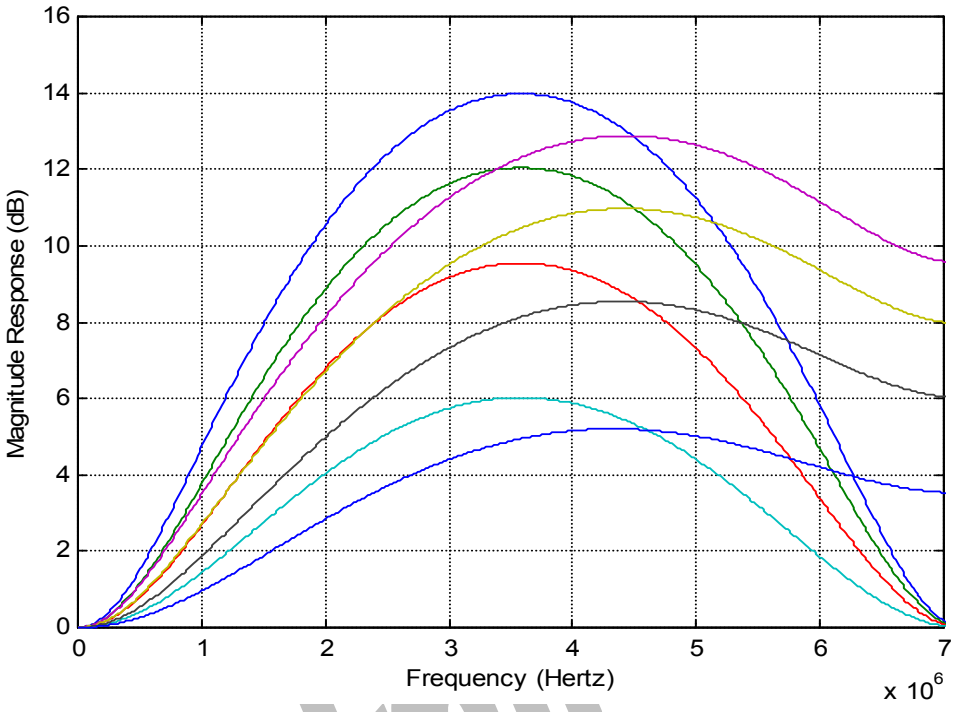
Horizontal Scaler Pre- Filter curves



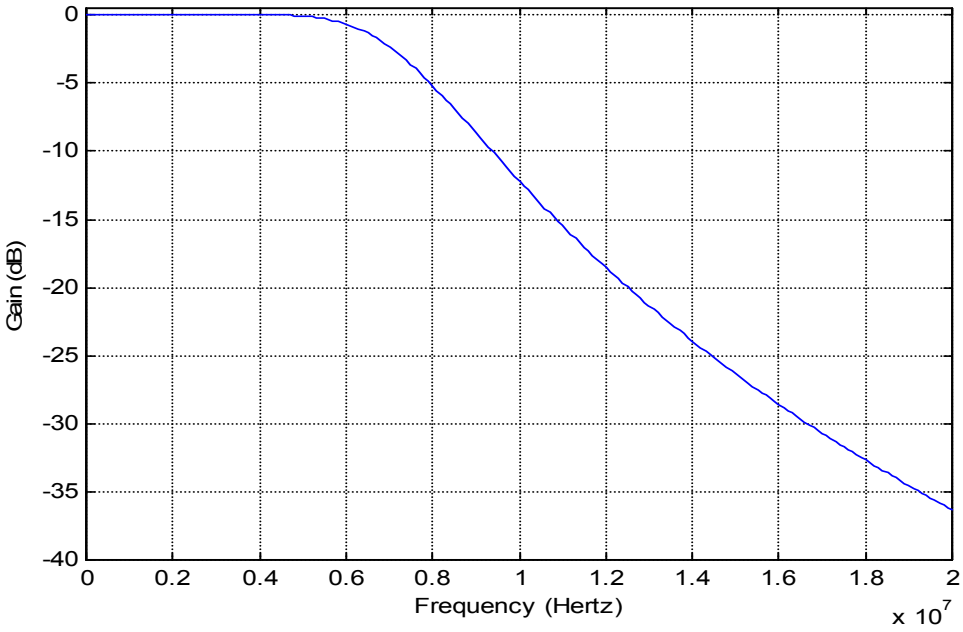
Vertical Interpolation Filter curves



Peaking Filter Curves



Anti-aliasing Filter Curves



Control Registers

Register Description

TW6816 supports two types of address spaces. The first one is configuration address space of the pre-defined PCI configuration registers. The second includes all the local registers. The local registers are used to control TW6816 functions and provide status information.Both the PCI configuration address space and the memory address space start at memory location 00h. The PCI based system distinguishes the two address spaces based on the Initialization Device Select, PCI address and command signals that are issued during power on. In this section, the following types are used to indicate how the registers are implemented:

RO: read only. Write has no effect.

WO: write only. Read will produce uncertain value.

R/W: read and write

RR: same as R/W, but writing "1" resets corresponding bit location; writing "0" has no effect.

PCI Function 0/1/2/3 Configuration Space Registers for Video

0x00 – Vendor ID and Device ID

Bit	Function	R/W	Description	Reset
31-16	Device ID	RO	TW6810 device ID Function 0 : 6810h Function 1 : 6811h Function 2 : 6812h Function 3 : 6813h	6810h/ 6811h/ 6812h/ 6813h
15-0	Vendor ID	RO	Techwell Inc PCI vendor ID	1797h

0x04 – Command and Status Register

Bit	Function	R/W	Description	Reset
31,30	Reserved	RO	These bits are hardwired to 0.	0h
29	Received Master Abort	RR	Set when master transaction is terminated with Master Abort.	0
28	Received Target Abort	RR	Set when master transaction is terminated with Target Abort.	0
27	Reserved	RO	This bit is hardwired to 0.	0
26,25	Address Decode Time	RO	Responds with medium DEVSEL timing.	01b
24-22	Reserved	RO	These bits are hardwired to 0.	0h
21	66MHz CAPABLE	RO	This bit is hardwired to 1.	1
20	New Capabilities	RO	A value of 1 indicates that the value read at PCI configuration offset is a pointer in configuration space to a linked list of new capabilities.	1
19-16	Reserved	RO	These bits are hardwired to 0.	0h
15-10	Reserved	RO	These bits are hardwired to 0.	0h
9	Fast Back-to-Back Enable	R/W	This bit should be set to 1 normally.	0
8	SERR# Enable	R/W	This bit should be set to 0 normally.	0
7	Stepping Control	RO	This bit is hardwired to 0.	0
6	Parity Error Response	R/W	This bit should be set to 0 normally.	0
5	VGA Palette Snoop	RO	This bit is hardwired to 0.	0
4	Memory Write and Invalidate Enable	R/W	This bit should be set to 1 normally.	0
3	Special Cycles	R/W	This bit must be set to 0.	0
2	Bus Master	R/W	A value of 1 enables this function space to act as a bus initiator.	0

1	Memory Space	R/W	A value of 1 enables response to memory space accesses (target decoded to memory mapped registers).	0
0	IO Space	RO	This bit is always "0".	0

0x08 – Revision ID and Class Code

Bit	Function	R/W	Description	Reset
31-8	Class code	RO	This function space is a multimedia video device	040000h
7-0	Revision ID	RO	Revision number	10h

0x0C – Cache Line Size

Bit	Function	R/W	Description	Reset
7-0	Cache Line Size	R/W	This read/write register specifies the system cacheline size in units of DWORDs. These bits should be set to 0 normally.	08h

0x0D – Latency Timer

Bit	Function	R/W	Description	Reset
15-8	Latency Timer	R/W	The number of PCI bus clocks for the latency timer used by the bus master. Once the latency expires, the master must initiate transaction termination as soon as GNT is removed.	40h

0x0E – Header Type

Bit	Function	R/W	Description	Reset
23-16	Header Type	RO	This chip is Multi-function PCI Device	80h

0x10 – Base Address 0

Bit	Function	R/W	Description	Reset
31-10	Relocatable Memory Pointer	R/W	Determine the location of the registers in the 32-bit addressable memory space.	Assigned by system at boot time
9-0	Memory Usage Specification	RO	Reserve 1kbytes of memory-mapped address space for local registers. Address space is prefetchable without side effects.	000h

0x2C – Subsystem ID and Subsystem Vendor ID

Bit	Function	R/W	Description	Reset
31-16	Subsystem ID	R	Function 0 : 6810h Function 1 : 6811h Function 2 : 6812h Function 3 : 6813h	6810h/ 6811h/ 6812h/ 6813h
15-0	Subsystem Vendor ID	R/W	Vendor specific.	1797h

0x34 – Capabilities Pointer

Bit	Function	R/W	Description	Reset
7-0	Cap_Ptr	RO	DWORD aligned byte address offset in configuration space to the first item in the list of capabilities.	44h

0x3C – Interrupt Line, Interrupt Pin, Min_Gnt, Max_Lat

Bit	Function	R/W	Description	Reset
31-24	Max_Lat	RO	Require bus access every 18us, at a minimum, in units of 250ns. Affects the desired settings for the latency timer value.	48h
23-16	Min_Gnt	RO	Desire a minimum grant burst period of 8us to empty data FIFO, in units of 250ns. Affects the desired settings for the latency timer value.	20h
15-8	Interrupt Pin	RO	Chip interrupt pin is connected to INTA, the only one usable by a single function device.	01h
7-0	Interrupt Line	R/W	The Interrupt Line register communicates interrupt line routing Information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the chip interrupt pin is connected. Device driver can use this value to determine interrupt priority and vector information.	System Assigned

0x44 – Power Management Capabilities

Bit	Function	R/W	Description	Reset
31-27	PME_Support	RO	The function does not capable of asserting the PME# signal.	00h
26	D2_Support	RO	The function does not support D2 state.	0
25	D1_Support	RO	The function does not support D1 state.	0
24-22	Aux_Current	RO	The function does not support PME# generation from $D3_{cold}$.	000b
21	DSI	RO	The function requires a device specific initialization sequence following transition to the D0 uninitialized state.	1
20	Reserved	RO		0
19	PME_Clk	RO	No PCI clock is requires for the function to generate PME#.	0
18-16	Version	RO	This function complies with Reversion 1.1 of PCI Power Management Interface Specification.	010b
15-8	Next_Item_Ptr	RO	Pointer to next item in the function's capability list. A value of 0 indicates there is no additional item.	00h
7-0	Cap_ID	RO	PCI power management capability ID.	01h

0x48 – Power Management Control/Status

Bit	Function	R/W	Description	Reset
31-24	Data	RO	The function does not support Data register.	00h
23-16	PMCSR_BSE	RO	The function does not support Bridge Support Extensions.	00h
15	PME_Status	RO	The function does not support PME# generation from $D3_{cold}$.	0
14-13	Data_Scale	RO	The function does not support Data register.	00b
12-9	Data_Select	RO	The function does not support Data register.	0h
8	PME_En	RO	The function does not support PME# generation from $D3_{cold}$.	0
7-2	Reserved	RO		00h
1-0	PowerState	R/W	This field is to determine the current power state of a function and to set the function into a new power state. 00 = D0 01 = D1 10 = D2 11 = $D3_{hot}$	00b

PCI Memory Space Registers for Video

Function 0 Video 1 Memory Register Summary

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
000	GAMMA	COLORF[2:0]			BSWAP		VFIFOEN	VDMAPEN	00
001	VDAMTRIG								16
002	Reserved							COLORF [3]	00
003	Reserved	S_BC_			Reserved	S_DM_			33
004	VDMAP_SA[7:0]								00
005	VDMAP_SA[15:8]								00
006	VDMAP_SA[23:16]								00
007	VDMAP_SA[31:24]								00
008	VDMAP_EXE[7:0]								00
009	VDMAP_EXE[15:8]								00
00A	VDMAP_EXE[23:16]								00
00B	VDMAP_EXE[31:24]								00
00C	VDMAP_PP[7:0]								00
00D	VDMAP_PP[15:8]								00
00E	VDMAP_PP[23:16]								00
00F	VDMAP_PP[31:24]								00
010 - 013	Reserved								00
014	SSDAT	SSCLK	Reserved				WREN	SBMODE	C0
015	SBCLK								A6
016	RDLEN				WDLEN				14
017	SBDEV							SBRW	01
018	WB1								00
019	WB2								00
01A	WB3								00
01B	WB4								00
01C	Reserved	VPABORT	VDMAPERR	Reserved	VFFOF	Reserved	VDMAPI	SBDONE	XX
01D	VFFERR	VPPERR	Reserved	Reserved	VIRQC				XX
01E	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	NOVIDEO	MONO	DET50	XX
01F	Reserved	MACRCH	STDCH	Reserved	Reserved	Reserved	EEPERR	SBERR	00
020	VINTMASK[7:0]								00
021	VINTMASK[15:8]								00
022	VINTMASK[23:16]								00
023	VINTMASK[31:24]								00
024 - 02B	Reserved								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
02C	UVSIGN	VDUMMY	SYNCSWAP	UVSWAP	RGB_PAT	RGB_SEL			00
02D	Reserved								00
02E	Reserved								00
02F	Reserved								00
030	RB1								00
031	RB2								00
032	RB3								00
033	RB4								00
034	Reserved							SBTRIG	00
035	Reserved								00
036	Reserved								00
037	Reserved								00
038 - 03F	Reserved								00
040	ODDEVENSEP	COLORF2[2:0]			BSWAP2		CAPEVENEN	CAPODDEN	00
041	Reserved								00
042	Reserved							COLORF2[3]	00
043	Reserved								00
044 - 4B	Reserved								00
04C	F1VREF								00
04D	F2VREF								00
04E	Reserved								00
04F	Reserved								00
050	Reserved							MR_VSVIDSEN	00
051	Reserved								00
052	Reserved								00
053	Reserved								00
054	MR_SUBSYSTEM_VENDOR_ID[7:0]								97
055	MR_SUBSYSTEM_VENDOR_ID[15:8]								17
056	MR_SUBSYSTEM_ID[7:0]								10
057	MR_SUBSYSTEM_ID[15:8]								68

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
058	Reserved	FUNC			Reserved				00
059	Revision ID								10
05A	Device ID[7:0]								10
05B	Device ID[15:8]								68
05C	Subsystem Vendor ID[7:0]								97
05D	Subsystem Vendor ID[15:8]								17
05E	Subsystem ID[7:0]								10
05F	Subsystem ID[15:8]								68
060	Reserved								08
061	Reserved		VADCCKPOL	Reserved					00
062	Reserved								00
063	Reserved								00
064	Reserved							RSTI2C	00
065	Reserved								00
066	Reserved								00
067	Reserved								00
068 - 077	Reserved								00
078	0	0	0	0	0	0	M66EN	0	0X
079	Reserved								00
07A	Reserved								00
07B	Reserved								00
07C - 1FF	Reserved								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
200	Reserved								C8
204	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	NOVIDEO	MONO	DET50	00
208	YSEL2	FC27	IFSEL		YSEL		Reserved		40
20C	Reserved								08
210	GMEN	CKHY		HSDLY					00
214	Reserved								00
218	SRESET	IREF	VREF	AGC_EN	CLKPDN	Y_PDN	Reserved		00
21C	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		02
220	VDELAY_LO								12
224	VACTIVE_LO								F0
228	HDELAY_LO								10
22C	HACTIVE_LO								D0
230	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CC
234	VSCALE_LO								00
238	VSCALE_HI				HSCALE_HI				11
23C	HSCALE_LO								00
240	BRIGHTNESS								00
244	CONTRAST								64
248	SCURVE	VSF	CTI		SHARPNESS				11
24C	SAT_U								80
250	SAT_V								80
254	HUE								00
258	-				-				00
25C	SHCOR				Reserved	VSHP			30
260	CTCOR		CCOR		VCOR		CIF		44
264	Reserved								00
268	Reserved				YFLEN	YSV	Reserved		00
26C	Reserved								00
270	DTSTUS	STDNOW			ATREG	STANDARD			07
274	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSC	7F
278	NT50	Reserved							08
27C	Reserved								00
280	CLPEND				CLPST				50
284	NMGAIN				WPGAIN			Agcgain8	42
288	AGCGAIN[7:0]								F0
28C	PEAKWT								D8
290	CLMPLD	CLMPL							BC
294	SYNCTD	SYNCT							B8
298	MISSCNT				HSWIN				44
29C	PCLAMP								2A
2A0	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00
2A4	BSHT		VSHT						00
2A8	CKILMAX	CKILMIN							78
2AC	HTL				VTL				4C

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
2B0	CKLM	YDLY			HFLT				**30**
2B4	HPLC	EVCNT	PALC	SDET	Reserved	BYPASS	Reserved		**14**
2B8	HPM		ACCT		SPM		CBW		**A5**
2BC	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	**E0**
2C0	sf	pf	ff	kf	CSBAD	MCVSN	CSTRIPE	CTYPE	**00**
2C4	VCR	WKAIR	WKAIR1	VSTD	NINTL	Reserved			**00**
2C8	HFREF								**X**
2CC	FRM		YNR		CLMD		PSP		**05**
2D0	IDX		NSEN / SSEN / PSEN / WKTH						**00**
2D4	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	**00**
2D8 - 3D8	Reserved								**00**
3DC	V2DELAY_HI		V2ACTIVE_HI		H2DELAY_HI		H2ACTIVE_HI		**02**
3E0	V2DELAY_LO								**12**
3E4	V2ACTIVE_LO								**F0**
3E8	H2DELAY_LO								**0F**
3EC	H2ACTIVE_LO								**D0**
3F0	Reserved							F2CNT	**0**
3F4	V2SCALE_LO								**00**
3F8	V2SCALE_HI				H2SCALE_HI				**11**
3FC	H2SCALE_LO								**00**

Function 0 Video 1 Memory Register Description

0x000 – VDMAC[31:4]

Bit	Function	R/W	Description	Reset
31	Reserved	RO		0
30-28	S_BC_	R/W	Dither Output Format Selection.These bits are effective when COLORF select RGB15 with Dither or RGB16 with Dither.These bits must be set to 2 or 3 when RGB15 with Dither or RGB16 with Dither are selected. 2: RGB16(RGB 5:6:5) mode 3: RGB15(RGB 5:5:5) mode Others: reserved.	3
27	Reserved	RO		0
26-24	S_DM_	R/W	Dither Option Code.3h is recommended for both RGB15 with Dither and RGB16 with Dither. If COLORF select RGB16 with Dither mode. Input LSBs Used in Dither Calculation Dither Method 1h: (2) (1) (2) 2x2 2h: (2,1) (1,0) (2,1) 2x2 3h: (2,1,0) (1,0),(2,1,0) 2x2 If COLORF select RGB15 with Dither mode. Input LSBs Used in Dither Calculation Dither Method 1h: (2) (2) (2) 2x2 2h: (2,1) (2,1) (2,1) 2x2 3h: (2,1,0) (2,1,0),(2,1,0) 2x2	3
23-17	Reserved	RO		0h
16	COLORF[3]	R/W	See bit6-4 description in this register.	0
15-8	VDMATRIG	R/W	DMA trigger point. This register defines the number of dwords of data pre-stored in Video FIFO before the DMA controller starts to burst data onto PCI bus.	16h
7	GAMMA	R/W	A value of 1 enables gamma correction removal with factor 2.2 for NTSC or 2.8 for PAL.	0
6-4	COLORF[2:0]	R/W	COLORF[3:0] bits select the color format of video data that is sent to FIFO. 0000 = RGB32 0001 = RGB24 0010 = RGB16 without Dither 0011 = RGB15 without Dither 0100 = YUY2 (YCbCr 4:2:2) 0101 = BtYUV(Y41P)(YCbCr 4:1:1) 0110 = Y411(YCnCr 4:1:1) 1010 = RGB16 with Dither 1011 = RGB15 with Dither Others = reserved.	000b

0x000 – VDMAC[3:0]

Bit	Function	R/W	Description	Reset
3-2	BSWAP	R/W	Byte Swap. The data bytes of packed dword are swapped before sent into FIFO according to the setting of this register. 00 = { byte 3, byte 2, byte 1, byte 0 }. 01 = { byte 2, byte 3, byte 0, byte 1 }. 10 = { byte 1, byte 0, byte 3, byte 2 }. 11 = { byte 0, byte 1, byte 2, byte 3 }.	00b
1	VFIFO_EN	R/W	Set to 1 to enable the video FIFO, 0 to flush the FIFO.	0
0	VDMAP_EN	R/W	A value of 1 enables the VIDEO DMA Programmer to process DMAP program starting from VDMAP_SA.	0

0x004 – VDMAP_SA

Bit	Function	R/W	Description	Reset
31-0	VDMAP_SA	R/W	The starting address of VIDEO DMAP in the memory address space.	00000000h

0x008 – VDMAP_EXE

Bit	Function	R/W	Description	Reset
31-0	VDMAP_EXE	RO	The dword of DMAP instruction packet that the VIDEO DMA Programmer is currently executing.	00000000h

0x00C – VDMAP_PP

Bit	Function	R/W	Description	Reset
31-0	VDMAP_PP	RO	The memory address of the last dword of VIDEO DMAP in memory address space fetched by the DMA Programmer.	00000000h

0x014 – SBUSC

Bit	Function	R/W	Description	Reset
31-25	SBDEV	R/W	This is the slave device chip address for Hardware mode.	00h
24	SBRW	R/W	Hardware Read/Write mode.1: read, 0:write	1
23	Reserved	RO		0
22-20	RDLEN	R/W	This register defines the number of bytes after Slave Chip Address to the last data byte in Serial Bus Read mode. This value must be 1h to 4h.	1h
19	Reserved	RO		0
18-16	WDLEN	R/W	This register defines the number of bytes after Slave Chip Address to the last data byte in Serial Bus Write mode. This value must be 1h to 4h.	4h
15-8	SBCLK	R/W	This register defines half of the clock period of serial bus in the number of PCI clocks. One clock period = 2xSBCLK PCI clocks. The recommended value is 0xA6 at 99.4kHz and 0x2A at 392.8kHz.	A6h
7	SSDAT	R/W	Read this bit to get the current status of SDAT in both software and hardware modes. In software mode, write a 0 to force SDAT low, write a 1 to release SDAT.	1
6	SSCLK	R/W	Read this bit to get the current status of SCLK in both software and hardware modes. In software mode, write a 0 to force SCLK low, write a 1 to release SCLK.	1
5-2	Reserved	RO		0h
1	WREN	R/W	This bit is only effective for Serial Bus Read Protocol. 0:sevd Device Chip address (with Read enable bit) and receive bytes. 1:Send Device Chip Address (with Write enable bit) and send WB1 1 byte, then send Device Chip Address (with Read enable bit) and receive bytes	0
0	SBMODE	R/W	This bit controls the operation of serial bus. 0: software mode. In this mode, driver software can control serial bus directly by reading and writing SSCLK and SSDAT. 1: Hardware mode.	0

0x018 – SBUSSD

Bit	Function	R/W	Description	Reset
31-24	WB4	R/W	The fourth data byte in a serial bus sends transaction.	00h
23-16	WB3	R/W	The third data byte in a serial bus send transaction.	00h
15-8	WB2	R/W	The second data byte in a serial bus send transaction.	00h
7-0	WB1	R/W	The first data byte in a serial bus send transaction after slave device chip address.	00h

0x01C – INTSTAT

Bit	Function	R/W	Description	Reset
31	Reserved	RR		0
30	MACROSTCH	RR	Set if Macrovision status changed.	0
29	STDCH	RR	Set if Video standard changed.	0
28-26	Reserved	RR		0
25	EEPERR	RR	Set if EEPROM read had errors on PCI initial time.	0
24	SBERR	RR	Set if the operation on serial bus was completed, but not successful. This bit is valid if SBDONE is set.	0
23	VDLOSS	RR	Set if VDLOSS bit in decoder status register changed.	0
22	HLOCK	RR	Set if HLOCK bit in decoder status register changed.	0
21	SLOCK	RR	Set if SLOCK bit in decoder status register changed.	0
20	FIELD	RR	Set if FIELD bit in decoder status register changed.	0
19	VLOCK	RR	Set if VLOCK bit in decoder status register changed.	0
18	NOVIDEO	RR	Set if NOVIDEO bit in decoder status register changed.	0
17	MONO	RR	Set if MONO bit in decoder status register changed.	0
16	DET50	RR	Set if DET50 bit in decoder status register changed.	0

0x01C – INTSTAT (cont.)

Bit	Function	R/W	Description	Reset
15	FFERR	RR	Set if the sync flag from Video FIFO is wrong in format or sequence.	0
14	PPERR	RR	Set if a parity error is detected on PCI bus.	0
13	SBERR2	RR	SBERR2 controlled by mask bit	0
12	SBDONE2	RR	SDONE2 controlled by mask bit	0
11-8	IRQC	RO	IRQC Counter Value. (Reserved)	0h
7	Reserved	RR	This bit is always 0.	0
6	PABORT	RR	Set if Chip is a PCI bus master and receives master or target abort.	0
5	DMAPERR	RR	Set if DMA Programmer detects any error occurs on DMAP program.	0
4	Reserved	RO	This bit is always 0.	0
3	FFOF	RR	Video FIFO is overflowed, and DMA programmer starts to drop data in FIFO.	0
2	Reserved	RR		0
1	VDMAPI	RR	When the IRQ bit in the DMAP instruction packet is set, this bit is set after DMA Programmer completes the Video data instruction.	0
0	SBDONE	RR	Set when serial bus has completed a read or write operation.	0

0x020 – INTMASK

Bit	Function	R/W	Description	Reset
31-0	INTMASK	R/W	Writing a 1 to INTMASK[n] enables the interrupt bit INTSTAT[n].	00000000h

0x02C – RGB_PAT

Bit	Function	R/W	Description	Reset
31-8	Reserved	RO		0h
7	UVSIGN	R/W	1:Cb and Cr data are changed into signed data. Bit7 is inversed. 0: Cb and Cr data are normal.	0
6	VDUMMY	R/W	1:Dummy data output on PCI Bus.(Test Purpose only) 0:normal video data output on PCI Bus.	0
5	SYNCSWAP	R/W	1:Video field information inversed on Video data. 0:Video field information not inversed on Video data.	0
4	UVSWAP	R/W	1: Cb and Cr data position is swapped. 0: not swapped.	0
3	RGB_PAT	R/W	RGB Test Pattern Selection. 0:disabled, 1:enabled by RGB_SEL color	0
2-0	RGB_SEL	R/W	RGB Color Pattern Selection. 000 = Black. 001 = Blue. 010 = Green. 011 = Cyan. 100 = Red. 101 = Magenta. 110 = Yellow. 111 = white.	0h

0x030 – SBUSRD

Bit	Function	R/W	Description	Reset
31-24	RB4	RO	The fourth data byte in a serial bus receive transaction.	00h
23-16	RB3	RO	The third data byte in a serial bus receive transaction.	00h
15-8	RB2	RO	The second data byte in a serial bus receive transaction.	00h
7-0	RB1	RO	The first data byte in a serial bus receive transaction after slave device chip address.	00h

0x034 – SBUSTRIG

Bit	Function	R/W	Description	Reset
0	SBTRIG	WO	Write a 1 to trigger hardware state machine to perform Serial bus functions. This bit is rest to “0” automatically. SBMODE must be 1 when this function is used.	0

0x040 – Video Capture Control

Bit	Function	R/W	Description	Reset
31-17	Reserved	RO		0h
16	COLORF2[3]	R/W	See bit6-4 description in this register.	0
15-8	Reserved	RO		0h
7	ODDEVENSEP	R/W	1:Odd/Even field data separate control.0: no separate	0
6-4	COLORF2[2:0]	R/W	COLORF2[3:0] bits select the color format of video data that is sent to FIFO in Even field data if ODDEVENSEP is set to 1. 0000 = RGB32 0001 = RGB24 0010 = RGB16 without Dither 0011 = RGB15 without Dither 0100 = YUY2 (YCbCr 4:2:2) 0101 = BtYUV(Y41P)(YCbCr 4:1:1) 0110 = Y411(YCnCr 4:1:1) 1010 = RGB16 with Dither 1011 = RGB15 with Dither Others = reserved.	0h
3-2	BSWAP2	R/W	Byte Swap. The data bytes of packed dword are swapped before sent into FIFO according to the setting of this register in Even field data if ODDEVENSEP is set to 1. 00 = { byte 3, byte 2, byte 1, byte 0 }. 01 = { byte 2, byte 3, byte 0, byte 1 }. 10 = { byte 1, byte 0, byte 3, byte 2 }. 11 = {byte 0, byte 1, byte 2, byte 3}.	0h
1	CAP_EVEN_EN	R/W	1:Even field capture enable, 0:disable	1
0	CAP_ODD_EN	R/W	1:Odd field capture enable, 0:disable	1

0x04C – VIDEO FRAME DROP CONTROL

Bit	Function	R/W	Description	Reset
15-8	F2VREF	R/W	00h: no video dropping. Others: FIELD 2 Video is dropped by 1/(F2VREF + 1) rate.	00h
7-0	F1VREF	R/W	00h: no video dropping. Others: FIELD 1 Video is dropped by 1/(F1VREF + 1) rate.	00h

0x050 – VIDEO SVIDS

Bit	Function	R/W	Description	Reset
0	MR_VSVIDSEN	R/W	1:SubsystemID/SubsystemVendorID registers in Video CFG are set by VIDEO SUBSYS register (Test purpose only) 0:no	0

0x054 – MR VIDEO SUBSYS

Bit	Function	Type	Description	Reset
31-16	MR_SUBSYSTEM_ID	R/W	Subsystem ID value set by MR_VSVIDSEN mode. (Test purpose only)	6810h
15:0	MR_SUBSYSTEM_VENDOER_ID	R/W	Subsystem Vendor ID value set by MR_VSVIDSEN mode.(Test purpose only)	1797h

0x058 – DEVICE ID

Bit	Function	Type	Description	Reset
31-16	DEVICE ID	RO	These bits show Device ID value in PCI Configuration Space Registers.	6810h
15-8	REV_ID	RO	These bits show Revision ID value in PCI Configuration Space Registers.	10h
7	Reserved	RO		0
6-4	FUNC	RO	These bits show Function space number in this Function space.	0h
3-0	Reserved	RO		0h

0x058 – SUBSYSTEM ID

Bit	Function	Type	Description	Reset
31-16	Subsystem ID	RO	These bits show Subsystem ID value in PCI Configuration Space Registers.	6810h
15-0	Subsystem Vendor ID	RO	These bits show Subsystem Vendor ID value in PCI Configuration Space Registers.	1797h

0x060– VADCKPOL

Bit	Function	Type	Description	Reset
13	VADCCKPOL	R/W	1: Video ADC clock polarity inverse. 0: not inverse.	0
12-0	Reserved	RW		040h

0x064 – I2C RST

Bit	Function	R/W	Description	Reset
0	RSTI2C	WO	Write “1” reset I2C master block. This register bit is set to “0” after write “1” automatically.	0

0x078 – M66EN

Bit	Function	R/W	Description	Reset
1	M66EN	RO	M66EN pin status. 0:33MHz PCI Bus is connected to TW6816. 1:66MHz PCI Bus is connected to TW6816.	X
0	Reserved	RO		0

0x204 – Decoder Status Register 1 (STATUS1)

Bit	Function	R/W	Description	Reset
7	VDLOSS	RO	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
6	HLOCK	RO	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	RO	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	RO	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	RO	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	NOVIDEO	RO	1=No Video 0=Video	0
1	MONO	RO	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	RO	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x208 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7	Reserved	RO		0
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.(special purpose only)	1
5-4	IFSEL	R/W	00 = Composite video decoding	0h
3-2	YSEL	R/W	These two bits control the input video selection. 00 = VIN1A selected 01 = VIN1B selected 10 = VIN2C selected 11 = VIN1D selected	0h
1-0	Reserved	RO		0h

0x210 – GAMMA and HSYNC Delay Control

Bit	Function	R/W	Description	Reset
7	GMEN	R/W	Reserved	0
6-5	CKHY	R/W	Color killer sensitivity. Lower value gives higher sensitivity.	0h
4-0	HSDLY	R/W	Reserved.	0h

0x218 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	SRESET	WO	A 1 written to this bit resets the device to its default state but all register content remain unchanged. This bit is self-resetting.	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference 2.	0
5	VREF	R/W	1 = Internal voltage reference. 0 = external voltage reference using VCOM, VREFP and VREFN.	0
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = System clock in power down mode.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1-0	Reserved	RO	Reserved for future use	0

0x21C – Cropping Register High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	0
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0x220 – Vertical Delay Register Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12h

0x224 – Vertical Active Register Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0h

0x228 – Horizontal Delay Register Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	10h

0x22C – Horizontal Active Register Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0h

0x230 – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Reserved	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC 0 = Notch filter	1
2	HCOMP	R/W	1 = operation mode 1. (recommended) 0 = mode 0.	1
1	YCOMB	R/W	This bit controls the Y comb. 1 = Y output is the averaging of two adjacent lines. 0 = No comb.	0
0	PDLY	R/W	PAL delay line. 1 = enabled. 0 = disabled.	1

0x234 – Vertical Scaling Register, Low (VSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	VSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register	00h

0x238 – Scaling Register High (SCALE_HI)

Bit	Function	R/W	Description	Reset
7-4	VSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register.	1
3-0	HSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register.	1

0x23C – Horizontal Scaling Register Low (HSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	HSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register.	00h

0x240 – BRIGHTNESS Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00h

0x244 – CONTRAST Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	CONTRAST	R/W	These bits control the luminance contrast gain.A value of 100(64h) has a gain of 1.The range od adjustment is from 0% to 255% at 1% per step.	64h

0x248 – SHARPNESS Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the center frequency of peaking filter.The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	1
5-4	CTI	R/W	CTI level selection. 0 = none. 3 = highest.	1h
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest.	1h

0x24C – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80h

0x250 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80h

0x254 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from $+36^{o}$ (7Fh) to -36^{o} (80h) with an increment of 0.28^{o}. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0^{o} (00h). This is effective only on NTSC system.	00h

0x25C – Vertical Sharpness (VSHARP)

Bit	Function	R/W	Description	Reset
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	8h
3	Reserved	RO	Reserved	0
2-0	VSHP	R/W	Vertical peaking level. 0 = none. 7 = highest.	0

0x260 – Coring Control Register (CORING)

Bit	Function	R/W	Description	Reset
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0x268 – Analog Control II

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		0
3	YFLEN	R/W	Y-Ch anti-alias filter control 1 = enable 0 = disable	0
2	YSV	R/W	Y-Ch power saving mode 1 = enable 0 = disable	0
1-0	Reserved	R/W		0

0x270 – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	RO	0 = Idle 1 = detection in progress	0
6-4	STDNOW	RO	Current standard invoked 0 = NTSC (M) 1 = PAL (B, D, G, H, I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC (M) 1 = PAL (B, D, G, H, I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0x274 – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B, D, G, H, I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0x278 – NT50

Bit	Function	R/W	Description	Reset
7	NT50	R/W	1 = Force decoding format to 50Hz NTSC. 0 = decoding format is set by register 0x270 (SDT)	0
6-0	Reserved	R/W		08h

0x280 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping time is determined by this together with CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0

0x284 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN8	R/W	This bit is the MSB of the 9-bit register that controls the AGC gain when AGC loop is disabled.	0

0x288 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0

0x28C – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. Setting 'FF' can disable this function.	D8

0x290– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	0
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3Ch

0x294– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	0
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38h

0x298 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits determine the VCR detection sensitivity.	4

0x29C – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	28h

0x2A0 – Vertical Control I (VCNTL1)

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = long 0 = normal	0

0x2A4 – Vertical Control II (VCNTL2)

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control for test.	0
5-0	VSHT	R/W	Vsync output delay control in the increment of half line length.	00

0x2A8 – Color Killer Level Control (CKILL)

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	28

0x2AC – Comb Filter Control (COMB)

Bit	Function	R/W	Description	Reset
7-4	HTL	R/W	Adaptive Comb filter control.	4
3-0	VTL	R/W	Adaptive Comb filter combing strength control. Higher value provides stronger comb filtering.	4

0x2B0 – Luma Delay and H Filter Control (LDLY)

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	HFLT	R/W	If HSCALE[11-8]=1,HFLT [3:0] controls the peaking function. If HSCALE[11-8]>1,HFLT [2:0] function is bellow. Pre-filter selection for horizontal scaler 1** = Bypass 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image 010 = Recommended for QCIF size image 011 = Recommended for ICON size image	0

0x2B4 – Miscellaneous Control I (MISC1)

Bit	Function	R/W	Description	Reset
7	HPLC	R/W	Reserved for future use.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
5	PALC	R/W	Reserved for future use.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	Reserved	RO		0
2	BYPASS	R/W	Reserved for future use.	1
1-0	Reserved	RO		0

0x2B8 – LOOP Control Register (LOOP)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Slow	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0x2BC – Miscellaneous Control II (MISC2)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0x2C0 – Macrovision Detection (MVSN)

Bit	Function	R/W	Description	Reset
7	SF	RO	Reserved	0
6	PF	RO	Reserved	0
5	FF	RO	Reserved	0
4	KF	RO	Reserved	0
3	CSBAD	RO	1 = Macrovision color stripe detection may be un-reliable	0
2	MCVSN	RO	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	RO	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	RO	This bit is valid only when color stripe protection is detected, i.e. Cstripe=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0x2C4 – Decoder Chip STATUS II (STATUS2)

Bit	Function	R/W	Description	Reset
7	VCR	RO	1 = VCR signal	0
6	WKAIR	RO	1 = Weak signal	0
5	WKAIR1	RO	Weak signal indicator 2	0
4	VSTD	RO	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	RO	1 = Non-interlaced signal 0 = interlaced signal	0
2-0	Reserved	RO		0

0x2C8 – H monitor (HFREF)

Bit	Function	R/W	Description	Reset
7-0	HFREF	RO	Horizontal line frequency indicator(Test purpose only).	X

0x2CC – CLAMP MODE (CLMD)

Bit	Function	R/W	Description	Reset
7-6	FRM	R/W	Free run mode control 0 = Auto 2 = default to 60Hz 3 = default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None 1 = smallest 2 = small 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = low 1 = medium 2 = high	1

0x2D0 – ID Detection Control (IDCNTL)

Bit	Function	R/W	Description	Reset
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1E / 18 / 1C / 2A

0x2D4 – Clamp Control I (CLCNTL1)

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control for debugging use.	0
6	YCLEN	R/W	1 = Y channel clamp disabled 0 = Enabled.	0
5-4	Reserved	R/W		0
3	GTEST	R/W	1 = Test. 0 = Normal operation.	0
2	VLPF	R/W	Sync filter BW control. 0 = Normal	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0x3DC – Field2 Cropping High (F2CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	V2DELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Field2 Vertical Delay register.	0h
5-4	V2ACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit Field2 VACTIVE register. Refer to description on Reg09 for its shadow register.	0h
3-2	H2DELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Field2 Horizontal Delay register.	0h
1-0	H2ACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit Field2 HACTIVE register.	2h

0x3E0 – Field2 Vertical Delay Low (F2VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	V2DELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Field2 Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12h

0x3E4 – Field2 Vertical Active Low (F2VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	V2ACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Field2 Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0h

0x3E8 – Field2 Horizontal Delay Low (F2HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	H2DELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Field2 Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0Fh

0x3EC – Field2 Horizontal Active Low (F2HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	H2ACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Field2 Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0h

0x3F0 – Field2 Control (F2CNT)

Bit	Function	R/W	Description	Reset
0	F2CNT	R/W	1:Field2 Video Capture Controlled by V2DELAY, V2ACTIVE, H2DELAY, and H2ACTIVE, V2SCALE, H2SCALE field2 registers. 0:Field2 Video Capture Controlled by VDELAY, VACTIVE, HDELAY, HACTIVE, VSCALE, HSCALE registers.	0

0x3F4 – Field2 Vertical Scaling Low (F2VSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	V2SCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit Field2 vertical scaling ratio register	00h

0x3F8 – Field2 Scaling High (F2SCALE_HI)

Bit	Function	R/W	Description	Reset
7-4	V2SCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit Field2 vertical scaling ratio register.	1h
3-0	H2SCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit Field2 horizontal scaling ratio register.	1h

0x3FC – Field2 Horizontal Scaling Low (F2HSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	H2SCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit Field2 horizontal scaling ratio register.	00h

Function 1/2/3 Video 2/3/4 Memory Register Summary

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
000	GAMMA	COLORF[2:0]			BSWAP		VFIFOEN	VDMAPEN	00
001	VDAMTRIG								16
002	Reserved							COLORF [3]	00
003	Reserved	S_BC_			Reserved	S_DM_			33
004	VDMAP_SA[7:0]								00
005	VDMAP_SA[15:8]								00
006	VDMAP_SA[23:16]								00
007	VDMAP_SA[31:24]								00
008	VDMAP_EXE[7:0]								00
009	VDMAP_EXE[15:8]								00
00A	VDMAP_EXE[23:16]								00
00B	VDMAP_EXE[31:24]								00
00C	VDMAP_PP[7:0]								00
00D	VDMAP_PP[15:8]								00
00E	VDMAP_PP[23:16]								00
00F	VDMAP_PP[31:24]								00
010 - 01B	Reserved								00
01C	Reserved	VPABORT	VDMAPERR	Reserved	VFFOF	Reserved	VDMAPI	SBDONE	XX
01D	VFFERR	VPPERR	Reserved	Reserved	VIRQC				XX
01E	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	NOVIDEO	MONO	DET50	XX
01F	Reserved	MACRCH	STDCH	Reserved	Reserved	Reserved	EEPERR	SBERR	00
020	VINTMASK[7:0]								00
021	VINTMASK[15:8]								00
022	VINTMASK[23:16]								00
023	VINTMASK[31:24]								00
024 - 02B	Reserved								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
02C	UVSIGN	VDUMMY	SYNCSWAP	UVSWAP	RGB_PAT	RGB_SEL			00
02D	Reserved								00
02E	Reserved								00
02F	Reserved								00
030 - 03F	Reserved								00
040	ODDEVENSEP	COLORF2[2:0]			BSWAP2		CAPEVENEN	CAPODDEN	00
041	Reserved								00
042	Reserved							COLORF2[3]	00
043	Reserved								00
044 - 4B	Reserved								00
04C	F1VREF								00
04D	F2VREF								00
04E	Reserved								00
04F	Reserved								00
050 - 057	Reserved								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
058	Reserved	FUNC			Reserved				10/20/30
059	Revision ID								10
05A	Device ID[7:0]								11/12/13
05B	Device ID[15:8]								68
05C	Subsystem Vendor ID[7:0]								97
05D	Subsystem Vendor ID[15:8]								17
05E	Subsystem ID[7:0]								11/12/13
05F	Subsystem ID[15:8]								68
060	Reserved								08
061	Reserved								00
062	Reserved								00
063	Reserved								00
064 - 077	Reserved								00
078	0	0	0	0	0	0	M66EN	0	0X
079	Reserved								00
07A	Reserved								00
07B	Reserved								00
07C - 1FF	Reserved								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
200	Reserved								C8
204	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	NOVIDEO	MONO	DET50	00
208	YSEL2	FC27	IFSEL		YSEL		Reserved		40
20C	Reserved								08
210	GMEN	CKHY		HSDLY					00
214	Reserved								00
218	SRESET	IREF	VREF	AGC_EN	CLKPDN	Y_PDN	Reserved		00
21C	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		02
220	VDELAY_LO								12
224	VACTIVE_LO								F0
228	HDELAY_LO								10
22C	HACTIVE_LO								D0
230	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CC
234	VSCALE_LO								00
238	VSCALE_HI				HSCALE_HI				11
23C	HSCALE_LO								00
240	BRIGHTNESS								00
244	CONTRAST								64
248	SCURVE	VSF	CTI		SHARPNESS				11
24C	SAT_U								80
250	SAT_V								80
254	HUE								00
258	-				-				00
25C	SHCOR				Reserved	VSHP			30
260	CTCOR		CCOR		VCOR		CIF		44
264	Reserved								00
268	Reserved				YFLEN	YSV	Reserved		00
26C	Reserved								00
270	DTSTUS	STDNOW			ATREG	STANDARD			07
274	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSC	7F
278	NT50	Reserved							08
27C	Reserved								00
280	CLPEND				CLPST				50
284	NMGAIN				WPGAIN			Agcgain8	42
288	AGCGAIN[7:0]								F0
28C	PEAKWT								D8
290	CLMPLD	CLMPL							BC
294	SYNCTD	SYNCT							B8
298	MISSCNT				HSWIN				44
29C	PCLAMP								2A
2A0	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00
2A4	BSHT		VSHT						00
2A8	CKILMAX	CKILMIN							78
2AC	HTL				VTL				4C

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
2B0	CKLM	YDLY			HFLT				**30**
2B4	HPLC	EVCNT	PALC	SDET	Reserved	BYPASS	Reserved		**14**
2B8	HPM		ACCT		SPM		CBW		**A5**
2BC	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	**E0**
2C0	sf	pf	ff	kf	CSBAD	MCVSN	CSTRIPE	CTYPE	**00**
2C4	VCR	WKAIR	WKAIR1	VSTD	NINTL	Reserved			**00**
2C8	HFREF								**X**
2CC	FRM		YNR		CLMD		PSP		**05**
2D0	IDX		NSEN / SSEN / PSEN / WKTH						**00**
2D4	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	**00**
2D8 - 3D8	Reserved								**00**
3DC	V2DELAY_HI		V2ACTIVE_HI		H2DELAY_HI		H2ACTIVE_HI		**02**
3E0	V2DELAY_LO								**12**
3E4	V2ACTIVE_LO								**F0**
3E8	H2DELAY_LO								**0F**
3EC	H2ACTIVE_LO								**D0**
3F0	Reserved							F2CNT	**0**
3F4	V2SCALE_LO								**00**
3F8	V2SCALE_HI				H2SCALE_HI				**11**
3FC	H2SCALE_LO								**00**

Function 1/2/3 Video 2/3/4 Memory Register Description

0x000 – VDMAC[31:4]

Bit	Function	R/W	Description	Reset
31	Reserved	RO		0
30-28	S_BC_	R/W	Dither Output Format Selection.These bits are effective when COLORF select RGB15 with Dither or RGB16 with Dither.These bits must be set to 2 or 3 when RGB15 with Dither or RGB16 with Dither are selected. 2: RGB16(RGB 5:6:5) mode 3: RGB15(RGB 5:5:5) mode Others: reserved.	3
27	Reserved	RO		0
26-24	S_DM_	R/W	Dither Option Code.3h is recommended for both RGB15 with Dither and RGB16 with Dither. If COLORF select RGB16 with Dither mode. Input LSBs Used in Dither Calculation Dither Method 1h: (2) (1) (2) 2x2 2h: (2,1) (1,0) (2,1) 2x2 3h: (2,1,0) (1,0),(2,1,0) 2x2 If COLORF select RGB15 with Dither mode. Input LSBs Used in Dither Calculation Dither Method 1h: (2) (2) (2) 2x2 2h: (2,1) (2,1) (2,1) 2x2 3h: (2,1,0) (2,1,0),(2,1,0) 2x2	3
23-17	Reserved	RO		0h
16	COLORF[3]	R/W	See bit6-4 description in this register.	0
15-8	VDMATRIG	R/W	DMA trigger point. This register defines the number of dwords of data pre-stored in Video FIFO before the DMA controller starts to burst data onto PCI bus.	16h
7	GAMMA	R/W	A value of 1 enables gamma correction removal with factor 2.2 for NTSC or 2.8 for PAL.	0
6-4	COLORF[2:0]	R/W	COLORF[3:0] bits select the color format of video data that is sent to FIFO. 0000 = RGB32 0001 = RGB24 0010 = RGB16 without Dither 0011 = RGB15 without Dither 0100 = YUY2 (YCbCr 4:2:2) 0101 = BtYUV(Y41P)(YCbCr 4:1:1) 0110 = Y411(YCnCr 4:1:1) 1010 = RGB16 with Dither 1011 = RGB15 with Dither Others = reserved.	000b

0x000 – VDMAC[3:0]

Bit	Function	R/W	Description	Reset
3-2	BSWAP	R/W	Byte Swap. The data bytes of packed dword are swapped before sent into FIFO according to the setting of this register. 00 = { byte 3, byte 2, byte 1, byte 0 }. 01 = { byte 2, byte 3, byte 0, byte 1 }. 10 = { byte 1, byte 0, byte 3, byte 2 }. 11 = { byte 0, byte 1, byte 2, byte 3 }.	00b
1	VFIFO_EN	R/W	Set to 1 to enable the video FIFO, 0 to flush the FIFO.	0
0	VDMAP_EN	R/W	A value of 1 enables the VIDEO DMA Programmer to process DMAP program starting from VDMAP_SA.	0

0x004 – VDMAP_SA

Bit	Function	R/W	Description	Reset
31-0	VDMAP_SA	R/W	The starting address of VIDEO DMAP in the memory address space.	00000000h

0x008 – VDMAP_EXE

Bit	Function	R/W	Description	Reset
31-0	VDMAP_EXE	RO	The dword of DMAP instruction packet that the VIDEO DMA Programmer is currently executing.	00000000h

0x00C – VDMAP_PP

Bit	Function	R/W	Description	Reset
31-0	VDMAP_PP	RO	The memory address of the last dword of VIDEO DMAP in memory address space fetched by the DMA Programmer.	00000000h

0x01C – INTSTAT

Bit	Function	R/W	Description	Reset
31	Reserved	RR		0
30	MACROSTCH	RR	Set if Macrovision status changed.	0
29	STDCH	RR	Set if Video standard changed.	0
28-26	Reserved	RR		0
25	EEPERR	RR	Set if EEPROM read had errors on PCI initial time.	0
24	Reserved	RR		0
23	VDLOSS	RR	Set if VDLOSS bit in decoder status register changed.	0
22	HLOCK	RR	Set if HLOCK bit in decoder status register changed.	0
21	SLOCK	RR	Set if SLOCK bit in decoder status register changed.	0
20	FIELD	RR	Set if FIELD bit in decoder status register changed.	0
19	VLOCK	RR	Set if VLOCK bit in decoder status register changed.	0
18	NOVIDEO	RR	Set if NOVIDEO bit in decoder status register changed.	0
17	MONO	RR	Set if MONO bit in decoder status register changed.	0
16	DET50	RR	Set if DET50 bit in decoder status register changed.	0

0x01C – INTSTAT (cont.)

Bit	Function	R/W	Description	Reset
15	FFERR	RR	Set if the sync flag from Video FIFO is wrong in format or sequence.	0
14	PPERR	RR	Set if a parity error is detected on PCI bus.	0
13-12	Reserved	RR		0
11-8	IRQC	RO	IRQC Counter Value. (Reserved)	0h
7	Reserved	RR	This bit is always 0.	0
6	PABORT	RR	Set if Chip is a PCI bus master and receives master or target abort.	0
5	DMAPERR	RR	Set if DMA Programmer detects any error occurs on DMAP program.	0
4	Reserved	RO	This bit is always 0.	0
3	FFOF	RR	Video FIFO is overflowed, and DMA programmer starts to drop data in FIFO.	0
2	Reserved	RR		0
1	VDMAPI	RR	When the IRQ bit in the DMAP instruction packet is set, this bit is set after DMA Programmer completes the Video data instruction.	0
0	Reserved	RR		0

0x020 – INTMASK

Bit	Function	R/W	Description	Reset
31-0	INTMASK	R/W	Writing a 1 to INTMASK[n] enables the interrupt bit INTSTAT[n].	00000000h

0x02C – RGB_PAT

Bit	Function	R/W	Description	Reset
31-8	Reserved	RO		0h
7	UVSIGN	R/W	1:Cb and Cr data are changed into signed data. Bit7 is inversed. 0: Cb and Cr data are normal.	0
6	VDUMMY	R/W	1:Dummy data output on PCI Bus.(Test Purpose only) 0:normal video data output on PCI Bus.	0
5	SYNCSWAP	R/W	1:Video field information inversed on Video data. 0:Video field information not inversed on Video data.	0
4	UVSWAP	R/W	1: Cb and Cr data position is swapped. 0: not swapped.	0
3	RGB_PAT	R/W	RGB Test Pattern Selection. 0:disabled, 1:enabled by RGB_SEL color	0
2-0	RGB_SEL	R/W	RGB Color Pattern Selection. 000 = Black. 001 = Blue. 010 = Green. 011 = Cyan. 100 = Red. 101 = Magenta. 110 = Yellow. 111 = white.	0h

0x040 – Video Capture Control

Bit	Function	R/W	Description	Reset
31-17	Reserved	RO		0h
16	COLORF2[3]	R/W	See bit6-4 description in this register.	0
15-8	Reserved	RO		0h
7	ODDEVENSEP	R/W	1:Odd/Even field data separate control.0: no separate.	0
6-4	COLORF2[2:0]	R/W	COLORF2[3:0] bits select the color format of video data that is sent to FIFO in Even field data if ODDEVENSEP is set to 1. 0000 = RGB32 0001 = RGB24 0010 = RGB16 without Dither 0011 = RGB15 without Dither 0100 = YUY2 (YCbCr 4:2:2) 0101 = BtYUV(Y41P)(YCbCr 4:1:1) 0110 = Y411(YCnCr 4:1:1) 1010 = RGB16 with Dither 1011 = RGB15 with Dither Others = reserved.	0h
3-2	BSWAP2	R/W	Byte Swap. The data bytes of packed dword are swapped before sent into FIFO according to the setting of this register in Even field data if ODDEVENSEP is set to 1. 00 = { byte 3, byte 2, byte 1, byte 0 }. 01 = { byte 2, byte 3, byte 0, byte 1 }. 10 = { byte 1, byte 0, byte 3, byte 2 }. 11 = {byte 0, byte 1, byte 2, byte 3}.	0h
1	CAP_EVEN_EN	R/W	1:Even field capture enable, 0:disable	1
0	CAP_ODD_EN	R/W	1:Odd field capture enable, 0:disable	1

0x04C – VIDEO FRAME DROP CONTROL

Bit	Function	R/W	Description	Reset
15-8	F2VREF	R/W	00h: no video dropping. Others: FIELD 2 Video is dropped by 1/(F2VREF + 1) rate.	00h
7-0	F1VREF	R/W	00h: no video dropping. Others: FIELD 1 Video is dropped by 1/(F1VREF + 1) rate.	00h

0x058 – DEVICE ID

Bit	Function	Type	Description	Reset
31-16	DEVICE ID	RO	These bits show Device ID value in PCI Configuration Space Registers. Reset value: Function1 Video2 : 6811h Function2 Video3 : 6812h Function3 Video4 : 6813h	6811h/ 6812h/ 6813h
15-8	REV_ID	RO	These bits show Revision ID value in PCI Configuration Space Registers.	10h
7	Reserved	RO		0
6-4	FUNC	RO	These bits show Function space number in this Function space. Reset value: Function1 Video2 : 1h Function2 Video3 : 2h Function3 Video4 : 3h	1h/2h/3h
3-0	Reserved	RO		0h

0x058 – SUBSYSTEM ID

Bit	Function	Type	Description	Reset
31-16	Subsystem ID	RO	These bits show Subsystem ID value in PCI Configuration Space Registers.	6811h/ 6812h/ 6813h
15-0	Subsystem Vendor ID	RO	These bits show Subsystem Vendor ID value in PCI Configuration Space Registers.	1797h

0x078 – M66EN

Bit	Function	R/W	Description	Reset
1	M66EN	RO	M66EN pin status. 0:33MHz PCI Bus is connected to TW6816. 1:66MHz PCI Bus is connected to TW6816.	X
0	Reserved	RO		0

0x204 – Decoder Status Register 1 (STATUS1)

Bit	Function	R/W	Description	Reset
7	VDLOSS	RO	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
6	HLOCK	RO	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	RO	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	RO	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	RO	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	NOVIDEO	RO	1=No Video 0=Video	0
1	MONO	RO	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	RO	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x208 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7	Reserved	RO		0
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.(special purpose only)	1
5-4	IFSEL	R/W	00 = Composite video decoding	0h
3-2	YSEL	R/W	These two bits control the input video selection. 00 = VINnA selected 01 = VINnB selected 10 = VINnC selected 11 = VINnD selected Function1 Video2 : n=2 Function2 Video3 : n=3 Function3 Video4 : n=4	0h
1-0	Reserved	RO		0h

0x210 – GAMMA and HSYNC Delay Control

Bit	Function	R/W	Description	Reset
7	GMEN	R/W	Reserved	0
6-5	CKHY	R/W	Color killer sensitivity. Lower value gives higher sensitivity.	0h
4-0	HSDLY	R/W	Reserved.	0h

0x218 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	SRESET	WO	A 1 written to this bit resets the device to its default state but all register content remain unchanged. This bit is self-resetting.	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference 2.	0
5	VREF	R/W	1 = Internal voltage reference. 0 = external voltage reference using VCOM, VREFP and VREFN.	0
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = System clock in power down mode.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1-0	Reserved	RO	Reserved for future use	0

0x21C – Cropping Register High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	0
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0x220 – Vertical Delay Register Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12h

0x224 – Vertical Active Register Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0h

0x228 – Horizontal Delay Register Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	10h

0x22C – Horizontal Active Register Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0h

0x230 – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Reserved	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC 0 = Notch filter	1
2	HCOMP	R/W	1 = operation mode 1. (recommended) 0 = mode 0.	1
1	YCOMB	R/W	This bit controls the Y comb. 1 = Y output is the averaging of two adjacent lines. 0 = No comb.	0
0	PDLY	R/W	PAL delay line. 1 = enabled. 0 = disabled.	1

0x234 – Vertical Scaling Register, Low (VSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	VSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register	00h

0x238 – Scaling Register High (SCALE_HI)

Bit	Function	R/W	Description	Reset
7-4	VSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register.	1
3-0	HSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register.	1

0x23C – Horizontal Scaling Register Low (HSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	HSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register.	00h

0x240 – BRIGHTNESS Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00h

0x244 – CONTRAST Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	CONTRAST	R/W	These bits control the luminance contrast gain.A value of 100(64h) has a gain of 1.The range od adjustment is from 0% to 255% at 1% per step.	64h

0x248 – SHARPNESS Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the center frequency of peaking filter.The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	1
5-4	CTI	R/W	CTI level selection. 0 = none. 3 = highest.	1h
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest.	1h

0x24C – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80h

0x250 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80h

0x254 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from $+36^{o}$ (7Fh) to -36^{o} (80h) with an increment of 0.28^{o}. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0^{o} (00h). This is effective only on NTSC system.	00h

0x25C – Vertical Sharpness (VSHARP)

Bit	Function	R/W	Description	Reset
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	8h
3	Reserved	RO	Reserved	0
2-0	VSHP	R/W	Vertical peaking level. 0 = none. 7 = highest.	0

0x260 – Coring Control Register (CORING)

Bit	Function	R/W	Description	Reset
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0x268 – Analog Control II

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		0
3	YFLEN	R/W	Y-Ch anti-alias filter control 1 = enable 0 = disable	0
2	YSV	R/W	Y-Ch power saving mode 1 = enable 0 = disable	0
1-0	Reserved	R/W		0

0x270 – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	RO	0 = Idle 1 = detection in progress	0
6-4	STDNOW	RO	Current standard invoked 0 = NTSC (M) 1 = PAL (B, D, G, H, I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC (M) 1 = PAL (B, D, G, H, I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0x274 – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B, D, G, H, I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0x278 – NT50

Bit	Function	R/W	Description	Reset
7	NT50	R/W	1 = Force decoding format to 50Hz NTSC. 0 = decoding format is set by register 0x270 (SDT)	0
6-0	Reserved	R/W		08h

0x280 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping time is determined by this together with CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0

0x284 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN8	R/W	This bit is the MSB of the 9-bit register that controls the AGC gain when AGC loop is disabled.	0

0x288 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0

0x28C – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. Setting 'FF' can disable this function.	D8

0x290– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	0
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3Ch

0x294– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	0
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38h

0x298 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits determine the VCR detection sensitivity.	4

0x29C – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	28h

0x2A0 – Vertical Control I (VCNTL1)

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = long 0 = normal	0

0x2A4 – Vertical Control II (VCNTL2)

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control for test.	0
5-0	VSHT	R/W	Vsync output delay control in the increment of half line length.	00

0x2A8 – Color Killer Level Control (CKILL)

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	28

0x2AC – Comb Filter Control (COMB)

Bit	Function	R/W	Description	Reset
7-4	HTL	R/W	Adaptive Comb filter control.	4
3-0	VTL	R/W	Adaptive Comb filter combing strength control. Higher value provides stronger comb filtering.	4

0x2B0 – Luma Delay and H Filter Control (LDLY)

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	HFLT	R/W	If HSCALE[11-8]=1,HFLT [3:0] controls the peaking function. If HSCALE[11-8]>1,HFLT [2:0] function is bellow. Pre-filter selection for horizontal scaler 1** = Bypass 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image 010 = Recommended for QCIF size image 011 = Recommended for ICON size image	0

0x2B4 – Miscellaneous Control I (MISC1)

Bit	Function	R/W	Description	Reset
7	HPLC	R/W	Reserved for future use.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
5	PALC	R/W	Reserved for future use.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	Reserved	RO		0
2	BYPASS	R/W	Reserved for future use.	1
1-0	Reserved	RO		0

0x2B8 – LOOP Control Register (LOOP)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Slow	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0x2BC – Miscellaneous Control II (MISC2)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0x2C0 – Macrovision Detection (MVSN)

Bit	Function	R/W	Description	Reset
7	SF	RO	Reserved	0
6	PF	RO	Reserved	0
5	FF	RO	Reserved	0
4	KF	RO	Reserved	0
3	CSBAD	RO	1 = Macrovision color stripe detection may be un-reliable	0
2	MCVSN	RO	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	RO	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	RO	This bit is valid only when color stripe protection is detected, i.e. Cstripe=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0x2C4 – Decoder Chip STATUS II (STATUS2)

Bit	Function	R/W	Description	Reset
7	VCR	RO	1 = VCR signal	0
6	WKAIR	RO	1 = Weak signal	0
5	WKAIR1	RO	Weak signal indicator 2	0
4	VSTD	RO	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	RO	1 = Non-interlaced signal 0 = interlaced signal	0
2-0	Reserved	RO		0

0x2C8 – H monitor (HFREF)

Bit	Function	R/W	Description	Reset
7-0	HFREF	RO	Horizontal line frequency indicator(Test purpose only).	X

0x2CC – CLAMP MODE (CLMD)

Bit	Function	R/W	Description	Reset
7-6	FRM	R/W	Free run mode control 0 = Auto 2 = default to 60Hz 3 = default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None 1 = smallest 2 = small 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = low 1 = medium 2 = high	1

0x2D0 – ID Detection Control (IDCNTL)

Bit	Function	R/W	Description	Reset
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1E / 18 / 1C / 2A

0x2D4 – Clamp Control I (CLCNTL1)

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control for debugging use.	0
6	YCLEN	R/W	1 = Y channel clamp disabled 0 = Enabled.	0
5-4	Reserved	R/W		0
3	GTEST	R/W	1 = Test. 0 = Normal operation.	0
2	VLPF	R/W	Sync filter BW control. 0 = Normal	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0x3DC – Field2 Cropping High (F2CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	V2DELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Field2 Vertical Delay register.	0h
5-4	V2ACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit Field2 VACTIVE register. Refer to description on Reg09 for its shadow register.	0h
3-2	H2DELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Field2 Horizontal Delay register.	0h
1-0	H2ACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit Field2 HACTIVE register.	2h

0x3E0 – Field2 Vertical Delay Low (F2VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	V2DELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Field2 Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12h

0x3E4 – Field2 Vertical Active Low (F2VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	V2ACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Field2 Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0h

0x3E8 – Field2 Horizontal Delay Low (F2HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	H2DELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Field2 Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0Fh

0x3EC – Field2 Horizontal Active Low (F2HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	H2ACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Field2 Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0h

0x3F0 – Field2 Control (F2CNT)

Bit	Function	R/W	Description	Reset
0	F2CNT	R/W	1:Field2 Video Capture Controlled by V2DELAY, V2ACTIVE, H2DELAY, and H2ACTIVE, V2SCALE, H2SCALE field2 registers. 0:Field2 Video Capture Controlled by VDELAY, VACTIVE, HDELAY, HACTIVE, VSCALE, HSCALE registers.	0

0x3F4 – Field2 Vertical Scaling Low (F2VSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	V2SCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit Field2 vertical scaling ratio register	00h

0x3F8 – Field2 Scaling High (F2SCALE_HI)

Bit	Function	R/W	Description	Reset
7-4	V2SCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit Field2 vertical scaling ratio register.	1h
3-0	H2SCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit Field2 horizontal scaling ratio register.	1h

0x3FC – Field2 Horizontal Scaling Low (F2HSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	H2SCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit Field2 horizontal scaling ratio register.	00h

PCI Configuration Space Registers for Audio

0x00 – Vendor ID and Device ID

Bit	Function	R/W	Description	Reset
31-16	Device ID	RO	Device ID Function 4 audio 1 : 6814h Function 5 audio 2 : 6815h Function 6 audio 3 : 6816h Function 7 audio 4 : 6817h	6814h/ 6815h/ 6816h/ 6817h
15-0	Vendor ID	RO	Techwell Inc PCI vendor ID	1797h

0x04 – Command and Status Register

Bit	Function	R/W	Description	Reset
31,30	Reserved	RO	These bits are hardwired to 0.	0
29	Received Master Abort	RR	Set when master transaction is terminated with Master Abort.	0
28	Received Target Abort	RR	Set when master transaction is terminated with Target Abort.	0
27	Reserved	RO	This bit is hardwired to 0.	0
26,25	Address Decode Time	RO	Responds with medium DEVSEL timing.	01b
24-22	Reserved	RO	These bits are hardwired to 0.	0
21	66MHz CAPABLE	RO	This bit is hardwired to 1.	1
20	New Capabilities	RO	A value of 1 indicates that the value read at PCI configuration offset is a pointer in configuration space to a linked list of new capabilities.	1
19-16	Reserved	RO	These bits are hardwired to 0.	0
15-10	Reserved	RO	These bits are hardwired to 0.	0
9	Fast Back-to-Back Enable	R/W	This bit should be set to 1 normally.	0
8	SERR# Enable	R/W	This bit should be set to 0 normally.	0
7	Stepping Control	RO	This bit is hardwired to 0.	0
6	Parity Error Response	R/W	This bit should be set to 0 normally.	0
5	VGA Palette Snoop	RO	This bit is hardwired to 0.	0
4	Memory Write and Invalidate Enable	R/W	This bit should be set to 1 normally.	0
3	Special Cycles	R/W	This bit must be set to 0.	0
2	Bus Master	R/W	A value of 1 enables this function space to act as a bus initiator.	0

1	Memory Space	R/W	A value of 1 enables response to memory space accesses (target decoded to memory mapped registers).	0
0	IO Space	RO	This bit is always "0".	0

0x08 – Revision ID and Class Code

Bit	Function	R/W	Description	Reset
31-8	Class code	RO	This function space is a multimedia other device	048000h
7-0	Revision ID	RO	revision number	10h

0x0C – Cache Line Size

Bit	Function	R/W	Description	Reset
7-0	Cache Line Size	R/W	This read/write register specifies the system cacheline size in units of DWORDs. These bits should be set to 0 normally.	08h

0x0D – Latency Timer

Bit	Function	R/W	Description	Reset
15-8	Latency Timer	R/W	The number of PCI bus clocks for the latency timer used by the bus master. Once the latency expires, the master must initiate transaction termination as soon as GNT is removed.	40h

0x0E – Header Type

Bit	Function	R/W	Description	Reset
23-16	Header Type	RO	This chip is Multi-function PCI device	80h

0x10 – Base Address 0

Bit	Function	R/W	Description	Reset
31-7	Relocatable Memory Pointer	R/W	Determine the location of the registers in the 32-bit addressable memory space.	Assigned by system at boot time
6-0	Memory Usage Specification	RO	Reserve 128bytes of memory-mapped address space for local registers. Address space is prefetchable without side effects.	00h

0x2C – Subsystem ID and Subsystem Vendor ID

Bit	Function	R/W	Description	Reset
31-16	Subsystem ID	RO	Function 4 audio 1 : 6814h Function 5 audio 2 : 6815h Function 6 audio 3 : 6816h Function 7 audio 4 : 6817h	6814h/ 6815h/ 6816h/ 6817h
15-0	Subsystem Vendor ID	R/W	Vendor specific.	1797h

0x34 – Capabilities Pointer

Bit	Function	R/W	Description	Reset
7-0	Cap_Ptr	RO	DWORD aligned byte address offset in configuration space to the first item in the list of capabilities.	44h

0x3C – Interrupt Line, Interrupt Pin, Min_Gnt, Max_Lat

Bit	Function	R/W	Description	Reset
31-24	Max_Lat	RO	Require bus access every 18us, at a minimum, in units of 250ns. Affects the desired settings for the latency timer value.	48h
23-16	Min_Gnt	RO	Desire a minimum grant burst period of 8us to empty data FIFO, in units of 250ns. Affects the desired settings for the latency timer value.	20h
15-8	Interrupt Pin	RO	Chip interrupt pin is connected to INTA, the only one usable by a single function device.	01h
7-0	Interrupt Line	R/W	The Interrupt Line register communicates interrupt line routing Information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the chip interrupt pin is connected. Device driver can use this value to determine interrupt priority and vector information.	System Assigned

0x44 – Power Management Capabilities

Bit	Function	R/W	Description	Reset
31-27	PME_Support	RO	The function does not capable of asserting the PME# signal.	00h
26	D2_Support	RO	The function does not support D2 state.	0b
25	D1_Support	RO	The function does not support D1 state.	0b
24-22	Aux_Current	RO	The function does not support PME# generation from $D3_{cold}$.	000b
21	DSI	RO	The function requires a device specific initialization sequence following transition to the D0 uninitialized state.	1b
20	Reserved	RO		0b
19	PME_Clk	RO	No PCI clock is requires for the function to generate PME#.	0b
18-16	Version	RO	This function complies with Reversion 1.1 of PCI Power Management Interface Specification.	010b
15-8	Next_Item_Ptr	RO	Pointer to next item in the function's capability list. A value of 0 indicates there is no additional item.	00h
7-0	Cap_ID	RO	PCI power management capability ID.	01h

0x48 – Power Management Control/Status

Bit	Function	R/W	Description	Reset
31-24	Data	RO	The function does not support Data register.	00h
23-16	PMCSR_BSE	RO	The function does not support Bridge Support Extensions.	00h
15	PME_Status	RO	The function does not support PME# generation from $D3_{cold}$.	0b
14-13	Data_Scale	RO	The function does not support Data register.	00b
12-9	Data_Select	RO	The function does not support Data register.	0h
8	PME_En	RO	The function does not support PME# generation from $D3_{cold}$.	0b
7-2	Reserved	RO		00h
1-0	PowerState	R/W	This field is to determine the current power state of a function and to set the function into a new power state. 00 = D0 01 = D1 10 = D2 11 = $D3_{hot}$	00b

PCI Memory Space Registers for Audio

Function 4 Audio 1 Memory Register Summary

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
000	Reserved						AFIFOEN	ADMAPEN	00
001	Reserved								00
002	Reserved								00
003	Reserved								00
004	ADMAP_SA[7:0]								00
005	ADMAP_SA[15:8]								00
006	ADMAP_SA[23:16]								00
007	ADMAP_SA[31:24]								00
008	ADMAP_EXE[7:0]								00
009	ADMAP_EXE[15:8]								00
00A	ADMAP_EXE[23:16]								00
00B	ADMAP_EXE[31:24]								00
00C	ADMAP_PP[7:0]								00
00D	ADMAP_PP[15:8]								00
00E	ADMAP_PP[23:16]								00
00F	ADMAP_PP[31:24]								00
010	Reserved			AMUTE	DA_LMT	Reserved			00
011	AGAIN								00
012	Reserved		SIGN	Reserved					20
013	Reserved								00
014	ALENGTH[7:0]								00
015	ALENGTH[15:8]								00
016	ALINE[7:0]								00
017	ALINE[15:8]								0
018	AMODE				Reserved	ADUMMY EN	Reserved		00
019	Reserved	ACKGVMODE		ADMATRIG					10
01A	Reserved								00
01B	Reserved								00
01C	Reserved	APABORT	ADMAPER R	Reserved	AFFOF	Reserved	ADMAPI	Reserved	00
01D	Reserved	APPERR	DETAUDI O	LOSTAUDI O	AIRQC				00
01E	Reserved								00
01F	Reserved								00
020	AINTMASK[7:0]								00
021	Reserved	AINTMASK[14:8]							00
022	Reserved								00
023	Reserved								00
024	Reserved	AIGAIN							20
025	Reserved								00
026	Reserved								00
027	Reserved								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
028	AADCOFS[7:0]								00
029							AADCOFS[9:8]		00
02A	Reserved								00
02B	Reserved								00
02C	ADJAADC[7:0]								00
02D	Reserved						AADJAADC[9:8]		00
02E	AUDADC[7:0]								00
02F							AUDADC[9:8]		00
030	Reserved							ARST	00
031	Reserved								00
032	Reserved								00
033	Reserved								00
034	PACLKREF6816[7:0]								34
035	PACLKREF6816[15:8]								E3
036	PACLKREF6816[23:0]								0F
037	Reserved							PACLKMD	00
038	Reserved								00
039	Reserved								00
03A	Reserved								00
03B	Reserved								00
03C	VACLKREF6816[7:0]								07
03D	VACLKREF6816[15:8]								6B
03E	VACLKREF6816[23:16]								13
03F	Reserved								00
040	Reserved					ACLKSEL			00
041	Reserved								00
042	Reserved								00
043	Reserved								00
044	VDLOSS1	HLOCK1	SLOCK1	FIELD1	VLOCK1	NOVIDEO 1	MONO1	DET501	XX
045	VDLOSS2	HLOCK2	SLOCK2	FIELD2	VLOCK2	NOVIDEO 2	MONO2	DET502	XX
046	VDLOSS3	HLOCK3	SLOCK3	FIELD3	VLOCK3	NOVIDEO 3	MONO3	DET503	XX
047	VDLOSS4	HLOCK4	SLOCK4	FIELD4	VLOCK4	NOVIDEO 4	MONO4	DET504	XX
048 - 04B	Reserved								00
04C	Reserved				DET_AUDIO4	DET_AUDIO3	DET_AUDIO2	DET_AUDIO1	00
04D	Reserved								00
04E	Reserved								00
04F	Reserved								00
050 - 057	Reserved								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
058	Reserved	FUNC			Reserved				40
059	Revision ID								10
05A	Device ID[7:0]								14
05B	Device ID[15:8]								68
05C	Subsystem Vendor ID[7:0]								97
05D	Subsystem Vendor ID[15:8]								17
05E	Subsystem ID[7:0]								14
05F	Subsystem ID[15:8]								68
060	Reserved								00
061	Reserved		AADCCKPOL	Reserved				ADMAERRPASS	01
062	Reserved								00
063	Reserved								00
064	Reserved								30
065	Reserved			ADROPVALUE					1F
066	Reserved								00
067	Reserved								00
068	ACKI[7:0]								07
069	ACKI[15:8]								6B
06A	Reserved		ACKI[21:16]						13
06B	Reserved								00
06C	ACKN[7:0]								78
06D	ACKN[15:8]								85
06E	Reserved						ACKN[17:16]		00
06F	Reserved								00
070	APZ	APG			Reserved	ACPL	SRPH	LRPH	C4
071	VRSTSEL	LRDIV							20
072	Reserved	SDIV							00
073	Reserved								00
074	Reserved	AUTOMUTE	AAMPMD	ADET_TH1					23
075	Reserved					ADET_FLT			07
076	Reserved								00
077	Reserved								00
078	Reserved			ADET_IND	Reserved			M66EN	1X
079	Reserved			ADET_TH2					03
07A	Reserved			ADET_TH3					03
07B	Reserved			ADET_TH4					03
07C	Reserved				AADCPWDN	ABP	AHPF_RES	ASAVE	00
07D	Reserved								00
07E	Reserved								00
07F	Reserved								00

Function 4 Audio 1 Memory Register Description

0x000 – ADMAC

Bit	Function	R/W	Description	Reset
31-2	Reserved	RO		0h
1	AFIFO_EN	R/W	Set to 1 to enable the Audio FIFO, 0 to flush the Audio FIFO.	0
0	ADMAP_EN	R/W	A value of 1 enables the Audio DMA Programmer to process DMAP program starting from ADMAP_SA.	0

0x004– ADMAP_SA

Bit	Function	R/W	Description	Reset
31-0	ADMAP_SA	R/W	The starting address of AUDIO DMAP in the memory address space.	00000000h

0x008 – ADMAP_EXE

Bit	Function	R/W	Description	Reset
31-0	ADMAP_EXE	RO	The dword of DMAP instruction packet that the AUDIO DMA Programmer is currently executing.	00000000h

0x00C – ADMAP_PP

Bit	Function	R/W	Description	Reset
31-0	ADMAP_PP	RO	The memory address of the last dword of AUDIO DMAP in memory address space fetched by the DMA Programmer.	00000000h

0x010 – Audio Control1 (ACTL1)

Bit	Function	R/W	Description	Reset
31-22	Reserved	RO		000h
21	SIGN	R/W	0:Unsigned 8 Bit PCM Data for 8Bit WAV File. This bit must be 0 to make 8 Bit WAV File for special application. 1:signed. Most application need only signed data mode.	1
20-16	Reserved	RO		00
15-8	AGAIN	R/W	Audio data Gain control by this register values. bit7-4: integer, bit3-0: fraction If AGAIN=0x00,Data just pass through without any again. If AGAIN=0x10,only Input Data 0x000 change into 0x001.	00H
7-5	Reserved	RO		0
4	AMUTE	R/W	1: Mute Audio data,0:no mute(normal audio)	0
3	DA_LMT	R/W	Enables detection of Audio data 0x8000(0x80) and replacement with 0x8001(0x81). Replace format determined by AMODE.1=Enable, 0=Disable. AMODE=00:0x80 > 0x81 AMODE=01:0x8000 > 0x8001	0
2-0	Reserved	RO		0

0x014 – AUDIO PACKET (APACKET)

Bit	Function	R/W	Description	Reset
31-16	ALINE	R/W	Number of audio lines (test purpose only)	0000h
15-0	ALENGTH	R/W	Number of bytes in Audio Line (test purpose only)	0000h

0x018 – Audio Control2 (ACTL2)

Bit	Function	R/W	Description	Reset
15	Reserved	RO		0
14-13	ACKGVMODE	R/W	ACKG (AUDIO Clock Generation) block frame mode. 00b:Video Field lock Audio clock generation. 01b:Video Frame lock Audio clock generation. 10b:no video lock generation.	00b
12-8	ADMATRIG	R/W	AUDIO FIFO DMA Timing control. No need to change on normal operation.	10h
7-4	AMODE	R/W	Audio function mode. 0h: 8bit mono sample from internal ADC. 1h: 16bit mono sample from internal ADC.	0h
3	Reserved	RO		0
2	ADUMMYEN	R/W	1:AUDIO FIFO Output is DUMMY data. (test purpose only) 0:AUDIO FIFO is output normal.	0
1-0	Reserved	RO		0

0x01C – Audio Interrupt Status (AINTSTAT)

Bit	Function	R/W	Description	Reset
31-15	Reserved	RO		0
14	PPERR	RR	Set if a parity error is detected on PCI bus.	0
13	DETAUDIO	RR	Set if audio is detected in AIN1 input.	0
12	LOSTAUDIO	RR	Set if audio is lost in AIN1 input.	0
11-8	AIRQC	RO	AUDIO IRQC Counter Value (Reserved).	0h
7	Reserved	RO		0
6	PABORT	RR	Set if Chip is a PCI bus master and receives master or target abort.	0
5	ADMAPERR	RR	Set if ADMA Programmer detects any error occurs on ADMAP program.	0
4	Reserved	RO		0
3	AFOVFI	RR	Audio FIFO overflowed.	0
2	Reserved	RO		0
1	ADMAPI	RR	When the IRQ bit in the ADMAP instruction packet is set, this bit is set after ADMA Programmer completes the Audio data instruction.	0
0	Reserved	RO		0

0x020 – Audio Interrupt Mask (AINTMASK)

Bit	Function	R/W	Description	Reset
31-15	Reserved	RO		0h
14-0	AINTMASK	R/W	Writing a 1 to AINTMASK[n] enables the interrupt bit AINTSTAT[n].	00h

0x024 – AIGAIN

Bit	Function	R/W	Description	Reset
7	Reserved	RO		0
6-0	AIGAIN	R/W	Analog Audio input gain control.0x20 is gain 1.128 steps control.	20h

0x024 – Audio ADC Digital Input Offset control

Bit	Function	R/W	Description	Reset
31-10	Reserved	RO		000000h
9-0	AADCOFS	R/W	Digital ADC input data offset control.Audio ADC data to be input to Digital process portion is adjusted by ADJAADC = AUDADC + AADCOFS AUDADC is 2's formatted Analog Audio ADC output. AAADCOFS is adjusted offset value by 2's format.	000h

0x02C – Adjusted Audio ADC data value

Bit	Function	R/W	Description	Reset
31-26	Reserved	RO		00h
25-16	AUDADC	RO	Current Audio ADC output data value	XXX
15-10	Reserved	RO		00h
9-0	ADJAADC	RO	Adjusted Audio ADC data value by AADCOFS.	XXX

0x030 – Audio Reset (ARSTN)

Bit	Function	R/W	Description	Reset
0	ARSTN	R/W	Write 1 is enable Audio Logic function,0:resetting.	0

0x034 – PALKREF6816

Bit	Function	R/W	Description	Reset
31-25	Reserved	RO		00h
24	PACLKMD	R/W	1: Only PACLKREF6816 controls apclk clock. When 66MHz PCI clock is connected, PACLKREF6816 need to be setup to half value of 33MHz PCI clock mode. 0: Internal PACLKREF6816 is automatically set up by M66EN input status. M66EN=1 : Internal PACLKREF6816 = PACLKREF6816 / 2 M66EN=0: Internal PACLKREF6816 = PACLKREG6816.	0
23-0	PACLKREF6816	R/W	Audio clock generation reference from PCI clock 33MHz.Internal audio clock apclk is generated by following equation. apclkFreq=256xFs. PACLKREF = 2^24 x apclkFreq / PCIClockFreq.	0FE334h

0x03C – VACLKREF6816

Bit	Function	R/W	Description	Reset
23-0	VACLKREF6816	R/W	Audio clock generation reference from Video clock XTI. Following equation generates internal audio clock avclk.avclkFreq=256xFs VACLKREF = 2^24 x avclkFreq / PCIClockFreq.	136B07h

0x040 – Audio Clock Selection

Bit	Function	R/W	Description	Reset
7-3	Reserved	RO		00h
2-0	ACLKSEL	R/W	Audio system clock select 0h:apclk(recommended for most PCI Bus connection) 1h:avclk. 2h:ackg block amclk 4h:ackg block asclk.	0h

0x044 – Video Decoder Status(VIN4 input video)

Bit	Function	R/W	Description	Reset
31	VDLOSS4	RO	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
30	HLOCK4	RO	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
29	SLOCK4	RO	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
28	FIELD4	RO	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
27	VLOCK4	RO	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
26	NOVIDEO4	RO	1= No Video 0= Video	0
25	MONO4	RO	1 = No color burst signal detected. 0 = Color burst signal detected.	0
24	DET504	RO	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x044 – Video Decoder Status(VIN3 input video)

Bit	Function	R/W	Description	Reset
23	VDLOSS3	RO	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
22	HLOCK3	RO	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
21	SLOCK3	RO	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
20	FIELD3	RO	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
19	VLOCK3	RO	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
18	NOVIDEO3	RO	1= No Video 0= Video	0
17	MONO3	RO	1 = No color burst signal detected. 0 = Color burst signal detected.	0
16	DET503	RO	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x044 –Video Decoder Status(VIN2 input video)

Bit	Function	R/W	Description	Reset
15	VDLOSS2	RO	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
14	HLOCK2	RO	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
13	SLOCK2	RO	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
12	FIELD2	RO	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
11	VLOCK2	RO	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
10	NOVIDEO2	RO	1= No Video 0= Video	0
9	MONO2	RO	1 = No color burst signal detected. 0 = Color burst signal detected.	0
8	DET502	RO	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x044 – Video Decoder Status(VIN1 input video)

Bit	Function	R/W	Description	Reset
7	VDLOSS1	RO	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
6	HLOCK1	RO	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK1	RO	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD1	RO	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK1	RO	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	NOVIDEO1	RO	1= No Video 0= Video	0
1	MONO1	RO	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET501	RO	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x04C – Audio Detection Status

Bit	Function	R/W	Description	Reset
7-4	Reserved	RO		0
3	DET_AUDIO4	RO	1: Audio detected in AIN4 input. 0: not detected.	0
2	DET_AUDIO3	RO	1: Audio detected in AIN3 input. 0: not detected.	0
1	DET_AUDIO2	RO	1: Audio detected in AIN2 input. 0: not detected.	0
0	DET_AUDIO1	RO	1: Audio detected in AIN1 input. 0: not detected.	0

0x058 – DEVICE ID

Bit	Function	R/W	Description	Reset
31-16	Device ID	RO	These bits show Device ID value in PCI configuration space.	6814h
15-8	Revision ID	RO	These bits show Revision ID value in PCI configuration spae.	10h
7	Reserved	RO		0
6-4	FUNC	RO	These bits show Function number in this function space.	4h
3-0	Reserved	RO		0

0x05C – SUBSYSTEM

Bit	Function	R/W	Description	Reset
31-16	Subsystem ID	RO	These bits show Subsystem ID value in this PCI configuration space.	6814h
15-0	Subsystem Vendor ID	RO	These bits show Subsystem Vendor ID value in this PCI configuration space.	1797h

0x060 – ADMAERRPASS

Bit	Function	R/W	Description	Reset
31-14	Reserved	RO		00000h
13	AADCCKPOL	R/W	1: Audio ADC clock input is polarity inversed. 0: not inversed.	0
12-1	Reserved	RO		000
0	ADMAERRPASS	R/W	1: Ignore error DMAP command data when those are received in audio DMA logic. 0: Generate admaperr interrupt when error DMAP command data are received.	1

0x064 – ADROPVALUE

Bit	Function	R/W	Description	Reset
31-13	Reserved	RO		00000h
12-8	ADROPVALUE	R/W	Audio data dropping threshold value. Audio data dropping are happening when audio FIFO has 32bit word data more than this value.	1Fh
7-0	Reserved	RO		00

0x068 – Audio Clock Increment (ACKI)

Bit	Function	R/W	Description	Reset
21-0	ACKI	R/W	ACKI	013B07h

0x06C – Audio Clock Number (ACKN)

Bit	Function	R/W	Description	Reset
17-0	ACKN	R/W	Audio clock number per field	08578h

0x070 – Audio ACKG Control

Bit	Function	R/W	Description	Reset
31-22	Reserved	RO		0
21-16	SDIV	R/W	Serial Clock divider	0Fh
15-14	VRSTSEL	R/W	Select vrst(V reset) signal on ackg(Audio Clock Generator) refin input when ACPL=0(Loop closed) 0 : VIN1 video decoder vrst 1 : VIN2 video decoder vrst 2 : VIN3 video decoder vrst 3 : VIN4 video decoder vrst	0
13-8	LRDIV	R/W	Left/Right Clock divider	20h
7	APZ	R/W	Loop control	1
6-4	APG	R/W	Loop control	4h
3	Reserved	RO		0
2	ACPL	R/W	0 = Loop closed 1 = Loop open	1
1	SRPH	R/W	ASCLK divider trigger phase	0
0	LRPH	R/W	ALRCLK divider trigger phase	0

0x074 – Audio Detection

Bit	Function	R/W	Description	Reset
10-8	ADET_FLT	R/W	Select the filter for audio detection. 0:Wide LPF(default),7:Narrow LPF	7
7	Reserved	RO		0
6	AUTOMUTE	R/W	1:Enable output mute audio data when audio is not detected. 0: Disable	0
5	AAMPMD	R/W	0:Detect audio if absolute amplitude is greater than threshold 1:Detect audio if differential amplitude is greater than threshold.	0
4-0	ADET_TH1	R/W	Define the threshold value for AIN1 audio detection. 0:Low value,31:High value	0

0x078 – Audio Detection Threshold

Bit	Function	R/W	Description	Reset
31-29	Reserved	RO		00
28-24	ADET_TH4	R/W	Define the threshold value for AIN4 audio detection. 0:Low value,31:High value	03
22-21	Reserved	RO		0
20-16	ADET_TH3	R/W	Define the threshold value for AIN3 audio detection. 0:Low value,31:High value	03
15-13	Reserved	RO		0
12-8	ADET_TH2	R/W	Define the threshold value for AIN2 audio detection. 0:Low value,31:High value	03
7-5	Reserved	RO		0
4	AET_IND	R/W	1: ADET_TH1,ADETTH_2,ADET_TH3,ADET_TH4 control audio detection in each audio input process. 0: ADET_TH1 value control all audio detetion in all audio input process.	1
3-2	Reserved	RO		0
0	M66EN	RO	M66EN pin status. 0:33MHz PCI Bus is connected to TW6816. 1:66MHz PCI Bus is connected to TW6816.	X

0x07C – Audio ADC control

Bit	Function	R/W	Description	Reset
31-4	Reserved	RO		00000 00h
3	AADCPWDN	RW	1: Audio ADC power down. 0: Audio ADC normal mode.	0
2	ABP	R/W	Input buffer bypass. 0 : normal 1:input buffer bypass test mode.	0
1	AHPF_RES	RW	High pass filter resistance control 0 : normal 1 : test mode	0
0	ASAVE	RW	1:Audio ADC saving mode. 0: Audio ADC normal function mode.	0

Function 5/6/7 Audio 2/3/4 Memory Register Summary

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
000	Reserved						AFIFOEN	ADMAPEN	00
001	Reserved								00
002	Reserved								00
003	Reserved								00
004	ADMAP_SA[7:0]								00
005	ADMAP_SA[15:8]								00
006	ADMAP_SA[23:16]								00
007	ADMAP_SA[31:24]								00
008	ADMAP_EXE[7:0]								00
009	ADMAP_EXE[15:8]								00
00A	ADMAP_EXE[23:16]								00
00B	ADMAP_EXE[31:24]								00
00C	ADMAP_PP[7:0]								00
00D	ADMAP_PP[15:8]								00
00E	ADMAP_PP[23:16]								00
00F	ADMAP_PP[31:24]								00
010	Reserved			AMUTE	DA_LMT	Reserved			00
011	AGAIN								00
012	Reserved		SIGN	Reserved					20
013	Reserved								00
014	ALENGTH[7:0]								00
015	ALENGTH[15:8]								00
016	ALINE[7:0]								00
017	ALINE[15:8]								0
018	AMODE				Reserved	ADUMMY EN	Reserved		00
019	Reserved			ADMATRIG					10
01A	Reserved								00
01B	Reserved								00
01C	Reserved	APABORT	ADMAPERR	Reserved	AFFOF	Reserved	ADMAPI	Reserved	00
01D	Reserved	APPERR	DETAUDIO	LOSTAUDIO	AIRQC				00
01E	Reserved								00
01F	Reserved								00
020	AINTMASK[7:0]								00
021	Reserved	AINTMASK[14:8]							00
022	Reserved								00
023	Reserved								00
024	Reserved	AIGAIN							20
025	Reserved								00
026	Reserved								00
027	Reserved								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
028	AADCOFS[7:0]								00
029							AADCOFS[9:8]		00
02A	Reserved								00
02B	Reserved								00
02C	ADJAADC[7:0]								00
02D	Reserved						AADJAADC[9:8]		00
02E	AUDADC[7:0]								00
02F							AUDADC[9:8]		00
030	Reserved							ARST	00
031	Reserved								00
032	Reserved								00
033	Reserved								00
034 - 043	Reserved								00
044	VDLOSS1	HLOCK1	SLOCK1	FIELD1	VLOCK1	NOVIDEO 1	MONO1	DET501	XX
045	VDLOSS2	HLOCK2	SLOCK2	FIELD2	VLOCK2	NOVIDEO 2	MONO2	DET502	XX
046	VDLOSS3	HLOCK3	SLOCK3	FIELD3	VLOCK3	NOVIDEO 3	MONO3	DET503	XX
047	VDLOSS4	HLOCK4	SLOCK4	FIELD4	VLOCK4	NOVIDEO 4	MONO4	DET504	XX
048 - 04B	Reserved								00
04C	Reserved				DET_AUDIO4	DET_AUDIO3	DET_AUDIO2	DET_AUDIO1	00
04D	Reserved								00
04E	Reserved								00
04F	Reserved								00
050 - 057	Reserved								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
058	Reserved	FUNC			Reserved				50/60/70
059	Revision ID								10
05A	Device ID[7:0]								15/16/17
05B	Device ID[15:8]								68
05C	Subsystem Vendor ID[7:0]								97
05D	Subsystem Vendor ID[15:8]								17
05E	Subsystem ID[7:0]								15/16/17
05F	Subsystem ID[15:8]								68
060	Reserved								00
061	Reserved							ADMAERR PASS	01
062	Reserved								00
063	Reserved								00
064	Reserved								30
065	Reserved			ADROPVALUE					1F
066	Reserved								00
067	Reserved								00
068 - 077	Reserved								00
078	Reserved							M66EN	0X
079	Reserved								00
07A	Reserved								00
07B	Reserved								00
07C - 07F	Reserved								00

Function 5/6/7 Audio 2/3/4 Memory Register Description

0x000 – ADMAC

Bit	Function	R/W	Description	Reset
31-2	Reserved	RO		0h
1	AFIFO_EN	R/W	Set to 1 to enable the Audio FIFO, 0 to flush the Audio FIFO.	0
0	ADMAP_EN	R/W	A value of 1 enables the Audio DMA Programmer to process DMAP program starting from ADMAP_SA.	0

0x004– ADMAP_SA

Bit	Function	R/W	Description	Reset
31-0	ADMAP_SA	R/W	The starting address of AUDIO DMAP in the memory address space.	00000000h

0x008 – ADMAP_EXE

Bit	Function	R/W	Description	Reset
31-0	ADMAP_EXE	RO	The dword of DMAP instruction packet that the AUDIO DMA Programmer is currently executing.	00000000h

0x00C – ADMAP_PP

Bit	Function	R/W	Description	Reset
31-0	ADMAP_PP	RO	The memory address of the last dword of AUDIO DMAP in memory address space fetched by the DMA Programmer.	00000000h

0x010 – Audio Control1 (ACTL1)

Bit	Function	R/W	Description	Reset
31-22	Reserved	RO		000h
21	SIGN	R/W	0:Unsigned 8 Bit PCM Data for 8Bit WAV File. This bit must be 0 to make 8 Bit WAV File for special application. 1:signed. Most application need only signed data mode.	1
20-16	Reserved	RO		00
15-8	AGAIN	R/W	Audio data Gain control by this register values. bit7-4: integer, bit3-0: fraction If AGAIN=0x00,Data just pass through without any again. If AGAIN=0x10,only Input Data 0x000 change into 0x001.	00H
7-5	Reserved	RO		0
4	AMUTE	R/W	1: Mute Audio data,0:no mute(normal audio)	0
3	DA_LMT	R/W	Enables detection of Audio data 0x8000(0x80) and replacement with 0x8001(0x81). Replace format determined by AMODE.1=Enable, 0=Disable. AMODE=00:0x80 > 0x81 AMODE=01:0x8000 > 0x8001	0
2-0	Reserved	RO		0

0x014 – AUDIO PACKET (APACKET)

Bit	Function	R/W	Description	Reset
31-16	ALINE	R/W	Number of audio lines (test purpose only)	0000h
15-0	ALENGTH	R/W	Number of bytes in Audio Line (test purpose only)	0000h

0x018 – Audio Control2 (ACTL2)

Bit	Function	R/W	Description	Reset
15-13	Reserved	RO		0
12-8	ADMATRIG	R/W	AUDIO FIFO DMA Timing control. No need to change on normal operation.	10h
7-4	AMODE	R/W	Audio function mode. 0h: 8bit mono sample from internal ADC. 1h: 16bit mono sample from internal ADC.	0h
3	Reserved	RO		0
2	ADUMMYEN	R/W	1:AUDIO FIFO Output is DUMMY data. (test purpose only) 0:AUDIO FIFO is output normal.	0
1-0	Reserved	RO		0

0x01C – Audio Interrupt Status (AINTSTAT)

Bit	Function	R/W	Description	Reset
31-15	Reserved	RO		0
14	PPERR	RR	Set if a parity error is detected on PCI bus.	0
13	DETAUDIO	RR	Set if audio is detected in AINn input for this function space audio.	0
12	LOSTAUDIO	RR	Set if audio is lost in AINn input for this function space audio.	0
11-8	AIRQC	RO	AUDIO IRQC Counter Value (Reserved).	0h
7	Reserved	RO		0
6	PABORT	RR	Set if Chip is a PCI bus master and receives master or target abort.	0
5	ADMAPERR	RR	Set if ADMA Programmer detects any error occurs on ADMAP program.	0
4	Reserved	RO		0
3	AFOVFI	RR	Audio FIFO overflowed.	0
2	Reserved	RO		0
1	ADMAPI	RR	When the IRQ bit in the ADMAP instruction packet is set, this bit is set after ADMA Programmer completes the Audio data instruction.	0
0	Reserved	RO		0

0x020 – Audio Interrupt Mask (AINTMASK)

Bit	Function	R/W	Description	Reset
31-15	Reserved	RO		0h
14-0	AINTMASK	R/W	Writing a 1 to AINTMASK[n] enables the interrupt bit AINTSTAT[n].	00h

0x024 – AIGAIN

Bit	Function	R/W	Description	Reset
7	Reserved	RO		0
6-0	AIGAIN	R/W	Analog Audio input gain control.0x20 is gain 1.128 steps control.	20h

0x024 – Audio ADC Digital Input Offset control

Bit	Function	R/W	Description	Reset
31-10	Reserved	RO		000000h
9-0	AADCOFS	R/W	Digital ADC input data offset control.Audio ADC data to be input to Digital process portion is adjusted by ADJAADC = AUDADC + AADCOFS AUDADC is 2's formatted Analog Audio ADC output. AAADCOFS is adjusted offset value by 2's format.	000h

0x02C – Adjusted Audio ADC data value

Bit	Function	R/W	Description	Reset
31-26	Reserved	RO		00h
25-16	AUDADC	RO	Current Audio ADC output data value	XXX
15-10	Reserved	RO		00h
9-0	ADJAADC	RO	Adjusted Audio ADC data value by AADCOFS.	XXX

0x030 – Audio Reset (ARSTN)

Bit	Function	R/W	Description	Reset
0	ARSTN	R/W	Write 1 is enable Audio Logic function,0:resetting.	0

0x044 – Video Decoder Status(VIN4 input video)

Bit	Function	R/W	Description	Reset
31	VDLOSS4	RO	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
30	HLOCK4	RO	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
29	SLOCK4	RO	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
28	FIELD4	RO	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
27	VLOCK4	RO	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
26	NOVIDEO4	RO	1= No Video 0= Video	0
25	MONO4	RO	1 = No color burst signal detected. 0 = Color burst signal detected.	0
24	DET504	RO	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x044 – Video Decoder Status(VIN3 input video)

Bit	Function	R/W	Description	Reset
23	VDLOSS3	RO	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
22	HLOCK3	RO	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
21	SLOCK3	RO	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
20	FIELD3	RO	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
19	VLOCK3	RO	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
18	NOVIDEO3	RO	1= No Video 0= Video	0
17	MONO3	RO	1 = No color burst signal detected. 0 = Color burst signal detected.	0
16	DET503	RO	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x044 –Video Decoder Status(VIN2 input video)

Bit	Function	R/W	Description	Reset
15	VDLOSS2	RO	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
14	HLOCK2	RO	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
13	SLOCK2	RO	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
12	FIELD2	RO	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
11	VLOCK2	RO	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
10	NOVIDEO2	RO	1= No Video 0= Video	0
9	MONO2	RO	1 = No color burst signal detected. 0 = Color burst signal detected.	0
8	DET502	RO	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x044 – Video Decoder Status(VIN1 input video)

Bit	Function	R/W	Description	Reset
7	VDLOSS1	RO	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
6	HLOCK1	RO	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK1	RO	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD1	RO	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK1	RO	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	NOVIDEO1	RO	1= No Video 0= Video	0
1	MONO1	RO	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET501	RO	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x04C – Audio Detection Status

Bit	Function	R/W	Description	Reset
7-4	Reserved	RO		0
3	DET_AUDIO4	RO	1: Audio detected in AIN4 input. 0: not detected.	0
2	DET_AUDIO3	RO	1: Audio detected in AIN3 input. 0: not detected.	0
1	DET_AUDIO2	RO	1: Audio detected in AIN2 input. 0: not detected.	0
0	DET_AUDIO1	RO	1: Audio detected in AIN1 input. 0: not detected.	0

0x058 – DEVICE ID

Bit	Function	R/W	Description	Reset
31-16	Device ID	RO	These bits show Device ID value in PCI configuration space. Function 5 Audio 2 : 6815h Function 6 Audio 3 : 6816h Function 7 Audio 4 : 6817h	6815h/ 6816h/ 6817h
15-8	Revision ID	RO	These bits show Revision ID value in PCI configuration space.	10h
7	Reserved	RO		0
6-4	FUNC	RO	These bits show Function number in this function space. Function 5 Audio 2 : 5h Function 6 Audio 3 : 6h Function 7 Audio 4 : 7h	5h/6h/7h
3-0	Reserved	RO		0

0x05C – SUBSYSTEM

Bit	Function	R/W	Description	Reset
31-16	Subsystem ID	RO	These bits show Subsystem ID value in this PCI configuration space. Function 5 Audio 2 : 6815h Function 6 Audio 3 : 6816h Function 7 Audio 4 : 6817h	6815h/ 6816h/ 6817h
15-0	Subsystem Vendor ID	RO	These bits show Subsystem Vendor ID value in this PCI configuration space.	1797h

0x060 – ADMAERRPASS

Bit	Function	R/W	Description	Reset
31-1	Reserved	RO		0h
0	ADMAERRPASS	R/W	1: Ignore error DMAP command data when those are received in audio DMA logic. 0: Generate admaperr interrupt when error DMAP command data are received.	1

0x064 – ADROPVAL

Bit	Function	R/W	Description	Reset
31-13	Reserved	RO		00000h
12-8	ADROPVALUE	R/W	Audio data dropping threshold value. Audio data dropping are happening when audio FIFO has 32bit word data more than this value.	1Fh
7-0	Reserved	RO		00

0x078 – M66EN

Bit	Function	R/W	Description	Reset
31-1	Reserved	RO		0
0	M66EN	RO	M66EN pin status. 0:33MHz PCI Bus is connected to TW6816. 1:66MHz PCI Bus is connected to TW6816.	X

Application Information

Video Input Interface

The TW6816 has a built-in 4:1 input MUX for software controllable input selections. This MUX can be used to select one composite video source of 4 input video sources. For a typical application, a video input should be first terminated with a 75-ohm resistor before it is AC coupled by a 0.1uF capacitor to the input of the MUX.

A/D Converter

The TW6816 has four internal A/D converters to cover all possible analog video signal sources. The reference supply generator for the A/D converter is also on-chip.

Clamping/AGC

The TW6816 has built-in automatic clamping control circuitry. No extra external component is needed for this operation. The clamping loop gain can be controlled through register setting. The TW6816 also has built-in automatic AGC control circuitry. The AGC loop gain can also be controlled by register. The AGC loop response time is also register programmable.

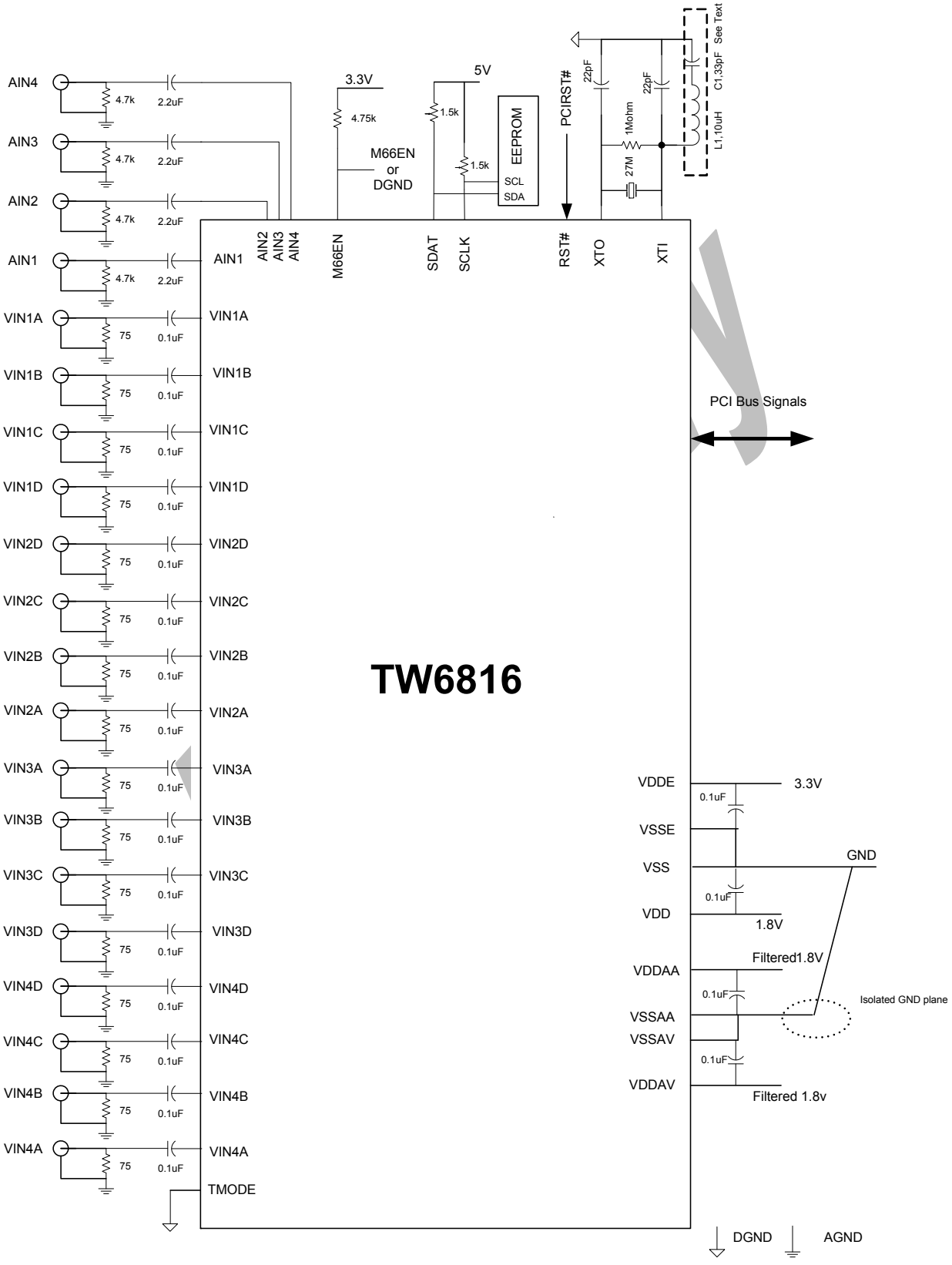
Clock Generation

The TW6816 requires one 27MHz crystal connected to XTI and XTO for all format decoding. The default crystal type should be 27MHz, fundamental mode, 20pF load capacitance or less, +-50ppm, and with series resistance of 80 ohm or less. An external clock source of 27MHz can also be connected to the XTI input in place of the crystal. A typical 27MHz third overtone crystal circuit is shown in the following figure. In the case of using 27MHz fundamental mode crystal, the C1 and L1 can be omitted.

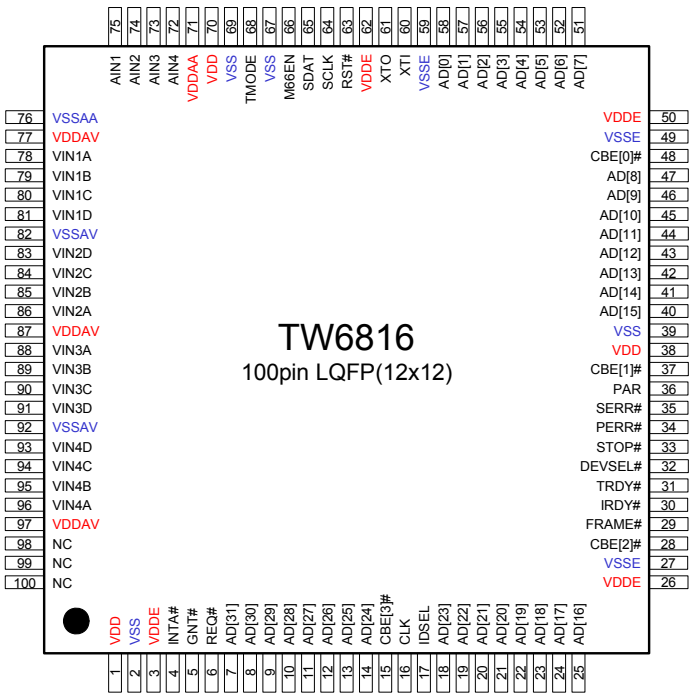
Application Schematics

Following pages show typical application schematics with TW6816.

Application Schematics



Pin Diagram



Pin Description

PCI Interface Pins

Pin#	I/O	Pin Name	Description
16	I	CLK	This input provides timing for all PCI transactions. All PCI signals except RST and INTA are sampled on the rising edge of CLK, and all other timing parameters are defined with respect to this edge. The TW6816 supports a PCI clock of up to 66 MHz.
63	I	RST#	This input three-states all PCI signals asynchronous to the CLK signal.
5	I	GNT#	Agent granted bus.
6	O	REQ#	Agent desires bus.
17	I	IDSEL	This input is used to select the TW6816 during configuration read and write transactions.
7-14, 18-25, 40-47, 51-58	I/O	AD[31:0]	These tri-state, bi-directional, I/O pins transfer both address and data information. A bus transaction consists of an address phase followed by one or more data phases for either read or write operations.
15, 28, 37, 48	I/O	CBE#[3:0]	These three-state, bi-directional, I/O pins transfer both bus command and byte enable information. During the address phase of a transaction, CBE[3:0] contain the bus command. During the data phase, CBE[3:0] are used as byte enables.
36	I/O	PAR	This tri-state, bi-directional, I/O pin provides even parity across AD[31:0] and CBE[3:0]. This means that the number of 1's on PAR, AD[31:0], and CBE[3:0] equals an even number.
29	I/O	FRAME#	This sustained tri-state signal is driven by the current master to indicate the beginning and duration of an access.
30	I/O	IRDY#	This sustained tri-state signal indicates the bus master's readiness to complete the current data phase. IRDY is used in conjunction with TRDY.
31	I/O	TRDY#	This sustained three-state signal indicates the target's readiness to complete the current data phase. TRDY is used in conjunction with IRDY.
32	I/O	DEVSEL#	This sustained three-state signal indicates device selection. When actively driven, DEVSEL indicates the driving device has decoded its address as the target of the current access.
33	I/O	STOP#	This sustained three-state signal indicates the target is requesting the master to stop the current transaction.
34	I/O	PERR#	Report data parity error.
35	O	SERR#	Report address parity error. Open drain.
4	O	INTA#	This signal is an open drain output for interrupts.

M66EN Pin

Pin#	I/O	Pin Name	Description
66	I	M66EN	Connect Pin49B M66EN on PCI Bus connector with Pull-up.If connected to digital GND,PCI Bus Interface is always working with 33MHz PCI clock mode.

Analog Interface Pins

Pin#	I/O	Pin Name	Description
78, 79, 80, 81, 86, 85, 84, 83, 88, 89, 90, 91, 96, 95, 94, 93	I, analog	VIN1A, VIN1B, VIN1C. VIN1D, VIN2A, VIN2B, VIN2C, VIN2D, VIN3A, VIN3B, VIN3C, VIN3D, VIN4A, VIN4B, VIN4C, VIN4D	These are the analog composite video inputs pins to the input selector.
75,74, 73,72	I, analog	AIN1, AIN2, AIN3, AIN4	These are the analog sound input pin to analog gain control block.

Two-wire Serial Interface Pins

Pin#	I/O	Pin Name	Description
64	I/O	SCLK	Serial clock
65	I/O	SDAT	Serial data

Video Decoder Clock Pins

Pin#	I/O	Pin Name	Description
60	I	XTI	Clock Zero pins. A 27 MHz fundamental (or third harmonic) crystal can be connected directly to this pin or a single-ended oscillator can be connected to XTI.
61	O	XTO	For crystal 27 MHz connection.

Test Pin

Pin#	I/O	Pin Name	Description
68	I	TMODE	Test Input pin. It must be connected to Digital ground during normal operation.

Power and Ground Pins

Pin#	I/O	Pin Name	Description
1,38,70	Power	VDD	+1.8 V power supply for digital circuitry. All VDD pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VDD pins and the digital ground plane as close to the device as possible.
2, 39, 67, 69	Ground	VSS	Core power return. Ground for digital circuitry.
3,26,50,62	Power	VDDE	+3.3v power supply for IO Pad. A 0.1 µF ceramic capacitor should be connected between each group of VDDE pins and the ground plane as close to the device as possible.
26,49,59	Ground	VSSE	I/O power return
71	Power	VDDAA	+1.8 power supply for analog audio circuits. VDDAA pin must be connected as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between VDDAA pin and the analog ground plane as close to the device as possible.
76	Ground	VSSAA	Analog 1.8 power return for analog audio circuits.
77,87,97	Power	VDDAV	+1.8 power supply for analog video circuits.All VDDAV pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VDDAV pins and the analog ground plane as close to the device as possible.
82,92	Ground	VSSAV	Analog 1.8 power return for analog video circuits.

Parametric Information

AC/DC Electrical Parameters

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VDDAV (measured to VSSAV)	V_{DDAVM}	-	-	2.0	V
VDDAA(measured to VSSAA)	V_{DDAAM}	-	-	2.0	V
V_{DD} (measured to VSS)	V_{DDM}		-	2.0	V
Voltage on any signal pin (See the note below)	-	VSS –0.5	-	V_{DDM} + 0.5	V
Analog Input Voltage	-	VSSAV – 0.5	-	V_{DDAVM} + 0.5	V
	-	VSSAA-0.5	-	V_{DDAAM} + 0.5	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}	-	-	+220	°C

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or drops below ground by more than 0.5 V can induce destructive latchup.

Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Supply					
Power Supply — IO	V_{DDE}	3.15	3.3	3.6	V
Power Supply — Analog	VDDAV	1.6	1.8	2.0	V
	VDDAA	1.6	1.8	2.0	V
Power Supply — Digital	V_{DD}	1.6	1.8	2.0	V
Maximum $\|V_{DD}$ – VDDAV|		-	-	0.3	V
Maximum $\|V_{DD}$ – VDDAA|		-	-	0.3	V
VIN1A,VIN1B,VIN1C,VIN1D,VIN2A,VIN2B, VIN2C,VIN2D,VIN3A,VIN3B,VIN3C,VIN3D, VIN4A,VIN4B,VIN4C,VIN4D Input Range (AC coupling required)		0.5	1.00	1.4	V
AIN1,AIN2,AIN3,AIN4 Input Range (AC coupling required)		0.5	1.00	1.4	V
Ambient Operating Temperature	T_A	0		+70	°C
Analog Core Supply current - Video	VDDAV	-	TBD	-	mA
Analog Core Supply current – Audio	VDDAA	-	TBD	-	mA
Digital IO Supply current	VDDE	-	TBD	-	mA
Digital Core Supply Current	VDD	-	TBD	-	mA

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	V_{DDE} + 0.5	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DDE} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	VSS -0.5	-	1.0	V
Input High Current (V_{IN} =V_{DD})	I_{IH}	-	-	10	μA
Input Low Current (V_{IN} =VSS)	I_{IL}	-	-	–10	μA
Input Capacitance (f=1 MHz, V_{IN} =2.4 V)	C_{IN}	-	5	-	pF
Digital Outputs					
Output High Voltage (I_{OH} = –4 mA)	V_{OH}	2.4	-	V_{DDE}	V
Output Low Voltage (I_{OL} = 4 mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	μA
Output Capacitance	C_O	-	5	-	pF
Analog Input					
Analog Pin Input voltage	Vi	-	1	-	Vpp
Analog Pin Input Capacitance	C_A	-	7	-	pF
Crystal spec					
nominal frequency (fundamental)		-	27	-	MHz
deviation		-	-	±50	ppm
Temperature range	Ta	0	-	70	°C
load capacitance	CL	-	20	-	pF
series resistor	RS	-	80	-	Ohm
Oscillator Input					
nominal frequency		-	27	-	MHz
deviation		-	-	±50	ppm
duty cycle		-	-	55	%

Video Decoder Parameter 1

Parameter	Symbol	Min	Typ	Max	Units
ADCs					
ADC resolution	ADCR	-	10	-	Bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	24	27	30	MHz
Horizontal PLL					
Line frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency (60Hz)	f_{LN}	-	15.734	-	KHz
static deviation	Δf_H	-	-	6.2	%
Subcarrier PLL					
subcarrier frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
subcarrier frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
subcarrier frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
subcarrier frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
lock in range	Δf_H	±450	-	-	Hz

Video Decoder Parameter 2

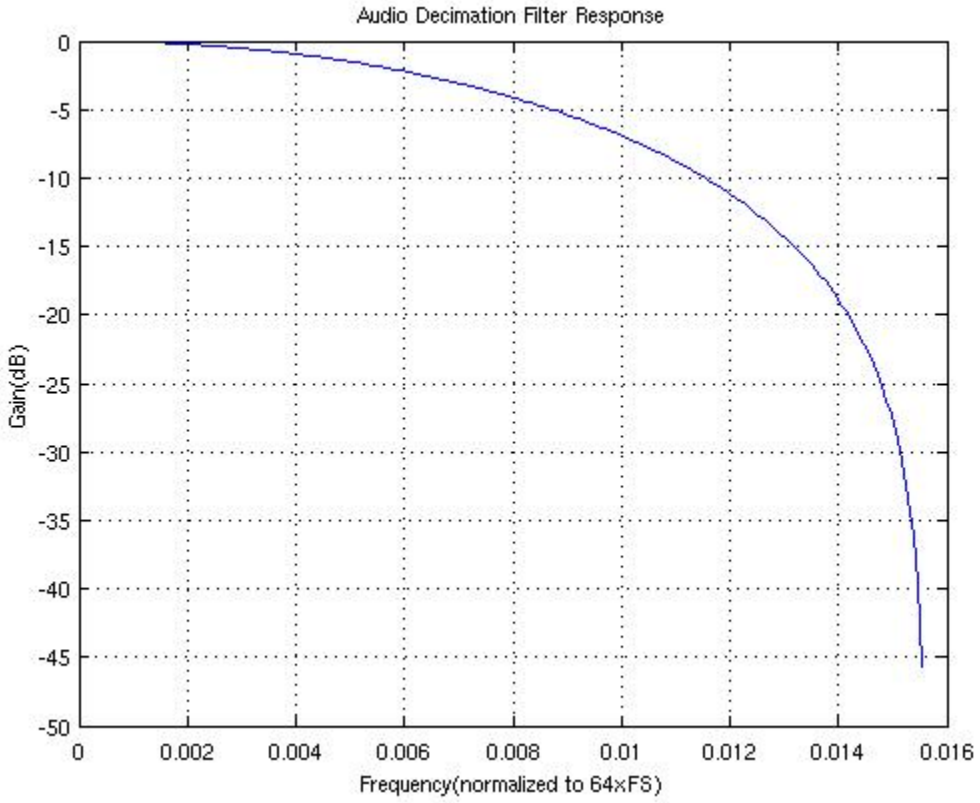
Parameter	Symbol	Min	Typ	Max	Units
Lock Specification					
Sync Amplitude Range		1		200	%
Color Burst Range		5		200	%
Horizontal Lock Range		-5		5	%
Vertical Lock Range		45		65	Hz
Fsc Lock Range			±450		Hz
Color Burst Position Range			±2.2		μs
Color Burst Width Range					cycle
Video Bandwidth					
B/W			6		MHz
Noise Specification					
SNR (Luma flat field)			57		dB
Nonlinear Specification					
Y Nonlinearity			0.5	0.7	%
Differential Phase	DP		0.4	0.6	Degree
Differential Gain	DG		0.6	0.8	%
Chroma Specification					
Hue Accuracy			1		Degree
Chroma ACC Range				400	%
Chroma Amplitude Error			1		%
Chroma Phase Error			0.3		%
Chroma Luma Intermodulation			0.2		%
K-Factor					
K_{2T}			0.5		%
$K_{pulse/bar}$			0.5		%

Analog Audio Parameters

Parameter	Symbol	Min	Typ	Max	Units
Analog Audio Input Characteristics					
AIN1-4 Input Impedance	RINX	10			Kohm
Interchannel gain mismatch			0.2		dB
Input voltage range				1.5	Vpp
Full scale input voltage[1]	V_{iFULL}		1		Vpp
Interchannel isolation[2]			90		dB
Analog Audio Output Characteristics					
AOUT Output Load Resistance	RLAO	300			ohm
AOUT Load Capacitance	CLAO			1	nF
AOUT Offset Voltage	VOSAO			100	mV
Full scale output voltage[3]	Vo_{FULL}		1.4		Vpp

1. Tested at input gain of 0 dB, Fin = 1KHz.
2. Tested at input gain of 0 dB, Fs=8 KHz and 16KHz.
3. Tested at output gain of 0 dB, Fout = 1KHz.

Audio Decimation Filter Response

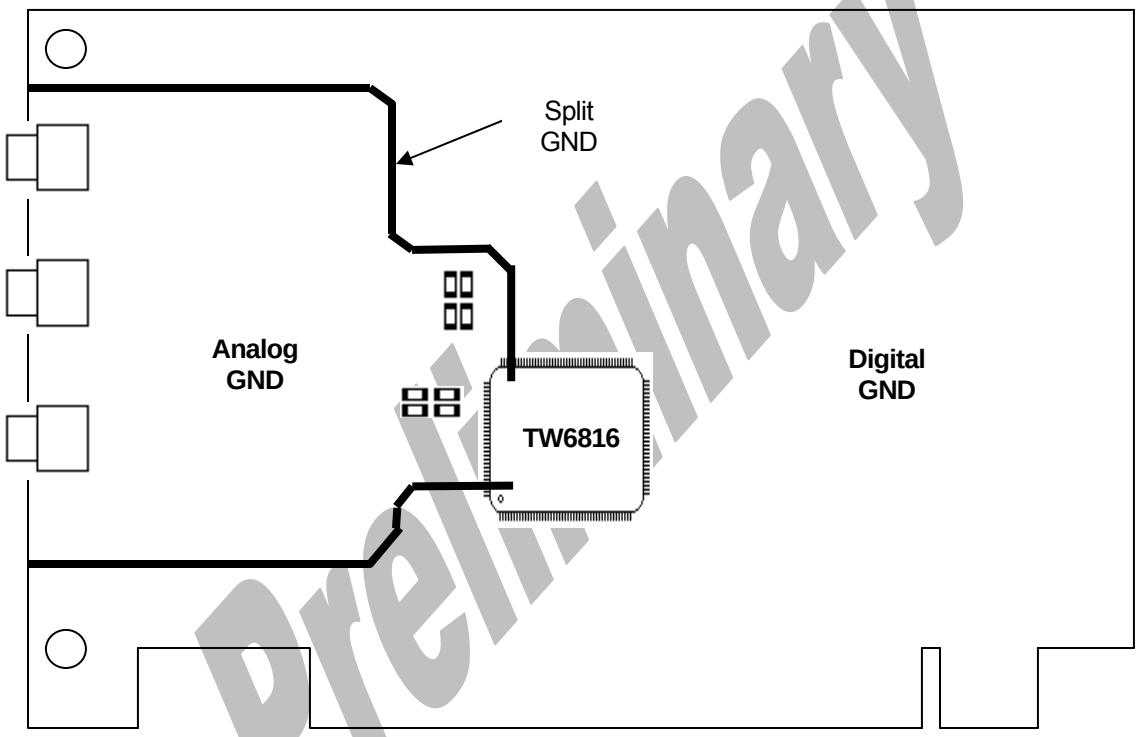


(*) 0.016 line = 0.016x64xFs

PCB Layout Considerations

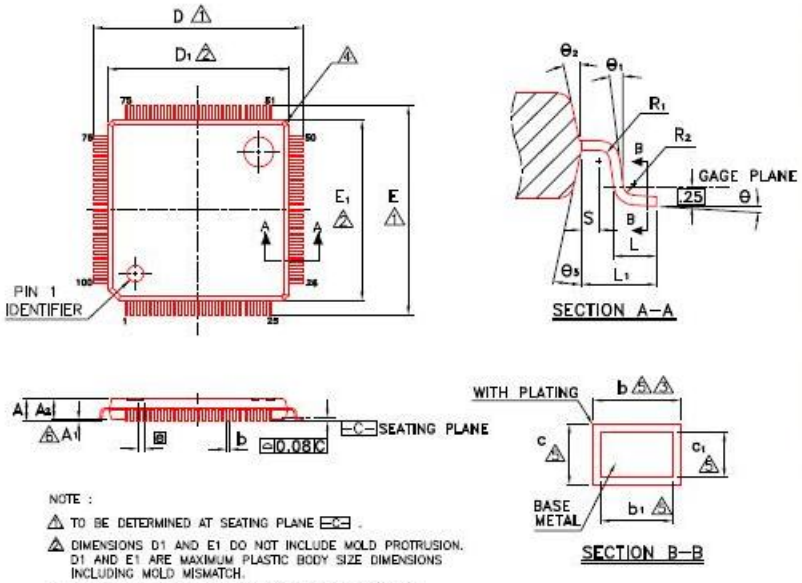
The PCB layout should be done to minimize the power and ground noise on the TW6816. This is done by good power de-coupling with minimum lead length on the de-coupling capacitors; well-filtered and regulated analog power input shielding and ground plane isolation.

The ground plane should cover most of the PCB area with separated digital and analog ground planes. These two planes should be at the same electrical potential and connected together under the TW6816. The input capacitor and termination registers are placed close to the input pins. The following figure shows a ground plane layout example.



To minimize crosstalk, the digital signals of TW6816 should be separated from the analog circuitry. Moreover, the digital signals should not cross over the analog power and ground plane. Parallel running of digital lines for long distance should also be avoided.

100-pin LQFP Package Mechanical Drawing



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	14.00 BSC			0.551 BSC		
D1	12.00 BSC			0.472 BSC		
E	14.00 BSC			0.551 BSC		
E1	12.00 BSC			0.472 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE :

1. TO BE DETERMINED AT SEATING PLANE C .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BDD.

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Revision History

Datasheet Revision History:

Revision	Date	File name	Note
REV. A1	10/15/2009	TW6816spec10152009	Initial documents