CS5460A

Single Phase Bi-Directional Power/Energy IC

Features

- Energy Data Linearity: 0.1% of Reading over 1000:1 Dynamic Range
- On-Chip Functions: Energy, I ∗ V, I_{RMS} and V_{RMS}, Energy to Pulse-Rate Conversion
- Smart "Auto-Boot" Mode from Serial EEPROM with no microcontroller.
- AC or DC System Calibration
- Mechanical Counter/Stepper Motor Driver
- Meets Accuracy Spec for IEC 687/1036, JIS
- Power Consumption <12 mW
- Interface Optimized for Shunt Sensor
- Phase Compensation
- Ground-Referenced Signals with Single Supply
- On-chip 2.5 V Reference (MAX 60 ppm/°C drift)
- Simple Three-Wire Serial Interface
- Watch Dog Timer
- Power Supply Monitor
- Power Supply Configurations
  VA+ = +5 V; VA- = 0 V; VD+ = +3 V to +5 V
  VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V

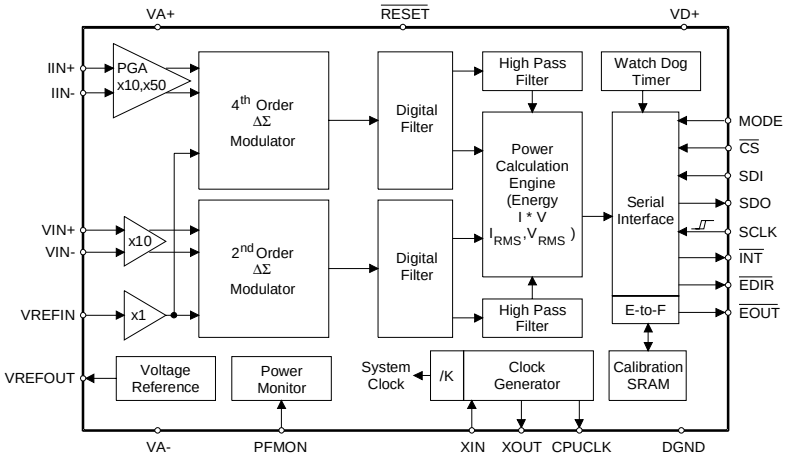
Description

The CS5460A is a highly integrated ΔΣ Analog-to-Digital Converter (ADC) which combines two ΔΣ ADCs, high speed power calculation functions, and a serial interface on a single chip. It is designed to accurately measure and calculate: Energy, Instantaneous Power, I_{RMS}, and V_{RMS} for single phase 2- or 3-wire power metering applications. The CS5460A interfaces to a low cost shunt or transformer to measure current, and resistive divider or transformer to measure voltage. The CS5460A features a bi-directional serial interface for communication with a micro-controller and a programmable frequency output that is proportional to energy. CS5460A has on-chip functionality to facilitate AC or DC system-level calibration.

The "Auto-Boot" feature allows the CS5460A to function "stand-alone" and to initialize itself on system power up. In Auto-Boot Mode, the CS5460A reads the calibration data and start-up instructions from an external EEPROM. In this mode, the CS5460A can work without the need for a microprocessor, for low-cost metering applications.

ORDERING INFORMATION:

CS5460A-BS	-40°C to +85°C	24-pin SSOP
CS5460A-KS	0°C to +70°C	24-pin SOIC



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = -40° C to +85° C; VA+, VD+ = +5 V ±10%; VREFIN = 2.5 V; VA- = AGND; MCLK = 4.096 MHz, K = 1; N = 4000, OWR = 4.0 kHz.)(See Notes 1, 2, and 3)

Parameter	Symbol	Min	Typ	Max	Unit
Accuracy (Both Channels)					
Total Harmonic Distortion	THD	74	-	-	dB
Common Mode Rejection (DC, 50, 60 Hz)	CMRR	80	-	-	dB
Offset Drift (Without the High Pass Filter)		-	5	-	nV/°C
Analog Inputs (Current Channel)					
Differential Input Voltage Range {(IIN+) - (IIN-)} (Gain = 10) (Gain = 50)	IIN	0 0	- -	±250 ±50	mV(dc) mV(dc)
Common Mode + Signal on IIN+ or IIN- (Gain = 10 or 50)		-0.25	-	VA+	V
Crosstalk with Voltage Channel at Full Scale (50, 60 Hz)		-	-	-115	dB
Input Capacitance (Gain = 10) (Gain = 50)	IC	- -	25 25	- -	pF pF
Effective Input Impedance (Note 4) (Gain = 10) (Gain = 50)	EII	 30 30	 - -	 - -	 kΩ kΩ
Noise (Referred to Input) (Gain = 10) (Gain = 50)		- -	- -	20 4	μV_{rms} μV_{rms}
Accuracy (Current Channel)					
Bipolar Offset Error (Note 1)	VOS	-	-	±0.001	%F.S.
Full-Scale Error (Note 1)	FSE	-	-	±0.001	%F.S.
Analog Inputs (Voltage Channel)					
Differential Input Voltage Range {(VIN+) - (VIN-)}	VIN	0	-	±250	mV(dc)
Common Mode + Signal on VIN+ or VIN-		-0.25	-	VA+	V
Crosstalk with Current Channel at Full Scale (50, 60 Hz)		-	-	-70	dB
Input Capacitance	IC	-	0.2	-	pF
Effective Input Impedance (Note 4)	EII	5	-	-	MΩ
Noise (Referred to Input)		-	-	250	μV_{rms}
Accuracy (Voltage Channel)					
Bipolar Offset Error (Note 1)	VOS	-	-	±0.01	%F.S.
Full-Scale Error (Note 1)	FSE	-	-	±0.01	%F.S.

Notes:
1. Applies after system calibration
2. Specifications guaranteed by design, characterization, and/or test.
3. Analog signals are relative to VA- and digital signals to DGND unless otherwise noted.
4. Effective Input Impedance (EII) is determined by clock frequency (DCLK) and Input Capacitance (IC). EII = 1/(IC*DCLK/4)

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Phase Compensation Range (Voltage Channel, 60 Hz)		-2.4	-	+2.5	°
High Rate Filter Output Word Rate (Both Channels)	OWR	-	DCLK/1024	-	Hz
Input Sampling Rate DCLK = MCLK/K		-	DCLK/4	-	Hz
Full Scale DC Calibration Range (Note 5)	FSCR	25	-	100	%F.S.
Channel-to-Channel Phase Error (60 Hz) (when PC[6:0] bits are set to “0000000”)			0.02		Deg
High Pass Filter Pole Frequency -3 dB		-	0.5	-	Hz
Reference Output					
Output Voltage	REFOUT	2.4	-	2.6	V
Temperature Coefficient		-	25	60	ppm/°C
Load Regulation (Output Current 1 µA Source or Sink)	ΔV_R	-	6	10	mV
Output Noise Voltage (0.1 Hz to 512 kHz)	eN	-	100	-	μV_{rms}
Reference Input					
Input Voltage Range	VREFIN	2.4	2.5	2.6	V
Input Capacitance		-	4	-	pF
Input CVF Current		-	25	-	nA
Power Supplies					
Power Supply Currents (Normal Mode) I_{A+}	PSCA	-	1.3	-	mA
I_{D+} (VD+ = 5 V)	PSCD	-	2.9	-	mA
I_{D+} (VD+ = 3 V)	PSCD	-	1.7	-	mA
Power Consumption Normal Mode (VD+ = 5 V)	PC	-	21	25	mW
(Note 6) Normal Mode (VD+ = 3 V)		-	11.6	-	mW
Standby		-	6.75	-	mW
Sleep		-	10	-	µW
Power Supply Rejection (50, 60 Hz)			-	-	
(Gain = 10)	PSRR	56			dB
(Gain = 50)	PSRR	70			dB
Power Monitor Hysteresis Thresholds	PM	2.3		2.7	V

Notes: 5. The minimum FSCR is limited by the maximum allowed gain register value.
6. All outputs unloaded. All inputs CMOS level.

5 V DIGITAL CHARACTERISTICS (T_A = -40° C to +85° C; VA+, VD+ = 5 V ±10% VA-, DGND = 0 V) (See Notes 2 and 7)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN and SCLK and /RESET		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and /RESET		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN and SCLK and /RESET		-	-	0.8	V
XIN		-	-	1.5	V
SCLK and /RESET		-	-	0.2 VD+	V
High-Level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

3 V DIGITAL CHARACTERISTICS (T_A = -40° C to +85° C; VA+ = 5 V ±10%, VD+ = 3 V ±10%; VA-, DGND = 0 V) (See Notes 2 and 7)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN and SCLK and /RESET		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and /RESET		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN and SCLK and /RESET		-	-	0.48	V
XIN		-	-	0.3	V
SCLK and /RESET		-	-	0.2 VD+	V
High-Level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

Notes: 7. All measurements performed under static conditions.

ABSOLUTE MAXIMUM RATINGS (DGND = 0 V; See Note 8)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 9 and 10)					
Positive Digital		VD+	-0.3	-	+6.0	V
Positive Analog		VA+	-0.3	-	+6.0	V
Negative Analog		VA-	+0.3	-	-6.0	V
Input Current, Any Pin Except Supplies	(Note 11 and 12)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Power Dissipation	(Note 13)	PDN	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	- 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 8. All voltages with respect to ground.

9. VA+ and VA- must satisfy {(VA+) - (VA-)} ≤ +6.0 V.

10. VD+ and VA- must satisfy {(VD+) - (VA-)} ≤ +6.0 V.

11. Applies to all pins including continuous over-voltage conditions at the analog input (AIN) pins.

12. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

13. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = -40° C to +85 °C; VA+ = 5.0 V ±10%; VD+ = 3.0 V ±10% or 5.0 V ±10%; VA- = 0.0 V; Logic Levels: Logic 0 = 0.0 V, Logic 1 = VD+; CL = 50 pF))

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency Internal Gate Oscillator (Note 14)	MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle		40	-	60	%
CPUCLK Duty Cycle (Note 15)		40		60	%
Rise Times Any Digital Input Except SCLK (Note 16)	t_{rise}	-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Fall Times Any Digital Input Except SCLK (Note 16)	t_{fall}	-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Start-up					
Oscillator Start-up Time XTAL = 4.096 MHz (Note 17)	t_{ost}	-	60	-	ms
Serial Port Timing					
Serial Clock Frequency	SCLK	-	-	2	MHz
Serial Clock Pulse Width High	t_1	200	-	-	ns
Pulse Width Low	t_2	200	-	-	ns
SDI Write Timing					
$\overline{CS}$ Enable to Valid Latch Clock	t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising	t_4	50	-	-	ns
Data Hold Time After SCLK Rising	t_5	100	-	-	ns
SCLK Falling Prior to CS Disable	t_6	100	-	-	ns
SDO Read Timing					
$\overline{CS}$ Enable to Valid Latch Clock	t_7	-	-	150	ns
SCLK Falling to New Data Bit	t_8	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z	t_9	-	-	150	ns
Auto-Boot Timing					
MODE setup time to /RESET rising	t_{10}	50			ns
/RESET rising to /CS falling	t_{11}	48			MCLK
/CS falling to SCLK rising	t_{12}	100			ns
SDO out from SCLK falling hold time	t_{13}	0	20	50	ns
SDI input to SCLK rising setup time	t_{14}	50			ns
SDI input from SCLK rising hold time	t_{15}	50			ns
SCLK falling to /CS rising	t_{16}	100			ns
/CS rising to driving MODE low (to end auto-boot sequence).	t_{17}	50			ns

Notes: 14. Device parameters are specified with a 4.096 MHz clock, however, clocks between 3 MHz to 20 MHz can be used.

15. If external MCLK is used, then its duty cycle must be between 45% and 55% to maintain this spec.

16. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.

17. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

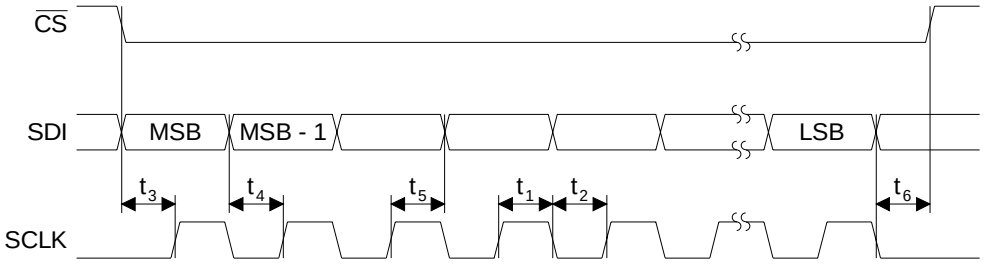


Figure 1. SDI Write Timing (Not to Scale)

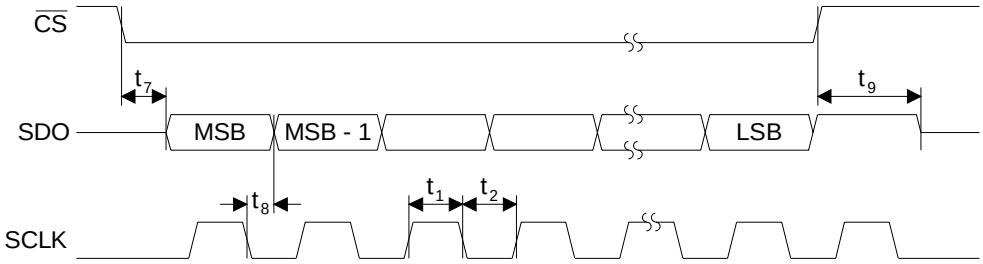


Figure 2. SDO Read Timing (Not to Scale)

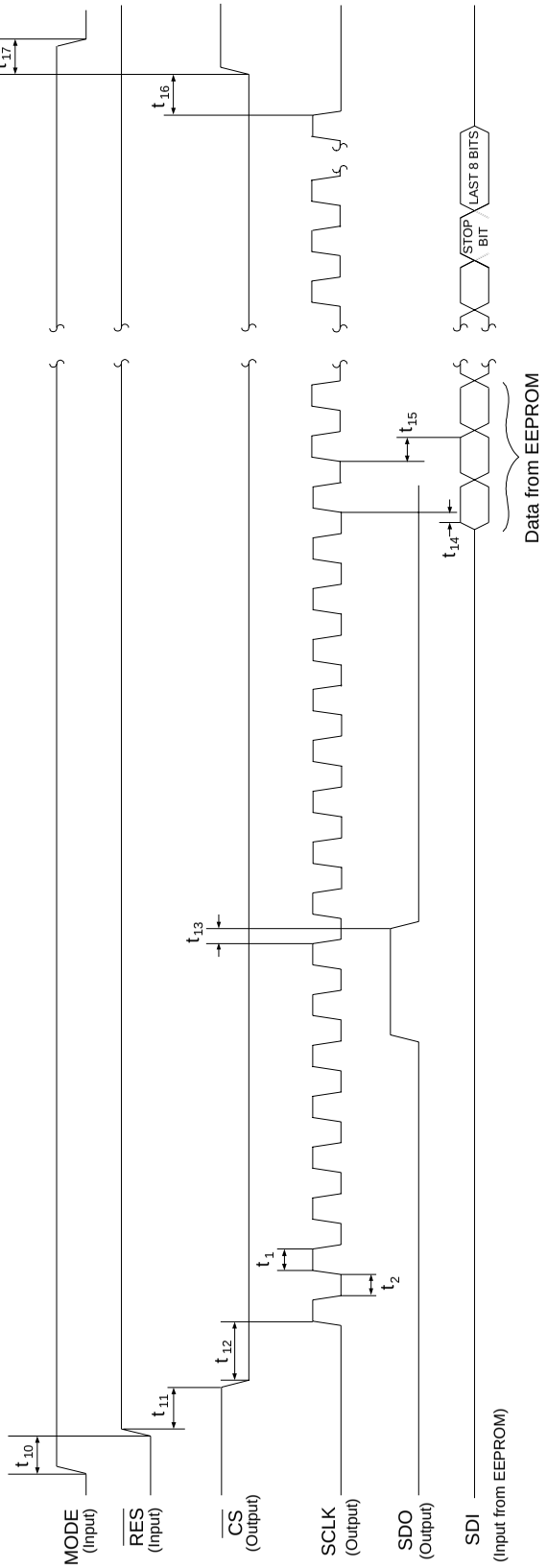


Figure 3. CS5460A Auto-Boot Sequence Timing

2. GENERAL DESCRIPTION

The CS5460A is a CMOS monolithic power measurement device with an energy computation engine. The CS5460A combines a programmable gain amplifier, two ΔΣ modulators, two high rate filters, system calibration, and power calculation functions to compute Energy, V_{RMS}, I_{RMS}, and Instantaneous Power.

The CS5460A is designed for power measurement applications and is optimized to interface to a shunt or current transformer to measure current, and a resistive divider or transformer to measure voltage. To accommodate various input voltage levels, the current channel includes a programmable gain amplifier (PGA) which provides either 150 mV_{RMS} or 30 mV_{RMS} as the full-scale input level.

The CS5460A includes two high-rate digital filters which output data at a (MCLK/K)/1024 output word rate (OWR).

To facilitate communication to a microcontroller, the CS5460A includes a simple three-wire serial interface which is SPI™ and Microwire™ compatible. The serial port has a Schmitt Trigger input on its serial clock (SCLK) to allow for slow rise time signals.

2.1 Theory of Operation

The CS5460A is designed to operate from a single +5 V supply or dual ±2.5 V supplies. It provides a 30 mV_{RMS} or 150 mV_{RMS} range for the current channel and to provide a 150mV_{RMS} range for the voltage channel. With single +5 V supply on VA+/-, the CS5460A accommodates common mode signals between -0.25 V and VA+.

Figure 4 shows the CS5460A connected to a service to measure power in a single-phase 2-wire system while operating in a single supply configuration. Figure 5 shows the CS5460A configured to measure power in a single-phase 3-wire system.

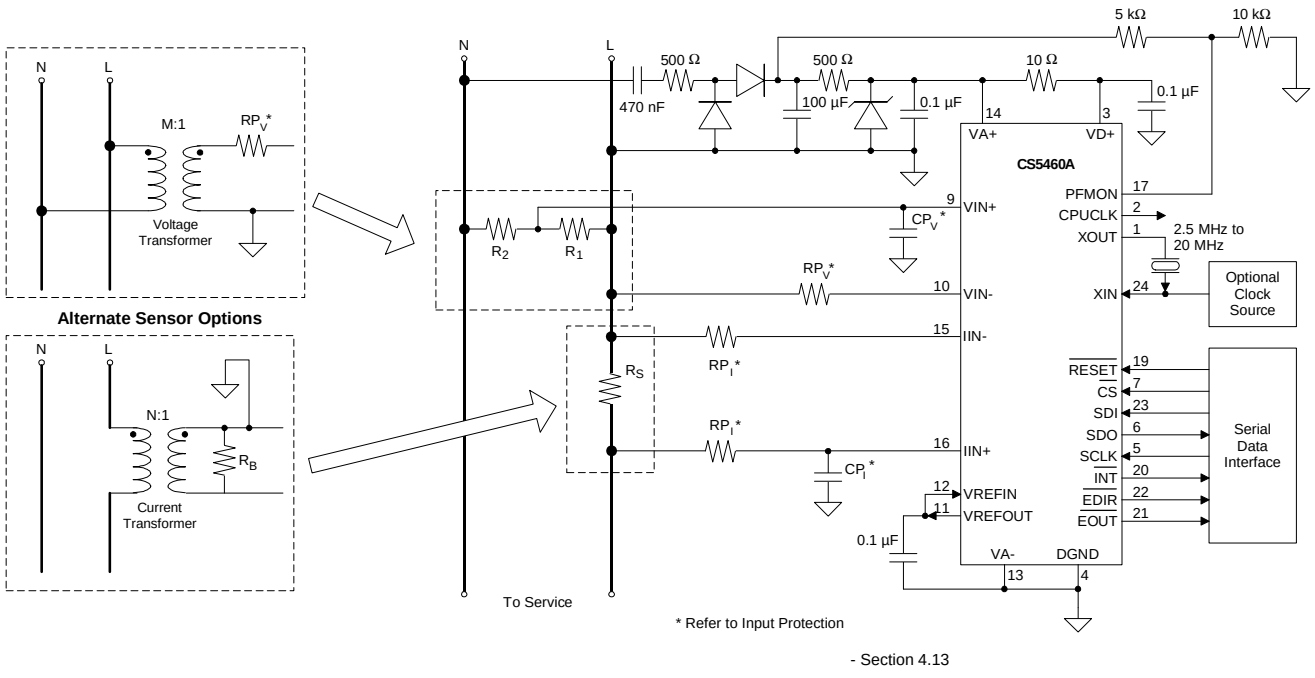


Figure 4. Typical Connection Diagram (One-Phase 2-Wire)

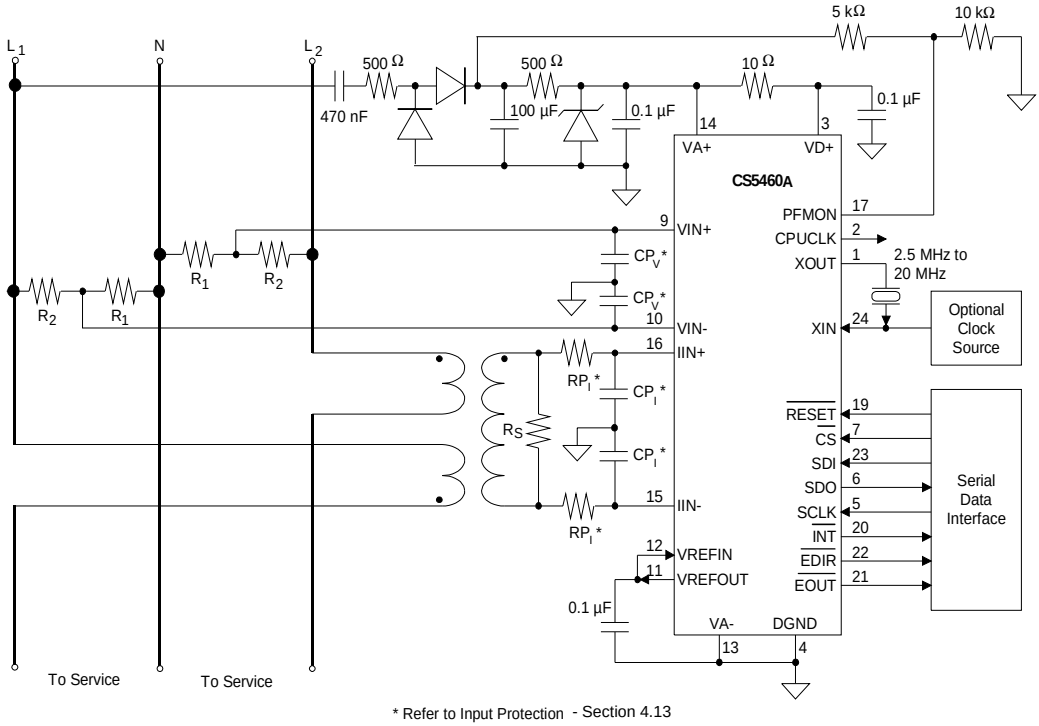


Figure 5. Typical Connection Diagram (One-Phase 3-Wire)

2.2 Performing Measurements

The CS5460A performs measurements of instantaneous current, instantaneous voltage, instantaneous power, energy, RMS current, and RMS voltage. These measurements are output as 24-bit signed and unsigned data formats as a percentage of full scale. This means that the 24-bit data words in the CS5460A output registers represent values between 0 and 1 (for unsigned output registers) or between -1 and +1 (for signed output registers). A register value of 1 represents the maximum possible value. Note that a value of 1.0 is never actually obtained in the registers of the CS5460A. As an illustration, in any of the signed output registers, the maximum register value is [(2^23 - 1) / (2^23)] = 0.999999880791. The flow of data to perform these calculations is shown in Figure 6. After each A/D conversion, the CRDY bit will be asserted in the Status Register, and the $\overline{\text{INT}}$ pin will also become active if the CRDY bit is unmasked. This assertion of CRDY bit indicates that new instantaneous voltage, current samples have been collected, and they are multiplied together to provide a corresponding instantaneous power sample.

The V_{RMS}, I_{RMS}, and energy calculations are updated every N conversions (which is known as 1 "*computation cycle*") where N is the content of the Cycle Count register. At the end of each computation cycle, the DRDY bit in the Status and Mask register will be set, and the $\overline{\text{INT}}$ pin will become active if the DRDY bit is unmasked.

DRDY is set only after each computation cycle has completed, whereas the CRDY bit is asserted after each individual A/D conversion. When these bits are asserted, they must be cleared by the user before they can be asserted again. If the Cycle Count Register value (N) is set to 1, all output calculations are instantaneous, and DRDY will indicate when instantaneous calculations are finished, just like the CRDY bit. For the RMS results to be valid, the Cycle-Count Register must be set to a value greater than 10.

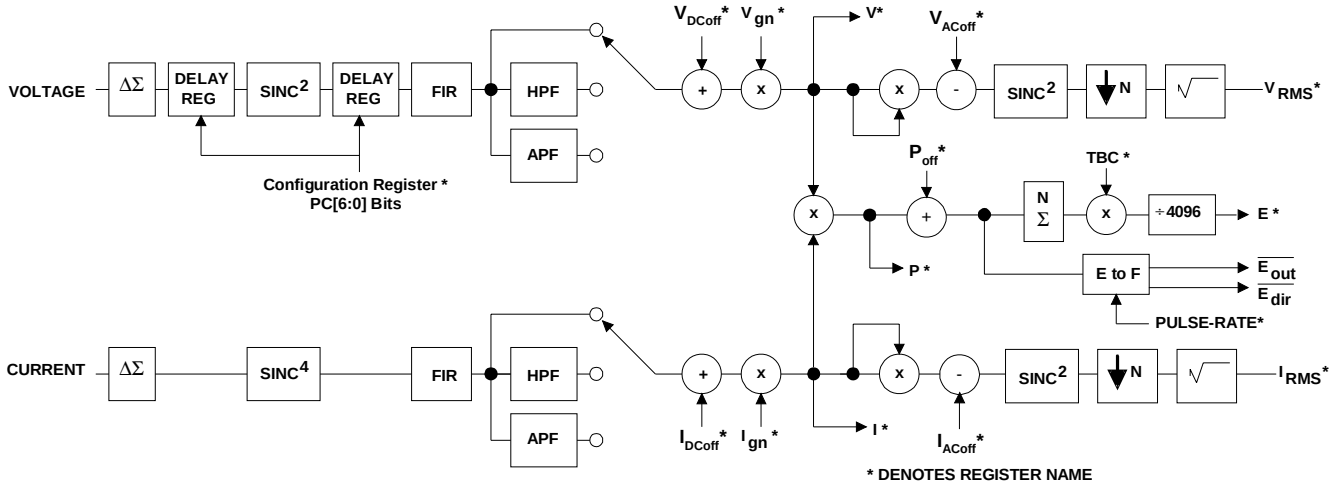


Figure 6. Data Flow.

Table 1 provides an example detailing the output linearity. A computation cycle is derived from the master clock and its frequency is (MCLK/K)/(1024*N). Under default conditions with a 4.096 Mhz clock at XIN, instantaneous A/D conversions for voltage, current, and power are performed at a 4000 Hz rate, whereas I_{RMS}, V_{RMS}, and energy calculations are performed at a 1 Hz rate.

2.2.1 Single Computation Cycle (C = 0)

Based on the information provided in the Cycle Count register, a single computation cycle is performed after the user transmits the single conversion cycle command. After the computations are complete, DRDY is set. Thirty-two SCLKs are then needed to acquire a calculation result from one of several result registers. The first 8 SCLKs are used to clock in the command to determine which register is to be read. The last 24 SCLKs are used to read the desired register. After reading the data, the serial port returns to the command mode, where it waits for a new command to be issued.

	Energy	Vrms	Irms
Range	1000:1	2:1	500:1
Max Input	See *Analog Characteristics*		
Linearity (After Calibration)	0.1% of reading	0.1% of reading	0.1% of reading
Output word	24-bits		

Table 1. Output Linearity after Calibration with MCLK = 4.096 MHz, K = 1, N = 4000

2.2.2 Multiple Computation Cycles (C = 1)

Based on the information provided in the Cycle Count register, computation cycles are repeatedly performed on the voltage and current channels (after every N conversions). Computation cycles cannot be started/stopped on a per channel basis. After each computation cycle is completed, DRDY is set. Thirty-two SCLKs are then needed to read a register. The first 8 SCLKs are used to clock in the command to determine which results register is to be read. The last 24 SCLKs are used to read the calculation result. While in this mode, the user may choose to acquire only the calculations required for the application as DRDY rises and falls to indicate the availability of a new data.

The RMS calculations undergo a $Sinc^2$ operation prior to their square root operation. Therefore, the first output for each channel will be invalid (i.e. all RMS calculations are invalid in the single compu-

tation cycle routine and the first RMS calculations will be invalid in the continuous computation cycle). All energy calculations will be valid since energy calculations do not require this $Sinc^2$ operation.

2.3 High Rate Digital Filters

Referring to Figure 6, the high rate filter on the voltage channel is implemented as a fixed $Sinc^2$ filter, compensated by a short length FIR. When the converter is driven with a 4.096 MHz clock (K=1), the filter has a magnitude response as shown in Figure 7. Note that the filter's response scales with MCLK frequency and K.

The current channel contains a $Sinc^4$ filter, compensated by a short length FIR. When the converter is driven with a 4.096 MHz clock (K=1) the composite filter response is given in Figure 8.

2.4 High-Pass Filters

A digital high-pass filter in both channels can be enabled to remove the DC content from the input signal before the energy calculations are made. These filters are activated by enabling certain bits in the configuration register. If the user wants to use the high-pass filters on just one of the two channels, then the user should apply the all-pass filter option to the other channel. For example, if high-pass filter is needed for voltage channel, but not the current channel, then the all-pass filter can be used in the voltage channel to match the phase delay that is naturally introduced by the high-pass filter.

3. SERIAL PORT OVERVIEW

The CS5460A's serial port incorporates a state machine with transmit/receive buffers. The state machine interprets 8 bit command words on the rising edge of SCLK. Upon decoding of the command word the state machine performs the requested command or prepares for a data transfer of the addressed register. Request for a read requires an internal register transfer to the transmit buffer, while a write waits until the completion of 24 SCLKs before performing a transfer. The internal registers are used to control the ADC's functions. All registers are 24-bits in length. Figure 20 summarizes the internal registers available to the user.

The CS5460A is initialized and fully operational upon power-on. After a power-on, serial port initialization, or reset, the serial port state machine is initialized into *command mode* where it waits to receive a valid command (the first 8-bits clocked into the serial port). Upon receiving and decoding a valid command word, the state machine instructs the converter to either perform a system operation, or transfer data to or from an internal register. The user should refer to the "Commands" section to decode all valid commands.

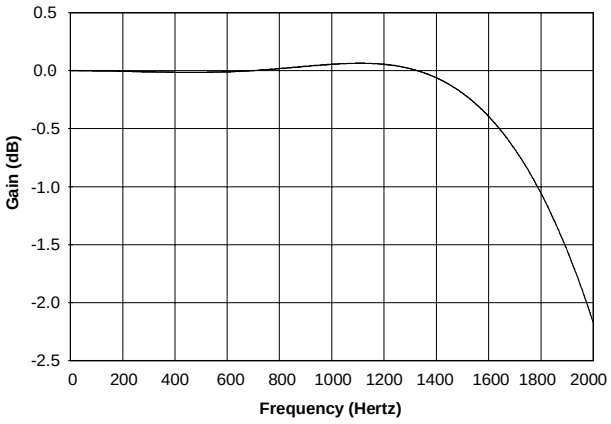


Figure 7. Voltage Input Filter Characteristics

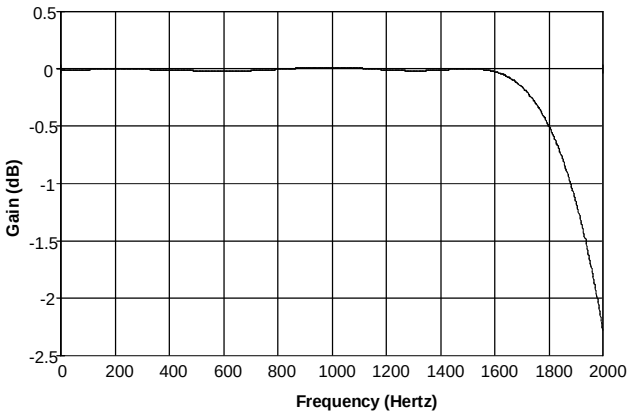


Figure 8. Current Input Filter Characteristics

3.1 Commands (Write Only)

All command words are 1 byte in length. Commands that write to a register must be followed by 1, 2, or 3 bytes of register data. Commands that read from registers initiate 3 bytes of register data. Commands that read data can be chained with other commands (e.g., while reading data, a new command can be sent to SDI which can execute before the original read is completed). This allows for “chaining” commands.

3.1.1 Start Conversions

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	C	0	0	0

This command indicates to the state machine to begin acquiring measurements and calculating results. The device has two modes of acquisition.

C = Modes of measurement
0 = Perform a single computation cycle
1 = Perform continuous computation cycles

3.1.2 SYNC0 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	0

This command is the end of the serial port re-initialization sequence. The command can also be used as a NOP command. The serial port is resynchronized to byte boundaries by sending three or more consecutive SYNC1 commands followed by a SYNC0 command.

3.1.3 SYNC1 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	1

This command is part of the serial port re-initialization sequence. The command can also serve as a NOP command.

3.1.4 Power-Up/Halt

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

If the device is powered-down, this command will power-up the device. When powered-on, no computations will be running. If the part is already powered-on, all computations will be halted.

3.1.5 Power-Down

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	S1	S0	0	0	0

The device has two power-down modes to conserve power. If the chip is put in stand-by mode all circuitry except the clock generator is turned off.

S1,S0 Power-down mode
00 = Reserved
01 = Halt and enter stand-by power saving mode. This mode allows quick power-on time
10 = Halt and enter sleep power saving mode. This mode requires a slow power-on time
11 = Reserved

3.1.6 Calibration

B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	V	I	R	G	O

The device has the capability of performing a system AC offset calibration, DC offset calibration, AC gain calibration, and DC gain calibration. The user can calibrate the voltage channel, the current channel, or both channels at the same time. Offset and gain calibrations should NOT be performed at the same time (must do one after the other). For a given application, if DC gain calibrations are performed, then AC gain calibration should not be performed (and vice-versa). The user must supply the proper inputs to the device before initiating calibration.

V,I Designates calibration channel
00 = Not allowed
01 = Calibrate the current channel
10 = Calibrate the voltage channel
11 = Calibrate voltage and current channel simultaneously

R Specifies AC calibration (R=1) or DC calibration (R=0)

G Designates gain calibration
0 = Normal operation
1 = Perform gain calibration

O Designates offset calibration
0 = Normal operation
1 = Perform offset calibration

3.1.7 Register Read/Write

B7	B6	B5	B4	B3	B2	B1	B0
0	W/$\overline{R}$	RA4	RA3	RA2	RA1	RA0	0

This command informs the state machine that a register access is required. On reads the addressed register is loaded into the output buffer and clocked out by SCLK. On writes the data is clocked into the input buffer and transferred to the addressed register on the 24th SCLK.

W/$\overline{R}$ Write/Read control
0 = Read register
1 = Write register

RA[4:0] Register address bits. Binary encoded 0 to 31. All registers are 24 bits in length.

Address	Name	Description
00000	Config	Configuration Register
00001	Ioff	Current offset calibration
00010	Ign	Current gain calibration
00011	Voff	Voltage offset calibration
00100	Vgn	Voltage gain calibration
00101	Cycle Count	Number of conversions to integrate over (N)
00110	Pulse-Rate	Used to calibrate/scale the energy to frequency output
00111	I	Last current value
01000	V	Last voltage value
01001	P	Last Power value
01010	E	Total energy value of last cycle
01011	I_{RMS}	RMS current value of last cycle
01100	V_{RMS}	RMS voltage value of last cycle
01101	TBC	Timebase Calibration
01110	Poff	Power Offset Register
01111	Status	Status Register
10000	I_{ACoff}	AC Current Offset Register
10001	V_{ACoff}	AC Voltage Offset Register
10010	Res	Reserved †
.		
.		
10111	Res	Reserved †
11000	Res	Reserved †
11001	Test	Reserved †
11010	Mask	Mask Register
11011	Res	Reserved †
11100	Ctrl	Control Register
11101	Res	Reserved †
.		
.		
11111	Res	Reserved †

† These Registers are for Internal Use only and should not be written to.

3.2 Serial Port Interface Pins

The CS5460A's serial interface consists of four control lines: $\overline{CS}$, SDI, SDO, and SCLK.

$\overline{CS}$, Chip Select, is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied to logic 0, the port can function as a three wire interface. SDI, Serial Data In, is the data signal used to transfer data to the converters.

SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1.

SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held at logic 0 before SCLK transitions can be recognized by the port logic. To accommodate opto-isolators SCLK is designed with a Schmitt-trigger input to allow an opto-isolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an opto-isolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.

3.3 Serial Read and Write

The state machine decodes the command word as it is received. Data is written to and read from the CS5460A by using the Register Read/Write command. Figure 9 illustrates the serial sequence necessary to write to, or read from the serial port's buffers. As shown in Figure 9, a transfer of data is always initiated by sending the appropriate 8-bit command (MSB first) to the serial port (SDI pin). It is important to note that some commands use information from the Cycle-Count Register and Configuration Register to perform the function. For those commands, it is important that the correct information is written to those registers first.

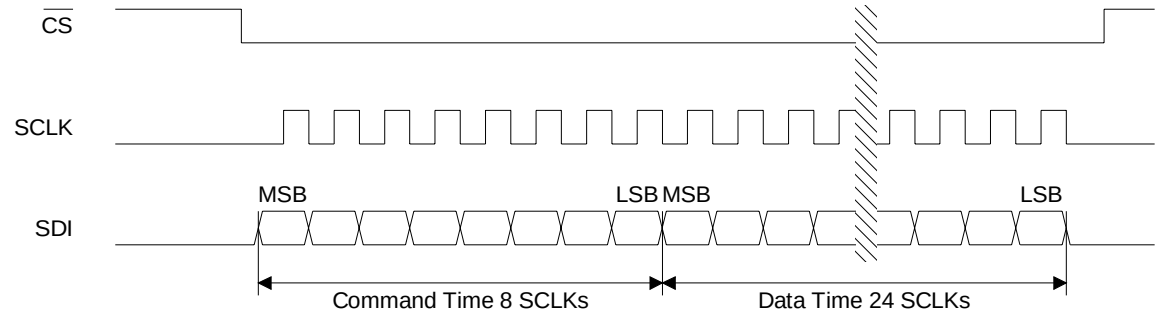
3.3.1 Register Write

Command words instructing a register write must be followed by 24 bits of data. For instance, to write the Configuration Register, the user would transmit the command (0x40) to initiate the write. The CS5460A will then acquire the serial data input from the (SDI) pin when the user pulses the serial clock (SCLK) 24 times. Once the data is received the state machine would write the data to the Configuration Register and return to the command mode.

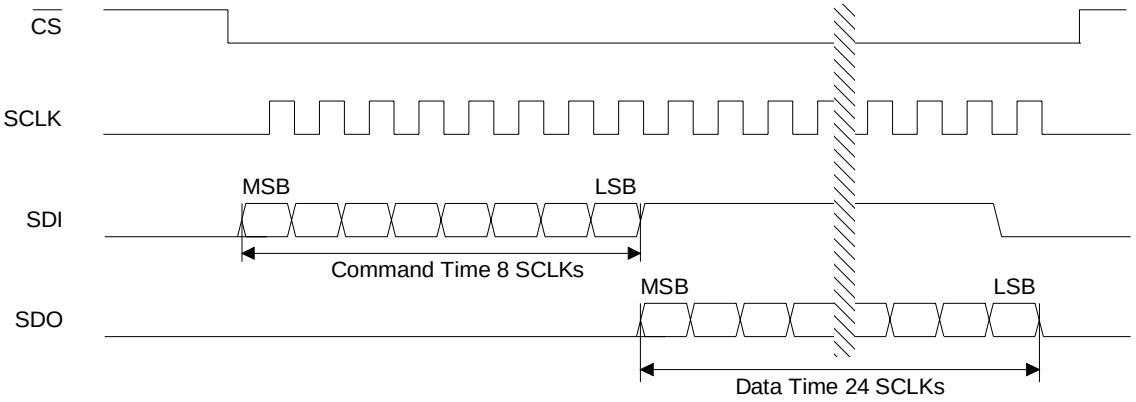
3.3.2 Register Read

Command words instructing a register read may be terminated at 8-bit boundaries (e.g., read transfers may be 8, 16, or 24 bits in length). Also data register reads allow "command chaining". For example, a command word instructs the state machine to read a signed output register. After the user pulses SCLK for 16-bits of data, a write command word (e.g., to clear the Status Register) may be pulsed on to the SDI line at the same time the remaining 8-bits of data are pulsed from the SDO line.

When a command involves a write operation, the serial port will continue to clock in the data bits (MSB first) on the SDI pin for the next 24 SCLK cycles. When a read command is initiated, the serial port will start transferring register content bits serial (MSB first) on the SDO pin for the next 8, 16, or 24 SCLK cycles depending on the command issued. The micro-controller is allowed to send a new command while reading register data. The new command will be acted upon immediately and could possibly terminate the register read. During the read cycle, the SYNC0 command (NOP) should be strobed on the SDI port while clocking the data from the SDO port.



Write Cycle



Read Cycle

Figure 9. Command and Data Word Timing

3.4 Serial Port Initialization

The serial port can be initialized to the command mode in several different ways. One of these is by issuing the serial port initialization sequence. The serial port initialization sequence involves clocking 3 (or more) SYNC1 command bytes (0xFF) followed by one SYNC0 command byte (0xFE). There are other valid ways to set the chip into command mode. For completeness, all of the possible initialization actions are listed here:

1) With power already on, issue Serial Port Initialization Sequence (described above). Or,
2) Power the chip on.
3) Wake the CS5460A out of Sleep Mode
4) Wake the CS5460A out of Stand-By Mode
5) Hardware Reset
6) Software Reset

Performing any of these actions will place the chip in the command mode, where it waits until a valid command is received.

3.5 System Initialization

A software or hardware reset can be initiated at any time. The software reset is initiated by writing a logic 1 to the RS (Reset System) bit in the configuration register, which automatically returns to logic 0 after reset. At the end of the 32nd SCLK (i.e., 8 bit command word and 24 bit data word) internal synchronization delays the loading of the configuration register by 3 or 4 DCLK (MCLK/K). Then the reset circuit initiates the reset routine on the 1st falling edge of MCLK.

A hardware reset is initiated when the $\overline{\text{RESET}}$ pin is forced low with a minimum pulse width of 50 ns. The $\overline{\text{RESET}}$ signal is asynchronous, requiring no MCLKs for the part to detect and store a reset event. The $\overline{\text{RESET}}$ pin is a Schmitt Trigger input, allows it to tolerate slow rise times and/or noisy control signals. (This can often turn out to be the case, after a power failure or brown-out on the power line.) Once the $\overline{\text{RESET}}$ pin is inactive, the internal reset circuitry remains active for 5 MCLK cycles to insure resetting the synchronous circuitry in the device. The modulators are held in reset for 12 MCLK cycles after $\overline{\text{RESET}}$ becomes inactive. After a hardware or software reset, the internal registers (some of which drive output pins) will be reset to their default values on the first MCLK received after detecting a reset event (see Table 2). The CS5460A will then wait for a valid command on the serial port.

The reader should refer to the section titled “Register Description” for a complete description of the registers listed in Table 2.

Configuration Register:	0x000001
Offset Register:	0x000000
Gain Registers	0x400000
Pulse-Rate Register:	0x0FA000
Cycle-Counter Register:	0x000FA0
Timebase Register:	0x800000
Status Register:	0x000000
Mask Register:	0x000000
Control Register:	0x000000
AC Current Offset Register:	0x000000
AC Voltage Offset Register:	0x000000
Power Offset Register:	0x000000
All Data Registers:	0x000000
All Unsigned Data Registers	0x000000

Table 2. Internal Registers Default Value

4. FUNCTIONAL DESCRIPTION

4.1 Pulse-Rate Output

As an alternative to reading the energy through the serial port, the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins provide a simple interface with which signed energy can be accumulated. Each $\overline{\text{EOUT}}$ pulse represents a predetermined magnitude of energy. The accompanying $\overline{\text{EDIR}}$ output represents the sign of the energy. With MCLK = 4.096 MHz, K = 1, the pulses will have an average frequency equal to the frequency setting in the Pulse Rate Register when the input levels into the voltage and current channels cause full-scale readings in the instantaneous voltage and current registers. When MCLK/K is not equal to 4.096 MHz, the user should scale the pulse-rate that one would expect to get with MCLK/K = 4.096 MHz by a factor of 4.096 MHz / (MCLK / K) to get the actual output pulse-rate.

EXAMPLE #1: Suppose that we want the pulse-frequency on the $\overline{\text{EOUT}}$ pin to be 'IR' = 100 pulses per second (100 Hz) when the RMS-voltage/RMS-current levels on the power line are 220 V and 15 A respectively, noting that the maximum rated levels on the power line are 250 V and 20 A. We also assume that we have calibrated the CS5460A voltage/current channel inputs such that a DC voltage level of 250 mV across the voltage/current channels will cause full-scale readings of 1.0 in the CS5460A Instantaneous Voltage and Current Registers as well as in the RMS-Voltage and RMS-Current Registers. We want to find out what frequency value we should put into the CS5460A's pulse-rate register (call this value 'PR') in order to satisfy this requirement. Our first step is to set the voltage and current sensor gain constants, K_V and K_I, such that there will be acceptable input voltage levels on the inputs when the power line voltage and current levels are at the maximum values of 250 V and 20 A, respectively. We need to calculate K_V and K_I in order to determine the appropriate ratios of the voltage/current transformers and/or shunt resistor values to use in the front-end voltage/current sensor networks.

We assume here that we are dealing with a sinusoidal AC power signal. For a sinewave, the largest RMS value that can be accurately measured (without over-driving the inputs) will register at ~0.7071 of the maximum DC input level. Since power signals are often not perfectly sinusoidal in real-world situations, and to provide for some over-range capability, we will set the RMS-Voltage and RMS-Current Registers to measure at 0.6 when the RMS-values of the line-voltage and line-current levels are at 250 V and 20 A. Therefore, when the RMS registers measure 0.6, the voltage level at the inputs will be 0.6 x 250 mV = 150 mV. We now find our sensor gain constants, K_V and K_I, by demanding that the voltage and current channel inputs should be at 150 mV RMS when the power line voltage and current are at the maximum values of 250 V and 20 A.

$$K_V = 150 \text{ mV} / 250 \text{ V} = 0.0006$$

$$K_I = 150 \text{ mV} / 20 \text{ A} = 0.0075 \text{ Ohms}$$

These sensor gain constants can help determine the ratios of the transformer or resistor-divider sensor networks. We now use these sensor gain constants to calculate what the input voltage levels will be on the CS5460A inputs when the line-voltage and line-current are at 220 V and 15 A. We call these values V_{Vnom} and V_{Inom}.

$$V_{Vnom} = K_V * 220 \text{ V} = 132 \text{ mV}$$

$$V_{Inom} = K_I * 15 \text{ A} = 112.5 \text{ mV}$$

The pulse rate on $\overline{\text{EOUT}}$ will be at 'PR' pulses per second (Hz) when the RMS-levels of voltage/current inputs are at 250 mV. When the voltage/current inputs are set at V_{Vnom} and V_{Inom}, we want the pulse rate to be at 'IR' = 100 pulses per second. IR will be some percentage of PR. The percentage is defined by the ratios of V_{Vnom}/250 mV and V_{Inom}/250 mV with the following formula:

$$\text{PulseRate} = \text{IR} = \text{PR} \cdot \frac{V_{Vnom}}{250\text{mV}} \cdot \frac{V_{Inom}}{250\text{mV}}$$

We can rearrange the above equation and solve for PR. This is the value that we put into the pulse-rate register.

$$\text{PR} = \frac{\text{IR}}{\frac{V_{Vnom}}{250\text{mV}} \times \frac{V_{Inom}}{250\text{mV}}} = \frac{100\text{Hz}}{\frac{132\text{mV}}{250\text{mV}} \times \frac{112.5\text{mV}}{250\text{mV}}}$$

Therefore we set the Pulse-Rate Register to ~420.875 Hz. Therefore, the Pulse-Rate Register would be set to 0x00349C.

The above equation is valid when current channel is set to x10 gain. If current channel gain is set to x50, then the equation becomes:

$$\text{PR} = \frac{\text{IR}}{\frac{V_{Vnom}}{250\text{mV}} \times \frac{V_{Inom}}{50\text{mV}}}$$

where it is assumed that the current channel has been calibrated such that the current-register will read at full-scale when the input voltage across the IIN+ and IIN- inputs is 50 mV (DC).

EXAMPLE #2: Suppose that instead of being given a desired frequency of pulses per second to be issued at a specific voltage/current level, we are given a desired number of pulses per unit energy to be present at $\overline{\text{EOUT}}$, given that the maximum line-voltage is at 250 V (RMS) and the maximum line-current is at 20 A (RMS). For example, suppose that the required number of pulses per kW-hr is specified to be 500 pulses/kW-hr. In such a situation, the nominal line voltage and current do not determine the appropriate pulse-rate setting. Instead, the *maximum* line-voltage and line-current levels must be considered. We use the given maximum line-voltage and line-current levels to determine K_V and K_I as previously described to get:

K_V = 150 mV / 250 V = 0.0006

K_I = 150 mV / 20 A = 0.0075 Ohms

where we again have calculated our sensor gains such that the maximum line-voltage and line-current levels will measure as 0.6 in the RMS-voltage and RMS-current registers.

We can now calculate the required Pulse-Rate Register setting by using the following equation:

$$\text{PR} = 500\frac{\text{pulses}}{\text{kW} \cdot \text{hr}} \cdot \frac{1\text{hr}}{3600\text{s}} \cdot \frac{1\text{kW}}{1000\text{W}} \cdot \frac{250\text{mV}}{K_V} \cdot \frac{250\text{mV}}{K_I}$$

Therefore PR = ~1.929 Hz.

Note that the Pulse-Rate Register cannot be set to a frequency of exact 1.929 Hz. The closest setting that the Pulse-Rate register can obtain is 0x00003E = 1.9375. To improve the accuracy, either gain register can be programmed to correct for the round-off error in PR. This value would be calculated as

$$\text{Ign or Vgn} = \frac{\text{PR}}{1.929} \cong 1.00441 = 0\text{x}404830$$

4.2 Multi-Phase Option for Pulse Output

To allow for a simpler interface in a multi-phase system, the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins can be connected together and used in a wire-AND configuration. In this type of operation, the EWA bit in the Configuration Register must be activated (set to 1), and the user must supply external pull-up devices in order to pull the wire-AND output to logic-high. See Figure 11. The parts must be driven with the same clock and programmed with different phases (see PH[1:0] bits in the Configuration Register). The pulse width and the pulse separation is an integer multiple of system clocks (approximately equal to 1/8 of the period of the contents of the pulse-rate register). The maximum frequency is therefore MCLK/K/8. A timing diagram for a multi-phase system is shown in Figure 10.

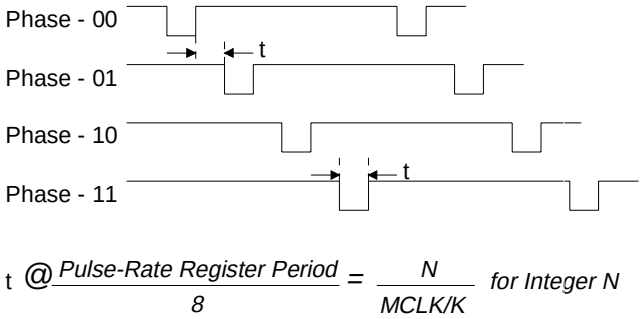


Figure 10. Multi-Phase System (Normal Mode only)

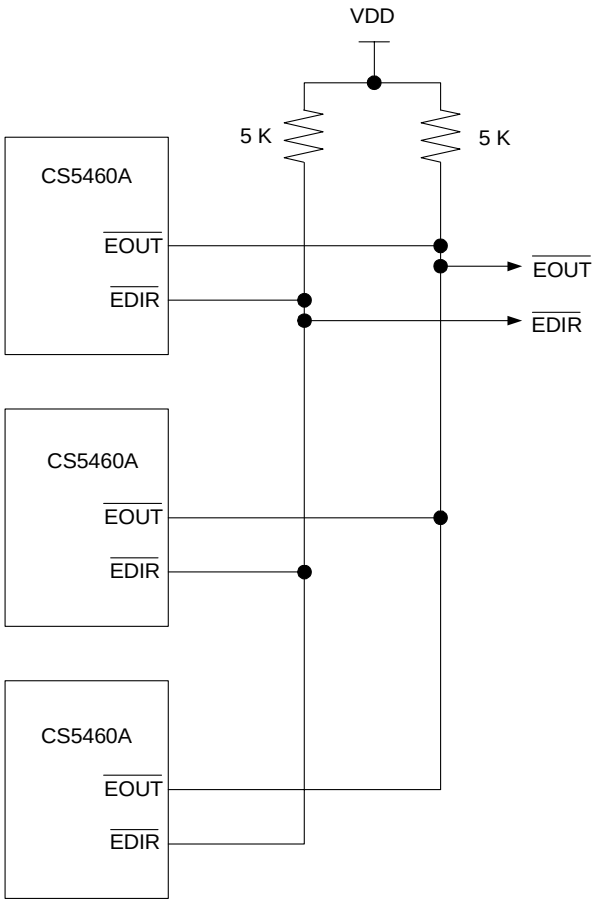


Figure 11. Option for wire and configuration of $\overline{\text{EOUT}}$ and EDIR pins for multi-phase metering

4.3 Pulse Output for Normal Mode, Stepper Motor Mode and Mechanical Counter Mode

The $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ output formats can be modified so that the time duration of the pulses is increased to the point that they can drive either an electro-mechanical counter or a stepper motor. These modes are controlled by setting certain bits in the Control Register.

4.3.1 Normal Mode

Referring to the description of the Control Register in *Section 5., REGISTER DESCRIPTION*, if both the MECH and STEP bits are set to '0', the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pulse outputs for a single CS5460A have the same format as the "Phase - 00" signal shown in Figure 10--active-low pulses with very short width. When energy is positive, $\overline{\text{EDIR}}$ is always high. When energy is negative, $\overline{\text{EDIR}}$ has the same output as $\overline{\text{EOUT}}$. When MCLK/K is not equal to 4.096 MHz, the user can predict the pulse-rate

4.3.2 Mechanical Counter Mode

Setting the MECH bit in the control register to '1' and the STEP bit to '0' enables wide stepping pulses for mechanical counters and similar appliances. In this mode, active-low pulses are 128 ms wide when using a 4.096 MHz crystal and K=1. When energy is positive, the pulses appear on $\overline{\text{EOUT}}$. When energy is negative, pulses appear on $\overline{\text{EDIR}}$. It is up to the user to insure that pulses will not occur at a rate faster than the 128 ms pulse duration, or faster than the mechanical counter can accommodate. The user must make sure that the Pulse-Rate Register is set to an appropriate value. Because the duration of each pulse is set to 128 ms, the maximum output pulse frequency is limited to ~7.8 Hz. (See Figure 12.) For values of MCLK / K different than 4.096 MHz, the duration of one pulse is (128 * 4.096 MHz)/(MCLK / K) milliseconds.

4.3.3 Stepper Motor Mode

Setting the STEP bit in the control register to '1' and the MECH bit to '0' transforms the EOUT and EDIR pins into two stepper motor phase outputs. When an energy pulse occurs, one of the outputs changes state. When the next energy pulse occurs, the other output changes state. The direction the motor will rotate is determined by the order of the state changes. When energy is positive, $\overline{\text{EOUT}}$ will lead $\overline{\text{EDIR}}$. When energy is negative, $\overline{\text{EDIR}}$ will lead $\overline{\text{EOUT}}$. See Figure 13.

4.4 Auto-Boot Mode Using EEPROM

The CS5460A has a MODE pin. When the MODE pin is set to logic low, the CS5460A is in normal operating mode, called *command mode*. This mode denotes the normal operation of the part, that

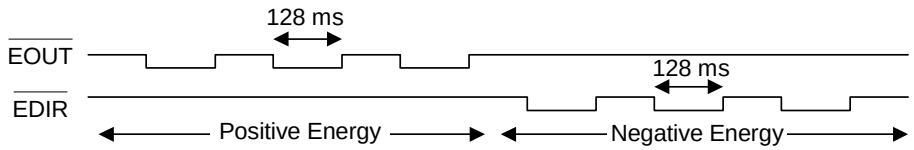


Figure 12. Mechanical Counter Mode on $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$

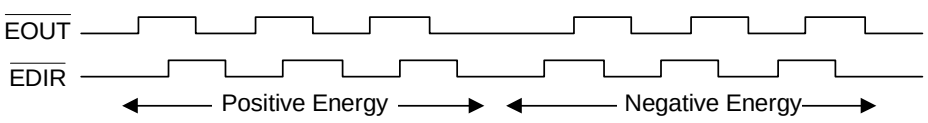


Figure 13. Stepper Motor Mode on $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$

has been described so far. But when this pin is set to logic high, the CS5460A *auto-boot mode* is enabled. In auto-boot mode, the CS5460A is configured to request a memory download from an external serial EEPROM. The download sequence is initiated by driving the /RESET pin to logic high. Auto-Boot mode allows the CS5460A to operate without the need for a microcontroller. Note that if the MODE pin is left unconnected, it will default to logic low because of an internal pull-down on the pin.

Figure 14 shows the typical connections between the CS5460A and a serial EEPROM for proper auto-boot operation. In this mode, /CS and SCLK are driven outputs. SDO is always an output. During the auto-boot sequence, the CS5460A drives /CS low, provides a clock output on SCLK, and drives out-commands on SDO. It receives the EEPROM data on SDI. The serial EEPROM must be programmed with the user-specified commands and register data that will be used by the CS5460A to initialize and begin conversions.

Figure 14 also shows the external connections that would be made to a calibrator device, such as a PC or custom calibration board. When the metering system is installed, the calibrator would be used to control calibration and/or to program user-specified commands and calibration values into the EEPROM. The user-specified commands/data will determine the CS5460A's exact mode of operation once the auto-boot sequence is initiated. Any of the valid commands can be used. For example, the EEPROM can be programmed so that it would first send out commands that write calibration values to the calibration registers inside the CS5460A, then it could enable the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ functionality and set a Pulse-Rate Register value. Finally, the code can send out the commands to initiate continuous conversions, and to set the pulse-output mode to specific format (e.g., set the MECH bit in the Control Register). The serial data for such a sequence is shown below in single-byte hexidecimal notation:

```
40 00 00 61     ;In configuration Register, turn high-pass filters on, set K = 1.
44 7F C4 A9     ;Write value of 0x7FC4A9 to Current Gain Register.
46 7F B2 53     ;Write value of 0xFFB253 to DC Voltage Offset Register.
4C 00 00 14     ;Set Pulse Rate Register to 0.625 Hz.
```

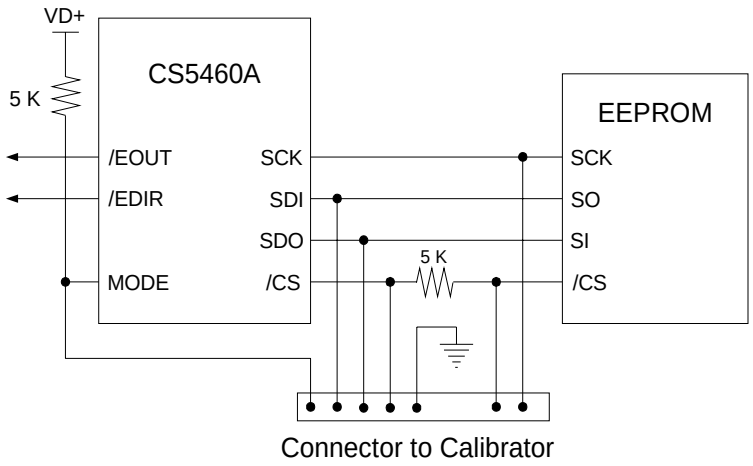


Figure 14. Typical Interface of EEPROM to CS5460A

E8	;Start continuous conversions.
78 00 01 40	;Write stop bit to CS5460A to terminate auto-boot sequence, and set the $\overline{\text{EOUT}}$ pulses to Mechanical Counter Mode.

This data from the EEPROM will drive the SDI pin of the CS5460A during the auto-boot sequence.

The following sequence of user-controlled events will cause the CS5460A to enter auto-boot mode: (A simple timing diagram for this sequence is shown below in Figure 15.) After the CS5460A has been powered on and has been allowed to initialize, if the MODE pin is set to logic high, then changing the /RESET pin from active state to inactive state (low to high) will cause CS5460A to bring the /CS pin low, and then issue the standard block read command out of the SDO line. Then the CS5460A will continue to issue SCLKs, to accept data from the EEPROM. A more detailed timing diagram can be found in the *SWITCHING CHARACTERISTICS* section of this data sheet.

Several industry-standard serial EEPROMs that will successfully run auto-boot with the CS5460A are listed below:

- Atmel

  AT25010
  AT25020
  AT25040

- National Semiconductor

  NM25C040M8
  NM25020M8

- Xicor

  X25040SI

These types of serial EEPROMs expect a specific 8-bit command word (00000011) in order to perform a memory download. The CS5460A has been hardware programmed to transmit this 8-bit command word to the EEPROM at the beginning of the auto-boot sequence.

The auto-boot sequence is terminated by writing a '1' to the STOP bit in the CS5460A's Control Register. This action is performed as the last command in the EEPROM command sequence. Once this event occurs, SCLK stops, and /CS rises, thereby reducing power consumed by the EEPROM. When the CS5460A is commanded by the EEPROM to perform a certain operation, it will continue to execute that operation after the STOP bit has been received. In the above example, the 'continuous conversion' command (0xE8) is issued from the EEPROM, and therefore the CS5460A will continue performing conversions even after the STOP bit is written.

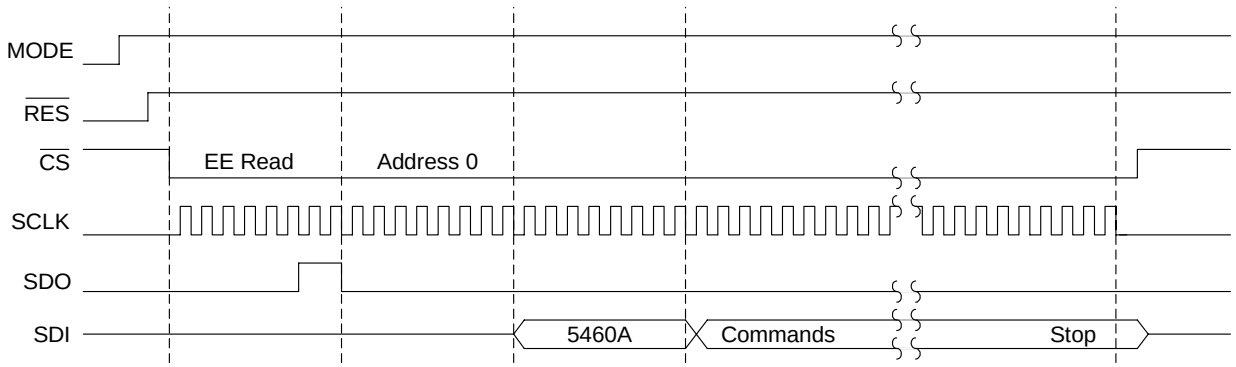


Figure 15. Timing Diagram for Auto-Boot Sequence

4.5 Interrupt and Watchdog Timer

4.5.1 Interrupt

The $\overline{\text{INT}}$ pin is used to indicate that an event has taken place in the converter that needs attention. These events inform the system about operation conditions and internal error conditions. The $\overline{\text{INT}}$ signal is created by combining the Status register with the Mask register. Whenever a bit in the Status register becomes active, and the corresponding bit in the Mask register is a logic 1, the $\overline{\text{INT}}$ signal becomes active. The interrupt condition is cleared when the bits of the Status Register are returned to their inactive state.

4.5.1.1 Clearing the Status Register

Unlike the other registers, the bits in the Status Register can only be cleared (set to logic 0). When a word is written to the Status Register, any 1s in the word will cause the corresponding bits in the Status Register to be cleared. The other bits of the Status Register remain unchanged. This allows the clearing of particular bits in the register without having to know the state of the other bits. This mechanism is designed to facilitate handshaking and to minimize the risk of losing events that haven't been processed yet.

4.5.1.2 Typical use of the $\overline{\text{INT}}$ pin

The steps below show how interrupts can be handled.

- *Initialization*:

  Step I0 - All Status bits are cleared by writing FFFFFF (Hex) into the Status Register.

  Step I1 - The conditional bits which will be used to generate interrupts are then written to logic 1 in the Mask register.

  Step I3 - Enable interrupts.

- *Interrupt Handler Routine*:

  Step H0 - Read the Status Register.

  Step H1 - Disable all interrupts.

  Step H2 - Branch to the proper interrupt service routine.

  Step H3 - Clear the Status Register by writing back the value read in step H0.

  Step H4 - Re-enable interrupts.

  Step H5 - Return from interrupt service routine.

  This handshaking procedure insures that any new interrupts activated between steps H0 and H3 are not lost (cleared) by step H3.

4.5.1.3 $\overline{\text{INT}}$ Active State

The behavior of the $\overline{\text{INT}}$ pin is controlled by the SI1 and SI0 bits of the configuration register. The pin can be active low (default), active high, active on a return to logic 0 (pulse-low), or active on a return to logic 1 (pulse-high).

4.5.1.4 Exceptions

The $\overline{\text{IC}}$ (Invalid Command) bit of the Status Register can only be cleared by performing the port initialization sequence. This is also the only Status Register bit that is active low.

To properly clear the WDT (WatchDog Timer) bit of the Status Register, first read the Energy Register, then clear the bit in the Status Register.

4.5.2 Watch Dog Timer

The Watch Dog Timer (WDT) is provided as means of alerting the system that there is a potential breakdown in communication with the micro-controller. By allowing the WDT to cause an interrupt, a controller can be brought back, from some unknown code space, into the proper code for processing the data created by the converter. The time-out is preprogrammed to approximately 5 seconds. The countdown restarts each time the Energy register is read. Under typical situations, the Energy register is read every second. As a result, the WDT will not time out. Other applications that use the watchdog timer will need to ensure that the En-

ergy register is read at least once in every 5 second span.

4.6 Oscillator Characteristics

XIN and XOUT are the input and output, respectively, of an inverting amplifier to provide oscillation and can be configured as an on-chip oscillator, as shown in Figure 16. The oscillator circuit is designed to work with a quartz crystal or a ceramic resonator. To reduce circuit cost, two load capacitors C1 are integrated in the device, one between XIN and DGND, one between XOUT and DGND. Lead lengths should be minimized to reduce stray capacitance. With these load capacitors, the oscillator circuit is capable of oscillation up to 20 MHz. To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS level signals. This amplifier works with sinusoidal inputs so there are no problems with slow edge times.

The CS5460A can be driven by a clock ranging from 2.5 to 20 MHz. The user must appropriately set the K divider value such that the internal DCLK will run somewhere between 2.5 MHz and 5 MHz. The K divider value is set with the K[3:0] bits in the Configuration Register. As an example, if XIN = MCLK = 15 MHz, and K is set to 5, then DCLK is 3 MHz, which is a valid value for DCLK. Note that if the K[3:0] bits are all set to zero, the value of the K divider value is 16.

4.7 Analog Inputs

The CS5460A accommodates a full scale range of 150 mV_{RMS} on both input channels. System calibration can be used to increase or decrease the full scale span of the converter as long as the calibration register values stay within the limits specified. See *Section 4.9, Calibration*, for more details.

The current input channel has an input range of 30 mV_{RMS} when the internal x50 gain stage is enabled. This signal range is designed to handle low level signals from a shunt sensor.

4.8 Voltage Reference

The CS5460A is specified for operation with a +2.5 V reference between the VREFIN and VA- pins. The converter includes an internal 2.5 V reference (60 ppm/°C drift) that can be used by connecting the VREFOUT pin to the VREFIN pin of the device. If higher accuracy/stability is required, an external reference can be used.

4.9 Calibration

4.9.1 Overview of Calibration Process

The CS5460A offers AC or DC calibration. The user decides which calibration is being performed by setting/clearing one or more of the 8 bits in the Calibration command word. Regardless of whether an AC or DC calibration is desired, there are two calibration modes: system offset and system gain. During calibration, the user must supply the input calibration signals to the "+" and "-" pins of the voltage-/current-channel input. These input calibration signals represent full-scale and ground input levels. Whether it is AC or DC calibration, the user must provide the positive full-scale reference signals to perform a system gain calibration, and a

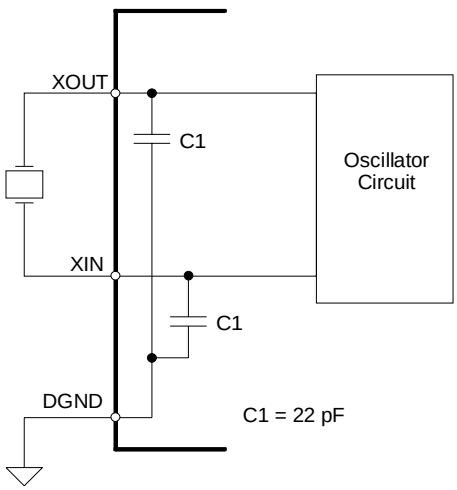


Figure 16. Oscillator Connection

ground-referenced signal to perform a system offset calibration. The differential voltage levels of the user-provided calibration signals must be within the specified voltage input limits (refer to "Differential Input Voltage Range" in *Section 1., Characteristics and Specifications*). The voltage level of these calibration input signals must be within the specified calibration limits for each specific calibration step and channel.

4.9.2 The Calibration Registers

Since both the voltage and current channels have separate offset and gain registers associated with them, the system offset or system gain can be performed on either channel without the calibration results from one channel affecting the other. Referring to Figure 6, it is important to note that for both the voltage channel and current channel, there are separate calibration registers for the AC and DC offset corrections. This is not true for gain corrections, as there is only one gain register per channel--AC and DC gain calibration results are stored in the same register. The results in the gain registers reflect either the AC or DC gain calibration results, whichever was performed most recently. Both a DC and AC offset can be applied to the system at the same time, but only one gain calibration can be applied to the system. The user must decide which type of gain calibration will be used: AC or DC, but not both. Therefore, the following six registers exist:

- Voltage Gain Register
- Current Gain Register
- DC Voltage Offset Register
- DC Current Offset Register
- AC Voltage Offset Register
- AC Current Offset Register

Referring to Figure 6, one should note that the AC Offset Registers affect the output results differently than the DC Offset Registers. The DC offset values are applied to the voltage/current signals very early in the signal path, and so the DC Offset Register value affects all CS5460A results. This is not true for the AC Offset. The AC Offset Registers only affect the results of the rms-voltage/rms-current calculations.

4.9.3 Calibration Sequence

The basic flow of the calibration sequence is to first apply the appropriate calibration signals to the "+" and "-" pins of the voltage/current channel inputs, and then the user must send the appropriate calibration command to the CS5460A. The calibration command is an 8-bit command. Various bits within this command specify the exact type of calibration that is to be performed (e.g., AC gain cal for voltage channel, DC offset cal for current channel, etc.) After the CS5460A is finished running its internal calibration, and storing the results in the appropriate calibration registers, the DRDY bit is set (in the Status Register) to indicate that the calibration sequence has been completed.

Note that when the calibration command is sent to the CS5460A by the user, the device should NOT be running in conversion mode. The calibration will not run if the part is already running in either of the two available conversion modes.

Figure 17 shows the basic setup for gain calibration. If a DC gain calibration is desired, the user should apply a DC voltage level that truly represents the *absolute maximum* voltage level that will be needs to be measured across the inputs.a DC voltage level that represents the desired absolute peak full-scale value. However, in many practical power metering situations, an AC signal is preferred over a DC signal to calibrate the gain. If the user decides to perform AC gain calibration instead of DC, the user should apply an AC reference signal that is set to the desired maximum RMS level. In general, the RMS level of the AC gain calibration signals will need to be significantly lower than the maximum output value of the instantaneous

voltage and current registers in order to avoid clipping the signals when they reach their maximum peak value. For example, the largest sinusoid that can be used in AC calibration is one whose RMS-value is ~0.7071 of the value of the peak DC input voltage value.

For the offset configuration, there is no difference between the AC and DC calibration signals, as the user should simply ground the voltage-/current-channel input(s) during this calibration. (See Figure 18.)

The user should not try to run both an offset and gain calibration at the same time. This will cause undesirable calibration results.

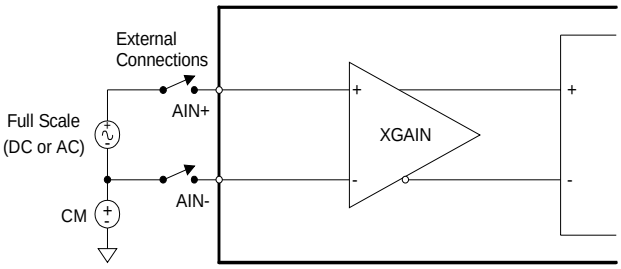


Figure 17. System Calibration of Gain.

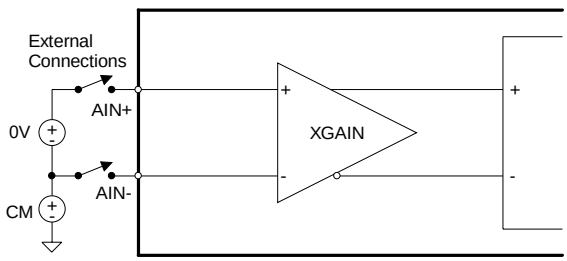


Figure 18. System Calibration of Offset.

4.9.4 Duration of Calibration Sequence

The value of the Cycle Count Register (N) determines the number of conversions averaged to obtain the calibration results. When N is increased by the user, the accuracy of the calibration results will increase. For DC offset/gain calibrations, the calibration sequence always takes at least N + 30 conversion cycles to complete. For AC offset/gain calibrations, the calibration sequence takes at least 6N + 30 A/D conversion cycles to complete, (about 6 computation cycles). For all calibrations (AC or DC), once a calibration cycle is complete, the DRDY bit is set and the results are stored in either the gain or offset registers.

4.9.5 Description of Calibration Algorithms

The algorithms for the AC and DC calibrations are shown in Figure 19. This figure applies to both the voltage channel and the current channel. The following descriptions of calibration algorithms will focus on the voltage channel, but apply equally to the current channel.

The AC voltage gain calibration algorithm attempts to adjust the voltage gain register value so that the calibration reference signal level presented at the voltage inputs will result in a value of 0.6 in the RMS-voltage register. The level of the calibration signal is determined by the user. During AC voltage gain calibration, the value in the RMS-voltage register is divided into 0.6. This result is the AC gain calibration value, stored in the gain register.

Note: For proper calibration, it is assumed that the value of the Voltage/Current Gain Registers are set to 1.0 before running the *gain* calibration(s), and the value in the AC and DC *Offset* Registers is set to 0 before running calibrations. This can be accomplished by a software or hardware reset of the device. The values in the Voltage/Current Gain Registers do affect the results of the AC/DC gain calibrations.

The idea of the AC offset calibration is to obtain an offset value that reflects the square of the RMS output level when the inputs are grounded. During normal operation, when the CS5460A is calculating the latest result for the RMS-Voltage Register, this AC offset register value will be subtracted from the square of each successive voltage sample in order to nullify the AC offset that may be inherent in the voltage-channel signal path. Note that the value in the AC offset register is proportional to the *square* of the AC offset. First, the inputs should be grounded by the user, and then the AC offset calibration command should be sent to the CS5460A. When the AC offset calibration sequence is initiated by the user, the most recent RMS-Voltage Register result is squared. This value is then subtracted from the square of each voltage sample that comes through the RMS data path. See Figure 19.

After the user-provided calibration voltage has been applied to the inputs, the CS5460A determines the DC Gain Register value by averaging the output signal values over one computation cycle (N samples) and then dividing this average into 1. Therefore, after the DC voltage gain calibration has been executed, the instantaneous voltage register will read at full-scale when the DC level of the input signal is equal to the level of the DC calibration signal that was applied to the voltage channel inputs during the DC gain calibration. For example, if a 240 mV DC signal is applied to the voltage channel inputs during the DC gain calibration for the current channel, then the Instantaneous Voltage Register will measure at unity whenever a 240 mV DC level is applied to the voltage channel inputs.

The DC offset register holds the negative of the simple average of N samples taken while the DC calibration was executed. The inputs should be grounded during DC offset calibration. The DC offset value is added to the signal path to nullify the DC offset in the system.

4.9.6 Is Calibration Required?

The CS5460A does not *have* to be calibrated. After the part is reset or powered on, the device is functional and can perform measurements without being calibrated. The output register values will be affected by the default values of the on-chip registers (Gain = 1.0, DC Offset = 0.0, AC Offset = 0). Although the device can be used without performing an offset or gain calibration, the accuracy and linearity specs of the CS5460A will not be valid until after a gain/offset calibration is performed. Note that the 0.1% linearity specs in this data sheet assume that the device has been calibrated with MCLK = 4.096 MHz, K = 1, and N = 4000.

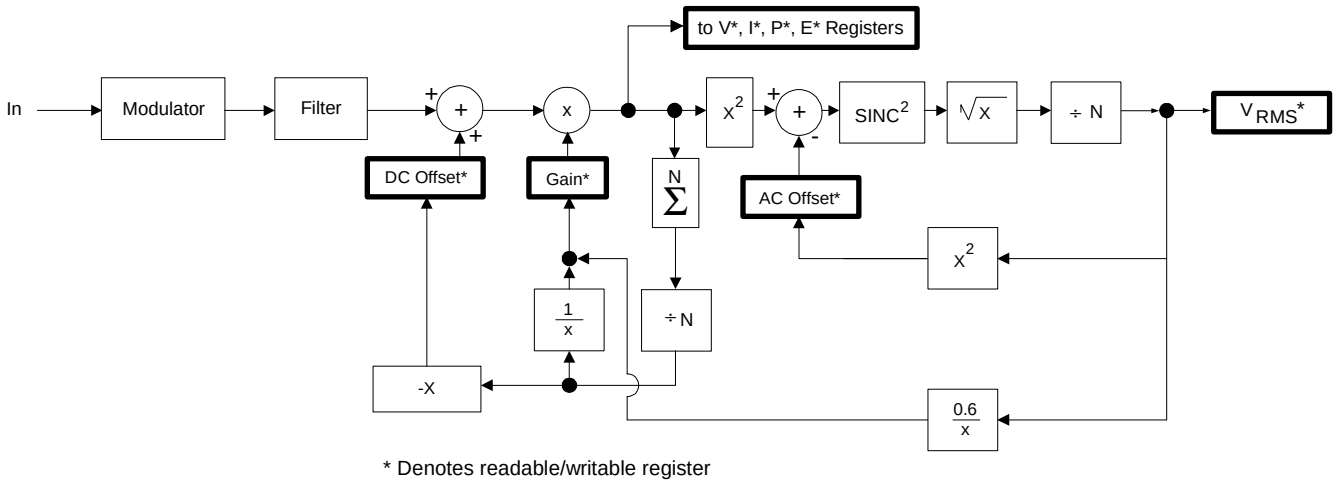


Figure 19. Calibration Data Flow

4.9.7 Calibration Tips

To minimize digital noise, the user should wait for each calibration step to be completed before reading or writing to the serial port.

After a calibration is performed, the offset and gain register contents can be read and stored externally. by the system micro-controller and recorded in memory. The same calibration words can be uploaded into the offset and gain registers of the converters when power is first applied to the system, or when the gain range on the current channel is changed.

An offset calibration should be performed before a gain calibration. Each gain calibration depends on the zero calibration point obtained from the offset calibration.

4.10 Phase Compensation

Bits 23 to 17 of the Configuration Register are used to program the amount of phase delay that is added to the voltage channel signal path. This phase delay is applied to the voltage channel signal in order to compensate for phase delay that is may be introduced by the user-supplied voltage and current sensor circuitry, which is external to the CS5460A. Voltage and current transformers, as well as other sensor equipment applied to the front-end of the CS5460A inputs can often introduce a phase delay in the system, which distorts the phase relationship between the voltage and current signals that are to be measured. The user can set the phase compensation bits to nullify this undesirable phase distortion between the two channels.

The CS5460A does not provide automatic phase calibration. The user must determine the phase compensation empirically. The default value of the phase compensation bits is 0000000. With this default setting, the phase delay on the voltage channel is ~0.0215 degrees (assuming a 60 Hz power signal). Note that the 7-bit phase compensation word is a 2's complement binary number. With MCLK = 4.096 MHz and K=1, the range of the internal phase compensation ranges from -2.8 degrees to +2.8 degrees when the input voltage/current signals are at 60 Hz. In this condition, each step of the phase compensation register (value of one LSB) is ~0.04 degrees. For values of MCLK other than 4.096 MHz, these values for the span (-2.8 to +2.8 degrees) and for the step size (0.04 degrees) should be scaled by 4.096 MHz / (MCLK / K). For power line frequencies other than 60Hz (e.g., 50 Hz), the user can predict the values of the range and step size by converting the above values to time-domain, and then computing the new range and step size in terms of degrees with respect to the new line frequency.

To calibrate the phase delay, the user may try adjusting the phase compensation bits while the CS5460A is in normal continuous conversion mode. Before doing so, the user should provide a purely resistive load (no inductance or capacitance) to the power line, such that nominal-level voltage and current signals from the power line are sensed into the voltage and current channels of the CS5460A. In this condition, any phase delay between the measured voltage and current signals is due only to phase delay introduced by the user's external voltage/current sensor circuitry. The objective is to adjust the phase compensation bits until the Energy Register value is maximized.

4.11 Time-Base Calibration Register

The Time-Base Calibration Register (notated as "TBC" in Figure 6) is used to compensate for slight errors in the XIN frequency. External oscillators and crystals have certain tolerances. If the user is concerned about improving the accuracy of the clock for energy measurements, the Time-Base Calibration Register can be manipulated to compensate for the frequency error. Note from Figure 6 that the TBC Register only affects the value in the Energy Register.

As an example, if the desired XIN frequency is 4.096 MHz, but the crystal is measured to actually be 4.091 MHz. The ratio of the desired frequency to the actual frequency is 4.096 MHz/4.091 MHz = ~1.00122219506. The TBC Register can be set to 1.0012223364 = 0x80280C(h), which is very close to the desired ratio.

4.12 Power Offset Register

Referring to Figure 6, note the P_{off} Register that appears just after the power computation. This register can be used to offset system power sources that may be resident in the system, but do not originate from the power line signal. These sources of extra energy in the system contribute undesirable and false offsets to the power/energy measurement results. For example, when a voltage signal is applied to the voltage channel inputs and the current channel has no line current, the current channel may still register a very small amount of current. This current measurement is cause by leakage of the voltage channel input signal into the current channel input signal path. The user can experimentally determine the amount of stray power that might be induced into the input pins, and then program the Power Offset Register to nullify the effects of this unwanted energy.

4.13 Input Protection and Filtering

In Figure 4 and Figure 5, note the series resistor RP_I which is connected to the IIN+ input pin. This resistor is used to provide current-limit protection for the current-channel input pin in the event of a power surge or lightening surge. The voltage/current-channel inputs have surge-current limits of 100 mA. This applies to brief voltage/current spikes (<500 msec). The limit is 10 mA for DC input overload situations.

The VIN+ pin does not need a protection resistor for the configurations shown in Figure 4 and Figure 5. This is because a resistive voltage-divider is used as the sensor, and so series resistance is already provided to the VIN+ input pin. In Figure 5, if a voltage transformer is used as the voltage sensor, then a resistor RP_V should be installed in series with the VIN+ pin.

Figure 4 shows how the analog inputs are connected for a common-mode configuration. Figure 5 shows a differential configuration. A differential input configuration can be used, because the voltage/current channel inputs are able to accept input voltage levels all the way down to -250 mV below the potential of the VA- pin (which is normally connected to ground). Note that a differential configuration could have been used in Figure 4, and a common-mode input configuration could have been used in Figure 5. If the negative sides of the CS5460A input channels are not grounded (i.e., if VIN- and IIN- are connected in a differential configuration) then it is appropriate to put protection resistors on these inputs as well (see Figure 5). In fact, even in the common-mode configuration, protection resistors and filter caps may be placed on the VIN- and IIN- inputs in order to provide a more balanced configuration, to improve common-mode rejection of very high-frequency EMI.

Capacitors CP_V and CP_I should be included to provide for attenuation of high-frequency noise that may be coupled into the input lines. In differential input configurations, such a capacitor should be added to the VIN- and IIN- pins in addition to the VIN+ and IIN+ pins. These capacitors should be placed in close proximity to the input pins for optimal protection against EMI.

Values for $RP_{V/I}$ and $CP_{V/I}$ must be chosen with the approximate input lowpass cutoff frequency in mind. In general, the cutoff frequency should not be less than 10 times the roll-off frequencies of the internal voltage/current channel filters (see Figure 7 and Figure 8). From these figures we see that the internal voltage channel roll-off is at ~1400 Hz while the current channel roll-off is at ~1600 Hz. If the cutoff frequency of the external

protection is much less than 10x these values (14000 Hz and 16000 Hz), then some of the harmonic content that may be present in the voltage/current signals may start to get attenuated by this input filtering, which is undesirable.

The exact values of $RP_{V/I}$ and $CP_{V/I}$ must be calculated for each particular application. The primary goal is to make sure that the input pins never receive transient input currents greater than 100 mA. Also, they should never be exposed to DC currents greater than 10 mA. The user-supplied protection resistors RP_V and RP_I will limit the current that comes into the pins in over-voltage situations--when the internal protection diodes turn on inside the CS5460A. For example, suppose that the value for RP_I (on the current channel input) was chosen to be 1000 Ohms. Then we know that the current channel can withstand brief voltage spikes of up to ~100 V (referenced to GND) without damage to the part. This is because 100 V / 1000 Ohm = 100 mA. The pin will also be protected for up to ~10 VDC, as we see that 10V / 1000 Ohm = 10 mA.

When computing appropriate values for $RP_{V/I}$, the differential input impedance of the CS5460A's voltage channel and current channel should also be considered. This is especially true for the current channel, which has a lower differential input impedance than the voltage channel. These impedance specs are given at the beginning of this data sheet (see the specification titled "Effective Input Impedance" for the voltage and current channels). For example, the differential input impedance in the current channel is spec'd to be 30 kOhm. As the user increases the value of RP_I to provide for more and more common-mode surge protection, the voltage drop across the external protection resistor increases, and it divides the input signal down more and more. This in turn reduces the dynamic range of the signals that are ultimately presented to the CS5460A's inputs. This voltage division by the protection resistors can sometimes by minimized, or even totally avoided: When possible, the user should first consider the input protection that is going to be necessary, and then determine the sensor gains such that the drop across the protection resistors is taken into account.

Typical values for these components are RP_I = 500 Ohm, CP_I = 0.02 uF, CP_V = 0.002 uF and if necessary, RP_V = 5 kOhm.

4.14 PCB Layout

The CS5460A should be placed entirely over an analog ground plane with both the VA- and DGND pins of the device connected to the analog plane. Place the analog-digital plane split immediately adjacent to the digital portion of the chip.

Note: See the CDB5460 data sheet for suggested layout details and Applications Note 18 for more detailed layout guidelines. Before layout, please call for our Free Schematic Review Service.

5. REGISTER DESCRIPTION

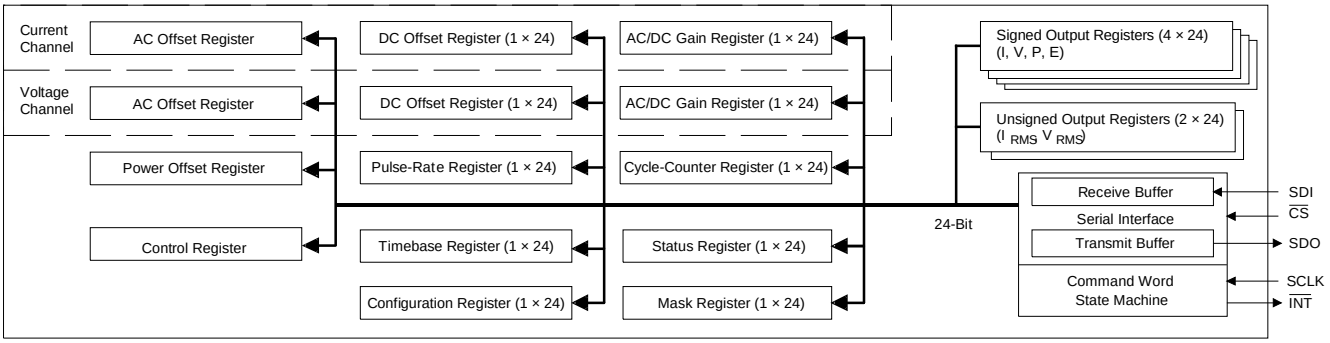


Figure 20. CS5460A Register Diagram

Note: 1. ** "default" => bit status after software or hardware reset

2. Note that all registers can be read from, and written to.

5.1 Configuration Register

Address: 0

23	22	21	20	19	18	17	16
PC6	PC5	PC4	PC3	PC2	PC1	PC0	Gi
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EWA	PH1	PH0	SI1	SI0	EOD	DL1	DL0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RS	VHPF	IHPF	iCPU	K3	K2	K1	K0

Default** = 0x000001

K[3:0] Clock divider. A 4 bit binary number used to divide the value of MCLK to generate the internal clock DCLK. The internal clock frequency is DCLK = MCLK/K. The value of K can range between 1 and 16. Note that a value of "0000" will set K to 16 (not zero).

iCPU Inverts the CPUCLK clock. In order to reduce the level of noise present when analog signals are sampled, the logic driven by CPUCLK should not be active during the sample edge.
0 = normal operation (default)
1 = minimize noise when CPUCLK is driving rising edge logic

IHPF Control the use of the High Pass Filter on the Current Channel.
0 = High-pass filter is disabled. If VHPF is set, use all-pass filter. Otherwise, no filter is used. (default)
1 = High-pass filter is enabled.

VHPF Control the use of the High Pass Filter on the voltage Channel.
0 = High-pass filter is disabled. If IHPF is set, use all-pass filter. Otherwise, no filter is used. (default)
1 = High-pass filter enabled

RS — Start a chip reset cycle when set 1. The reset cycle lasts for less than 10 XIN cycles. The bit is automatically returned to 0 by the reset cycle.

DL0 — When EOD = 1, $\overline{\text{EDIR}}$ becomes a user defined pin. DL0 sets the value of the $\overline{\text{EDIR}}$ pin. Default = '0'

DL1 — When EOD = 1, $\overline{\text{EOUT}}$ becomes a user defined pin. DL1 sets the value of the $\overline{\text{EOUT}}$ pin. Default = '0'

EOD — Allows the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins to be controlled by the DL0 and DL1 bits. $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ can also be accessed using the Status Register.
0 = Normal operation of the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins. (default)
1 = DL0 and DL1 bits control the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins.

SI[1:0] — Soft interrupt configuration. Select the desired pin behavior for indication of an interrupt.
00 = active low level (default)
01 = active high level
10 = falling edge (INT is normally high)
11 = rising edge (INT is normally low)

PH[1:0] — Set the phase of the EOUT and EDIR output pin pulse. The EOUT and EDIR pins, on different phases, can be wire-ANDed together as a simple way of summing the frequency of different parts.
00 = phase 0 (default)
01 = phase 1
10 = phase 2
11 = phase 3

Note: The above pulse-phase settings for multi-phase metering are intended for use in Normal Mode only, NOT intended for use in Stepper Mode and Mechanical Counter Mode.

EWA — Allows the output pins of $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ of multiple chips to be connected in a wire-AND, using an external pull-up device.
0 = normal outputs (default)
1 = only the pull-down device of the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins are active

Gi — Sets the gain of the current PGA
0 = gain is 10 (default)
1 = gain is 50

PC[6:0] — Phase compensation. A 2's complement number used to set the delay in the voltage channel. When MCLK=4.096 MHz and K=1, the phase adjustment range is about -2.8 to +2.8 degrees and each step is about 0.04 degrees (this assumes that the power line frequency is 60 Hz). If (MCLK / K) is not 4.096 MHz, the values for the range and step size should be scaled by the factor 4.096MHz / (MCLK / K).
Default setting is 0000000 = 0.0215 degrees phase delay (when MCLK = 4.096 MHz).

5.2 DC Current Offset Register and DC Voltage Offset Register

Address: 1 (DC Current Offset Register)
3 (DC Voltage Offset Register)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 0.000

The DC Offset Registers are initialized to zero on reset, allowing the device to function and perform measurements. The register is loaded after one computation cycle with the current or voltage offset when the proper input is applied and the DC Calibration Command is received. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. The value is in the range ± full scale. The numeric format of this register is two's complement notation.

5.3 AC/DC Current Gain Register and AC/DC Voltage Gain Register

Address: 2 (Current Gain Register)
4 (Voltage Gain Register)

MSB														LSB
2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default** = 1.000

The Gain Registers are initialized to 1.0 on reset, allowing the device to function and perform measurements. The Gain Registers hold the result of either the AC or DC gain calibrations, whichever was most recently performed. If DC calibration is performed, the register is loaded after one computation cycle with the system gain when the proper DC input is applied and the Calibration Command is received. If AC calibration is performed, then after ~(6N + 30) A/D conversion cycles (where N is the value of the Cycle-Count Register) the register(s) is loaded with the system gain when the proper AC input is applied and the Calibration Command is received. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. The value is in the range $0.0 \leq \text{Gain} < 4.0$.

5.4 Cycle Count Register

Address: 5

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default** = 4000

The Cycle Count Register determines the length of an energy and RMS conversion. A conversion cycle is derived from (MCLK/K)/(1024∗N) where MCLK is master clock, K is clock divider, and N is cycle count. N must be greater than 10 for I_{RMS}, V_{RMS} and energy calculations to be performed.

5.5 Pulse-Rate Register

Address: 6

MSB															LSB
2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	.....	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}

Default** = 32000.00Hz

The Pulse-Rate Register determines the frequency of the train of pulses output on the $\overline{EOUT}$ pin. Each $\overline{EOUT}$ pulse represents a predetermined magnitude of energy. The register's smallest valid value is 2^{-4} but can be in 2^{-5} increments.

5.6 I,V,P,E Signed Output Register Results

Address: 7 - 10

MSB															LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

The Signed Registers contain the last value of the measured results of I, V, P, and E. The results are in the range of $-1.0 \le I, V, P, E < 1.0$. The value is represented in two's complement notation, with the binary point place to the right of the MSB (which is the sign bit). I, V, P, and E are output results registers which contain signed values. Note that the I, V, and P registers are updated every conversion cycle, while the E register is only updated after each computation cycle. The numeric format of this register is two's complement notation.

5.7 I_{RMS}, V_{RMS} Unsigned Output Register Results

Address: 11,12

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

The Unsigned Registers contain the last value of the calculated results of I_{RMS} and V_{RMS}. The results are in the range of $0.0 \le I_{RMS}, V_{RMS} < 1.0$. The value is represented in binary notation, with the binary point place to the left of the MSB. I_{RMS} and V_{RMS} are output result registers which contain unsigned values.

5.8 Timebase Calibration Register

Address: 13

MSB															LSB
2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 1.000

The Timebase Register is initialized to 1.0 on reset, allowing the device to function and perform computations. The register is user loaded with the clock frequency error to compensate for a gain error caused by the crystal/oscillator tolerance. The value is in the range $0.0 \le TBC < 2.0$.

5.9 Power Offset Register

Address: 14

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 0.000

This offset value is added to each power value that is computed for each voltage/current sample pair before being accumulated in the energy register. The numeric format of this register is two's complement notation. This register can be used to offset contributions to the energy result that are caused by undesirable sources of energy that are inherent in the system.

5.10 AC Current Offset Register and AC Voltage Offset Register

Address: 16 (AC Current Offset Register)
17 (AC Voltage Offset Register)

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Default** = 0.000

The AC Offset Registers are initialized to zero on reset, allowing the device to function and perform measurements. First, the ground-level input should be applied to the inputs. Then the AC Offset Calibration Command is should be sent to the CS5460A. After ~(6N + 30) A/D conversion cycles (where N is the value of the Cycle-Count Register), the gain register(s) is loaded with the square of the system AC offset value. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. Note that this register value represents the square of the AC current/voltage offset.

5.11 Status Register and Mask Register

Address: *15* (Status Register)
26 (Mask Register)

23	22	21	20	19	18	17	16
DRDY	EOUT	EDIR	CRDY	MATH	Res	IOR	VOR
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWOR	IROR	VROR	EOR	EOOR	Res	ID3	ID2
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID1	ID0	WDT	VOD	IOD	LSD	0	$\overline{IC}$

Default** = 0x000000 (Status Register)

0x000000 (Mask Register)

The Status Register indicates the condition of the chip. In normal operation writing a '1' to a bit will cause the bit to go to the '0' state. Writing a '0' to a bit will maintain the status bit in its current state. With this feature the user can simply write back to the Status Register to clear the bits that have been seen, without concern of clearing any newly set bits. Even if a status bit is masked to prevent the interrupt, the status bit will still be set in the Status Register so the user can poll the status.

The Mask Register is used to control the activation of the $\overline{INT}$ pin. Placing a logic '1' in the mask register will allow the corresponding bit in the Status Register to activate the $\overline{INT}$ pin when the status bit becomes active.

$\overline{IC}$ Invalid Command. Normally logic 1. Set to logic 0 when the part is given an invalid command. Can be deactivated only by sending a port initialization sequence to the serial port. When writing to Status Register this bit is ignored.

LSD Low Supply Detect. Set when the voltage at the PFMON pin falls below the low-voltage threshold (with respect to VA- pin). For a given part, this threshold can anywhere between 2.3 V to 2.7 V.

IOD Modulator oscillation detect on the current channel. Set when the modulator oscillates due to an input above Full Scale. Note that the level at which the modulator oscillates is significantly higher than the current channel's Differential Input Voltage Range.

VOD Modulator oscillation detect on the voltage channel. Set when the modulator oscillates due to an input above Full Scale. Note that the level at which the modulator oscillates is significantly higher than the current channel's Differential Input Voltage Range.

Note: This IOD and VOD bits may be 'falsely' triggered by very brief voltage spikes from the power line. This event should not be confused with a DC overload situation at the inputs, when the IOD and VOD bits will re-assert themselves even after being cleared, multiple times.

WDT Watch-Dog Timer. Set when there has been no reading of the Energy register for more than 5 seconds. (MCLK = 4.096 MHz, K = 1) To clear this bit, first read the Energy register, then write to the Status Register with this bit set to logic '1'. When MCLK / K is not 4.096 MHz, the time duration is 5 * [4.096 MHz / (MCLK / K)] seconds.

ID3:0 Revision/Version Identification.

EOOR /EOUT Energy Summation Register went out of range. Note that the /EOUT Energy Summing Register is different than the Energy Register available through the serial port. This register cannot be read by the user. Assertion of the this bit can be caused by having an output rate that is too small for the power being measured. The problem can be corrected by specifying a higher frequency in the Pulse-Rate Register.

EOR Energy Out of Range. Set when the calibrated energy value is too large or too small to fit in the Energy Register, which can be read via the serial port.

VROR RMS Voltage Out of Range. Set when the calibrated RMS voltage value is too large to fit in the RMS-Voltage Register.

IROR RMS Current Out of Range. Set when the calibrated RMS current value is too large to fit in the RMS-Current Register.

PWOR Power Calculation Out of Range. Set when the *magnitude* of the calculated power is too large to fit in the Instantaneous Power Register.

VOR Voltage Out of Range.

IOR Current Out of Range. Set when the *magnitude* of the calibrated current value is too large or too small to fit in the Instantaneous Current Register.

MATH General computation Indicates that a divide operation overflowed. This can happen normally in the course of computation. If this bit is asserted but no other bits are asserted, then there is no error, and this bit should be ignored.

CRDY — Conversion Ready. Indicates a new conversion is ready. This will occur at the output word rate, which is usually 4 kHz.

EDIR — Set whenever the EOUT bit asserted (see below) as long as the energy result is negative.

EOUT — Indicates that the energy limit has been reached for the /EOUT Energy Summation Register, and so this register will be cleared, and one pulse will be generated on the /EOUT pin (if enabled). The energy flow may indicate negative energy or positive energy. This must be determined by looking at the EDIR bit (above). This EOUT bit is cleared automatically when the energy rate drops below the level that produces a 4 KHz EOUT pin rate. The bit can also be cleared by writing to the Status Register. This status bit is set with a maximum frequency of 4 KHz (when MCLK/K is 4.096 MHz). When MCLK/K is not equal to 4.096 MHz, the user should scale the pulse-rate that one would expect to get with MCLK/K = 4.096 MHz by a factor of 4.096 MHz / (MCLK/K) to get the actual pulse-rate.

DRDY — Data Ready. When running in single or continuous conversion mode, this bit will indicate the end of computation cycles. When running calibrations, this bit indicates that the calibration sequence has completed, and the results have been stored in the offset or gain registers.

5.12 Control Register

Address: 28

23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Res	Res	Res	Res	Res	Res	Res	STOP
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res	MECH	Res	INTL	SYNC	NOCPU	NOOSC	STEP

Default** = 0x000000

STOP — 1 = used to terminate the new EEBOOT sequence.

Res — Reserved. These bits must be set to zero.

MECH — 1 = widens $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pulses for mechanical counters.

INTL — 1 = converts the /INT output to open drain configuration.

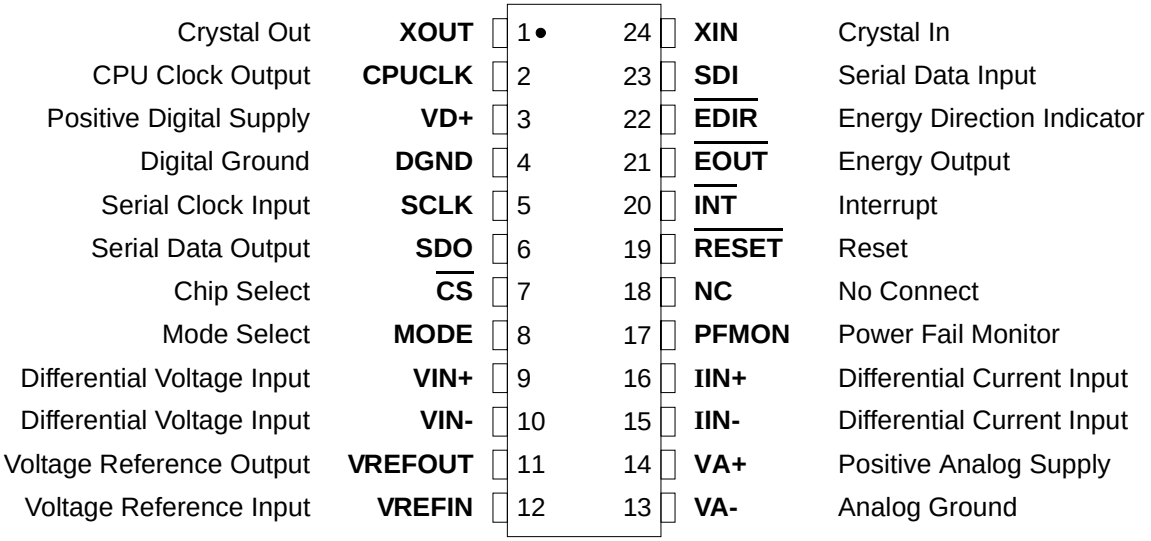
SYNC — 1 = forces internal A/D converter clock to synchronize to the initiation of a conversion command.

NOCPU — 1 = converts the CPUCLK output to a one-bit output port. Reduces power consumption.

NOOSC — 1 = saves power by disabling the crystal oscillator for external drive.

STEP — 1 = enables stepper-motor signals on the $\overline{\text{EOUT}}$/$\overline{\text{EDIR}}$ pins.

6. PIN DESCRIPTION

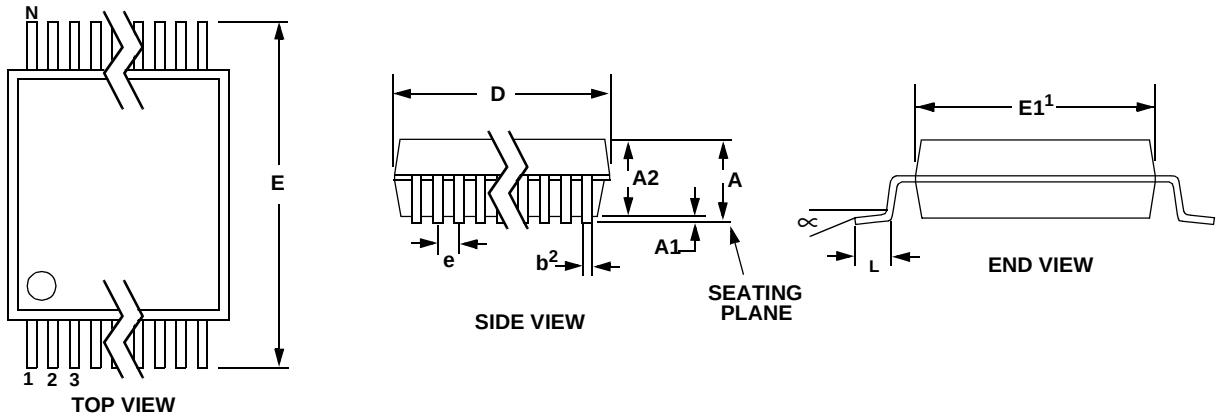


Clock Generator		
Crystal Out **Crystal In**	1,24	**XOUT, XIN** - A gate inside the chip is connected to these pins and can be used with a crystal to provide the system clock for the device. Alternatively, an external (CMOS compatible clock) can be supplied into XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins and Serial Data I/O		
Serial Clock Input	5	**SCLK -** A clock signal on this pin determines the input and output rate of the data for the SDI and SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.
Serial Data Output	6	**SDO -** SDO is the output pin of the serial data port. Its output will be in a high impedance state when $\overline{CS}$ is high.
Chip Select	7	**$\overline{CS}$ -** When low, the port will recognize SCLK. An active high on this pin forces the SDO pin to a high impedance state. $\overline{CS}$ should be changed when SCLK is low.
Mode Select	8	**MODE** - When at logic high, the CS5460A can perform the auto-boot sequence with the aid of an external serial EEPROM to receive commands and settings. When at logic low, the CS5460A assumes normal command-mode operation. This pin is pulled down to logic low if left unconnected.
Interrupt	20	**$\overline{INT}$ -** When $\overline{INT}$ goes low it signals that an enabled event has occurred. $\overline{INT}$ is cleared (logic 1) by writing the appropriate command to the CS5460A.
Energy Output	21	**$\overline{EOUT}$ -** The energy output pin output a fixed-width pulse rate output with a rate (programmable) proportional to energy.
Energy Direction Indicator	22	**$\overline{EDIR}$** - The energy direction indicator indicates if the measured energy is negative.
Serial Data Input	23	**SDI -** the input pin of the serial data port. Data will be input at a rate determined by SCLK.
Measurement and Reference Input		
Differential Voltage Inputs	9,10	**VIN+, VIN- -** Differential analog input pins for voltage channel.

Voltage Reference Output	11	**VREFOUT -** The on-chip voltage reference is output from this pin. The voltage reference has a nominal magnitude of 2.5 V and is reference to the VA- pin on the converter.
Voltage Reference Input	12	**VREFIN -** The voltage input to this pin establishes the voltage reference for the on-chip modulator.
Differential Current Inputs	15,16	**IIN+, IIN- -** Differential analog input pins for current channel.
Power Supply Connections		
Positive Digital Supply	3	**VD+ -** The positive digital supply is nominally +5 V ±10% relative to DGND.
Digital Ground	4	**DGND -** The digital ground is at the same level as VA-.
Negative Analog Supply	13	**VA- -** The negative analog supply pin must be at the lowest potential.
Positive Analog Supply	14	**VA+ -** The positive analog supply is nominally +5 V ±10% relative to VA-.
Power Fail Monitor	17	**PFMON -** The power fail Monitor pin monitors the analog supply. Typical threshold level is 2.5 V with respect to the VA- pin, with +/-50 mV of hysteresis. If PFMON voltage threshold is tripped, the LSD (low-supply detect) bit is set in the Status Register.
$\overline{\text{RESET}}$	19	**Reset -** When reset is taken low, all internal registers are set to their default states.
Other		
No Connection	18	**NC -** No connection. Pin should be left floating.

7. PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

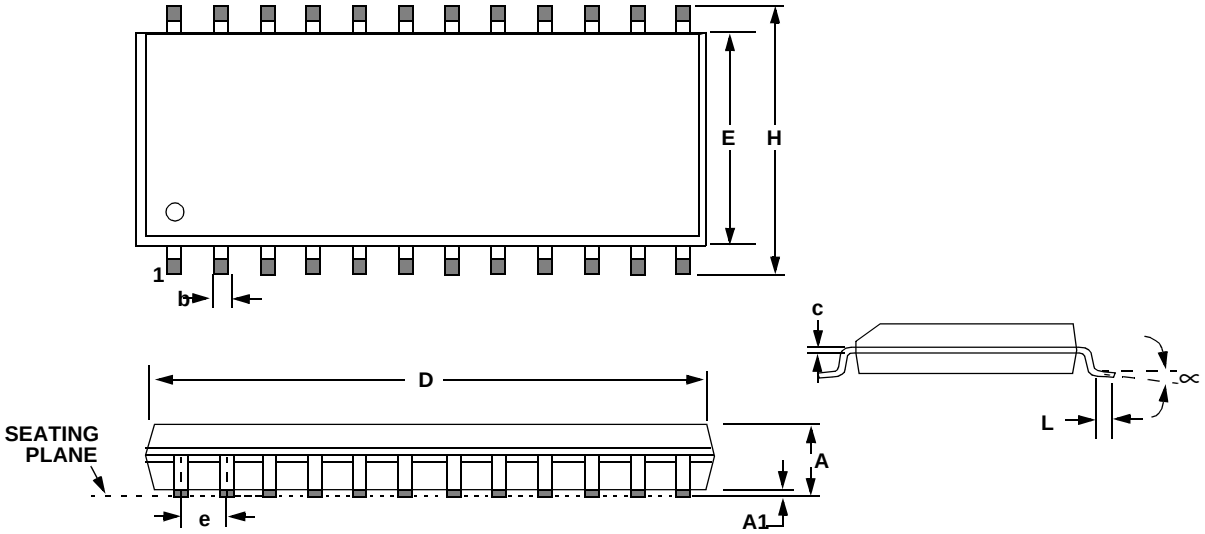
Controlling Dimension is Millimeters.

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

24L SOIC (300 MIL BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.093	0.098	0.104	2.35	2.50	2.65
A1	0.004	0.008	0.012	0.10	0.20	0.30
b	0.013	0.017	0.020	0.33	0.42	0.51
C	0.009	0.011	0.013	0.23	0.28	0.32
D	0.598	0.606	0.614	15.20	15.39	15.60
E	0.291	0.295	0.299	7.40	7.50	7.60
e	0.040	0.050	0.060	1.02	1.27	1.52
H	0.394	0.407	0.419	10.00	10.34	10.65
L	0.016	0.026	0.050	0.40	0.65	1.27
∝	0°	4°	8°	0°	4°	8°

JEDEC #: MS-013

Controlling Dimension is Millimeters

• Notes •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™