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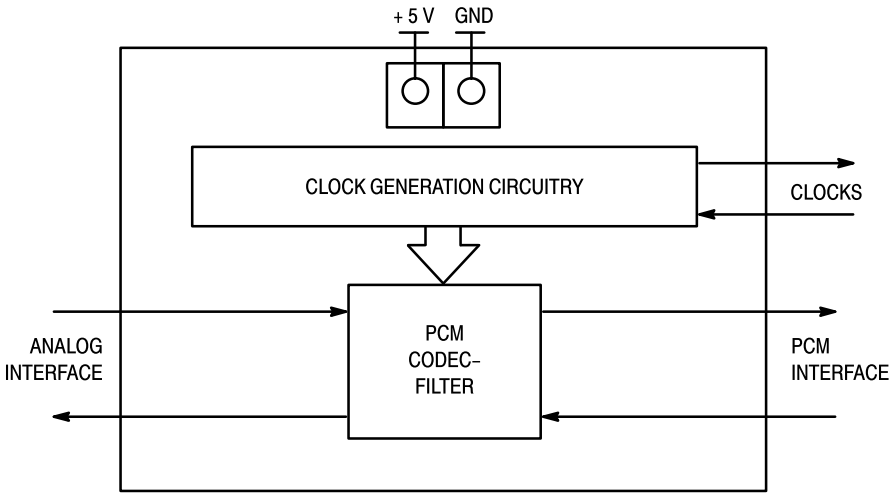
MC14LC5480EVK

Advance Information

MC14LC5480, MC145481, MC145482, MC145483, and MC145484 PCM Codec-Filter Evaluation Kit Users Manual



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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SECTION 1 – GENERAL DESCRIPTION

1.1 ORGANIZATION OF DATA SHEET

This document is composed of three sections. Section 1 is intended to introduce the MC14LC5480EVK Codec–Filter Evaluation Kit with a brief description of the evaluation board and a list of key features. Section 2 introduces the hardware comprising each functional block of the MC14LC5480EVK. Section 3 describes the standalone operating modes and indicates a recommended jumper positioning for these modes. It also discusses the back–to–back mode of operation using two MC14LC5480EVKs.

Appended to the end of this document are the latest data sheets for the applicable devices.

1.2 INTRODUCTION

The MC14LC5480EVK is the primary tool for evaluation and demonstration of the following PCM and linear codec–filters.

Table 1–1. Mu–/A–Law and Linear PCM Codec–Filters

Part Number	V_{CC}	Description
MC14LC5480	5 V	Mu–/A–Law Companding
MC145481	3 V	Mu–/A–Law Companding
MC145482	5 V	Linear
MC145483	3 V	Linear
MC145484	5 V	Mu–/A–Law Companding

Figure 1–1 is a functional block diagram of the MC14LC5480EVK. The MC14LC5480EVK is comprised of two functional blocks — the clocking circuitry, and one of the PCM Codec–Filters listed in Table 1–1.

User I/O to the board is provided via a number of convenient connectors. First, an industry standard 4–pin RJ11 handset jack (P1) is provided to connect the handset included with the kit. Next, a 2x20 pin header (P13) is provided for access to key analog and digital signals for connection to external test equipment, a user defined system, or a second MC14LC5480EVK. And finally, two male BNC connectors (P6 and P14) provide convenient access to the codec's analog transmit and receive paths for connection to external test equipment.

The MC14LC5480EVK requires either a 5 V or 3 V supply provided through P2 at the top of the circuit board.

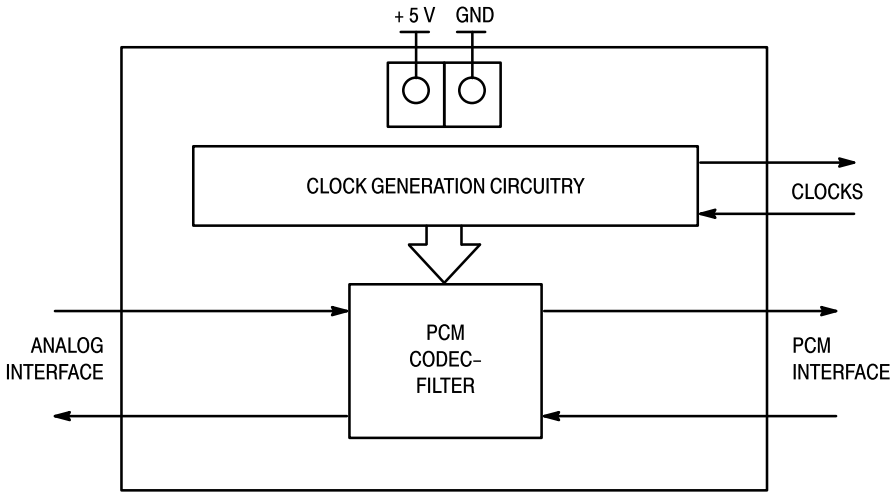

Figure 1–1. MC14LC5480EVK Functional Block Diagram

1.3 EVK FEATURES

- Provides Standalone Evaluation on a Single Board
- Single 5 V or 3 V Power Supply
- Easily Interfaced to Test Equipment, Customer System, or Second MC14LC5480EVK
- Convenient Access to Key Signals
- Generous Wire Wrap Area for Application Development
- Kit Provides Analog–to–Analog, Analog–to–Digital, and Digital–to–Analog
- Compatible Handset Provided
- Kit Includes: Schematics, Data Sheets, User's Manual, and Samples of Each PCM Codec–Filter

1.4 PRODUCT FEATURE OVERVIEW

GENERAL:

- All of the PCM Codec–Filter Products Described in this Document are:
  - Manufactured in a 0.8 Micron CMOS Process
  - Designed with Differential Analog Circuits for Lowest Noise
  - Available in 20–Pin Plastic SOIC and SSOP Packages

SPECIFIC BY DEVICE:

MC14LC5480

- Single 5 V Power Supply
- Typical Power Dissipation of 15 mW, Power Down of < 1 mW
- Conforms to CCITT, ITU–T, and Bell Specifications
- Pin 16 = Mu–Law or A–Law Companding
- Pin 1 = RO+ Output

MC145481

- Single 3 V Power Supply
- Typical Power Dissipation of 8 mW, Power Down of < 1 mW
- Conforms to CCITT, ITU–T, and Bell Specifications
- Pin 16 = Mu–Law or A–Law Companding
- Pin 1 = V_{AG} Ref

MC145482

- Single 5 V Power Supply
- Typical Power Dissipation of 30 mW, Power Down of < 1 mW
- 13–Bit Linear 2's Complement
- Sample Rates from 7 kHz to 16 kHz
- Pin 16 = HB (High–Pass Filter Bypass)
- Pin 1 = V_{AG} Ref

MC145483

- Single 3 V Power Supply
- Typical Power Dissipation of 8 mW, Power Down of < 1 mW
- 13–Bit Linear 2's Complement
- Sample Rate of 8 kHz
- Pin 16 = HB (High–Pass Filter Bypass)
- Pin 1 = V_{AG} Ref

MC145484

- Single 5 V Power Supply
- Typical Power Dissipation of 15 mW, Power Down of < 1 mW
- Conforms to CCITT, ITU–T, and Bell Specifications
- Pin 16 = Mu–Law or A–Law Companding
- Pin 1 = V_{AG} Ref

SECTION 2 – HARDWARE DESCRIPTION

NOTE

Please refer to the MC14LC5480EVK schematic for the following discussion of the hardware.

For the MC14LC5480 PCM Codec–Filter, Jumper J4 must be open. For the MC145481, MC145482, MC145483, and MC145484, Jumper J4 must be connected.

2.1 CLOCK GENERATION CIRCUITRY

A 4.096 MHz crystal oscillator is used as the system clock for the MC14LC5480EVK. From this 4.096 MHz crystal, frame sync (FSYNC), bit clock (BCLK), and 256 kHz are derived for use by the PCM Codec–Filter.

FSYNC

Frame sync (FSYNC) is generated on–board, and is controlled through J20A for FSR (frame sync receive), and J16 for FST (frame sync transmit). Populating these jumpers also routes the FSYNC to the 2x20 connector (P13), Pin 40 (FSR), and Pin 1 (FST).

S1 allows the user to select the “width” of FSYNC. The FSYNC pulse width is set as a number of BCLKs. The following number of BCLKs for FSYNC can be set with S1.

- 1–2–3–4–8–12–13–16

The switch S1 configurations for these settings are presented below.

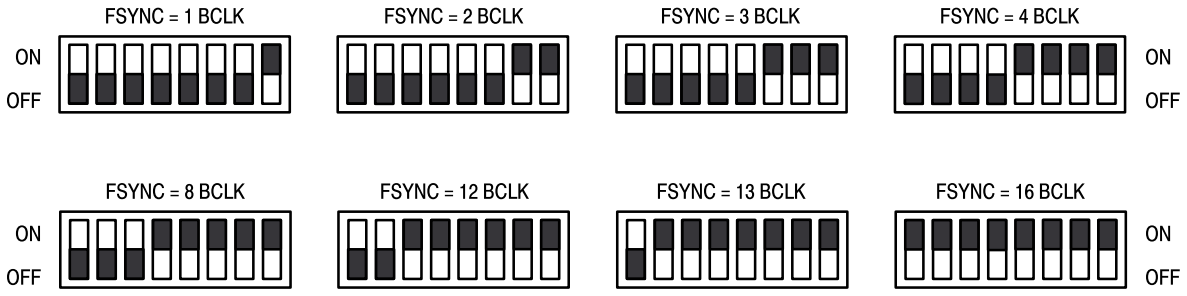

Figure 2–1. Switch S1 Settings for FSYNC Duration

When configuring the MC14LC5480EVK to connect to the MC145532 ADPCM Transcoder, the various transcoding rates of the MC145532 can be exercised using the S1 switch positions as shown in Figure 2–2. Refer to the MC145532 data sheet for relevant timing diagrams.

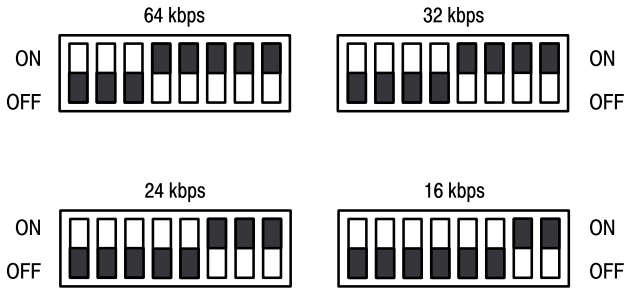

Figure 2–2. S1 Settings for Transcoding Rates

NOTE

For above settings to be valid, it is important to have the J2A jumper populated. This sets the FSYNC at 8 kHz. Populating J2B sets the FSYNC at 16 kHz, which is used exclusively for the MC145482 13–Bit Linear PCM Codec–Filter.

BCLK

Bit Clock (BCLK) is routed through J19A (BCLKR) and J8 (BCLKT). When these jumpers are populated, BCLK is presented to the 2x20 connector (P13), Pin 36 (BCLKR), and Pin 5 (BCLKT).

J1 allows the user to select the frequency at which BLCK operates. The jumper–selectable frequencies are 4.096 MHz, 2.048 MHz, 1.024 MHz, 512 kHz, 128 kHz, and 64 kHz.

256 kHz

256 kHz is presented to J7A as a possible frequency setting for the master clock (MCLK) input on the chosen PCM Codec–Filter. J7B will configure the MCLK input to have a frequency equal to BCLK.

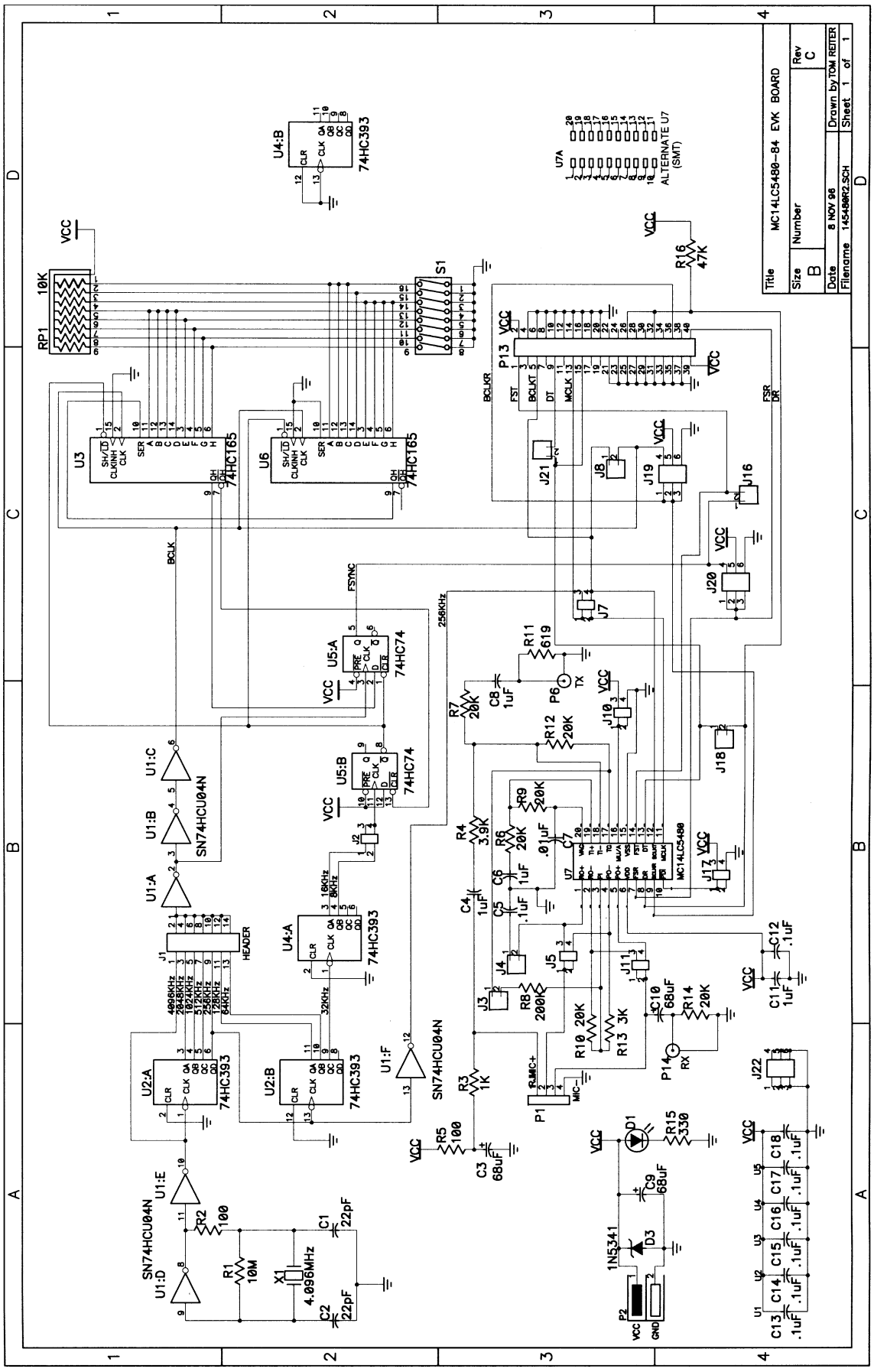

Figure 2–3. MC14LC5480EVK Schematic

2.2 JUMPER DESCRIPTIONS

NOTE

When a jumper is referenced as J#, where # is a number: A populated jumper enables the function, an unpopulated jumper disables the function.

When a jumper is referenced as J#@, where # is a number and @ is a letter: Only one jumper may be populated for each given # location. For example, populate J2A ***or*** J2B, not J2A ***and*** J2B.

J1: BCLK SELECT

J1 selects the BCLK frequency. A choice of seven frequencies is available — these are from 64 kHz to 4.096 MHz.

J2A: FSYNC = 8 kHz

J2A sets the FSYNC to 8 kHz.

J2B: FSYNC = 16 kHz

J2B sets the FSYNC to 16 kHz, for use with the MC145482 only.

J3: SIDETONE

J3 enables the sidetone path on the PCM Codec–Filter.

J4: V_{AG} CAP ENABLE

J4 enables the V_{AG} filter cap. This jumper should be populated only when evaluating the MC145481, MC145482, MC145483, and MC145484. It should ***not*** be populated when evaluating the MC14LC5480.

J5A: SPKR+ = RO+

J5A connects the path from the MC14LC5480 Pin 1 (RO+) to the RJ11 and handset. This jumper should ***not*** be populated when evaluating the MC145481, MC145482, MC145483, and MC145484.

J5B: SPKR+ = PO–

J5B connects a path from the PCM Codec–Filter Pin 4 (PO–) to the RJ11 and handset.

J6: NOT AVAILABLE

J7A: MCLK = 256 kHz

J7A sets the MCLK Pin 11 to 256 kHz.

J7B: MCLK = BCLK

J7B sets the MCLK Pin 11 to be equal to BCLK.

J8: BCLKT = BCLK

J8 connects BCLK to BCLKT (Pin 12) of the PCM Codec–Filter.

J9: NOT AVAILABLE

J10A: MU–LAW SELECT/HIGH–PASS FILTER BYPASS

J10A selects Mu–Law on the MC14LC5480, MC145481, and MC145484. On the MC145482 and MC145483, this jumper enables the high–pass filter bypass for frequency response down to DC for the transmit ADC conversion.

J10B: A–LAW SELECT/HIGH–PASS FILTER BYPASS DISABLE

J10B selects A–Law on the MC14LC5480, MC145481, and MC145484. On the MC145482 and MC145483, this jumper disables the high–pass filter bypass.

J11A: SPKR– = RO–

J11A connects RO– (Pin 2) to the RJ11 and the receive output BNC connector.

J11B: SPKR– = PO+

J11B connects PO+ (Pin 5) to the RJ11 and the receive output BNC connector.

J12: NOT AVAILABLE

J13: NOT AVAILABLE

J14: NOT AVAILABLE

J15: NOT AVAILABLE

J16: FST = FSYNC

J16 connects the on–board generated FSYNC to the PCM Codec–Filter (Pin 14) FST as well as Pin 1 of the 2x20 connector (P13).

J17A: POWER–UP

J17A connects the PDI (Pin 10) of the PCM Codec–Filter to V_{DD} to power–up the device.

J17B: POWER–DOWN

J17B connects the PDI (Pin 10) of the PCM Codec–Filter to V_{SS} to power–down the device.

J18: DT = DR

J18 connects the data transmit (DT Pin 13) to the data receive (DR Pin 8) of the PCM Codec–Filter.

J19A: BCLKR + BCLK

J19A connects BCLKR (Pin 9) of the PCM Codec–Filter to BCLK.

J19B: BCLKR = V_{DD}

J19B connects BCLKR (Pin 9) of the PCM Codec–Filter to V_{DD} for IDL interface compatibility.

J19C: BCLKR = V_{SS}

J19C connects BCLKR (Pin 9) of the PCM Codec–Filter to V_{SS} for GCI interface compatibility.

J20A: FSR = FSYNC

J20A connects FSR (Pin 7) of the PCM Codec–Filter to FSYNC.

J20B: FSR = V_{DD}

J20B connects FSR (Pin 7) of the PCM Codec–Filter to V_{DD} to select channel B2 in the IDL or GCI ISDN mode.

J20C: FSR = V_{SS}

J20C connects FSR (Pin 7) of the PCM Codec–Filter to V_{SS} to select channel B1 in the IDL or GCI ISDN mode.

J21: DT OUT

J21 connects DT of the PCM Codec–Filter to P13 (Pin 9).

2.3 HANDSET

The compatible handset included with the kit is a Walker Equipment Corporation W3–KM–EM–80RP00, reverse polarity. The handset is a “K” style unit with a 4–pin modular connector. The handset incorporates a low–level electret microphone and a dynamic receiver equipped with a hearing aid coil and a varistor for receive level limiting.

Transmitter

Transmit Output Level @ 1000 Hz: – 46 dBV ± 4 dB

Output Impedance @ 100 Hz: 1000 ± 300 Ω

Receiver

Receive Output Level @ 1000 Hz: 79 dBSPL ± 4 dB

Receive Input Impedance @ 100 Hz: 150 Ω ± 20%

For more detailed characteristics of the W3–KM–EM–80RP00 handset, please contact Walker Equipment Corporation at 1–800–HANDSET.

SECTION 3 – OPERATING MODES

3.1 STANDALONE OPERATION – MC14LC5480

Figure 3–1 indicates the proper position of jumpers to operate the MC14LC5480EVK “standalone”. The “darkened” areas indicate the position of a populated jumper. Signal flow for the standalone mode as indicated in Figure 3–1 is as follows. A signal input at P4, Transmit Input, is presented to the encoder of the MC14LC5480 where it is digitized and output on the Data Transmit (DT) pin (Jumper J18). This provides a “local loopback” of PCM data to the Data Receive (DR) pin of the MC14LC5480, where it is reconstructed and output at P14, Receive Output.

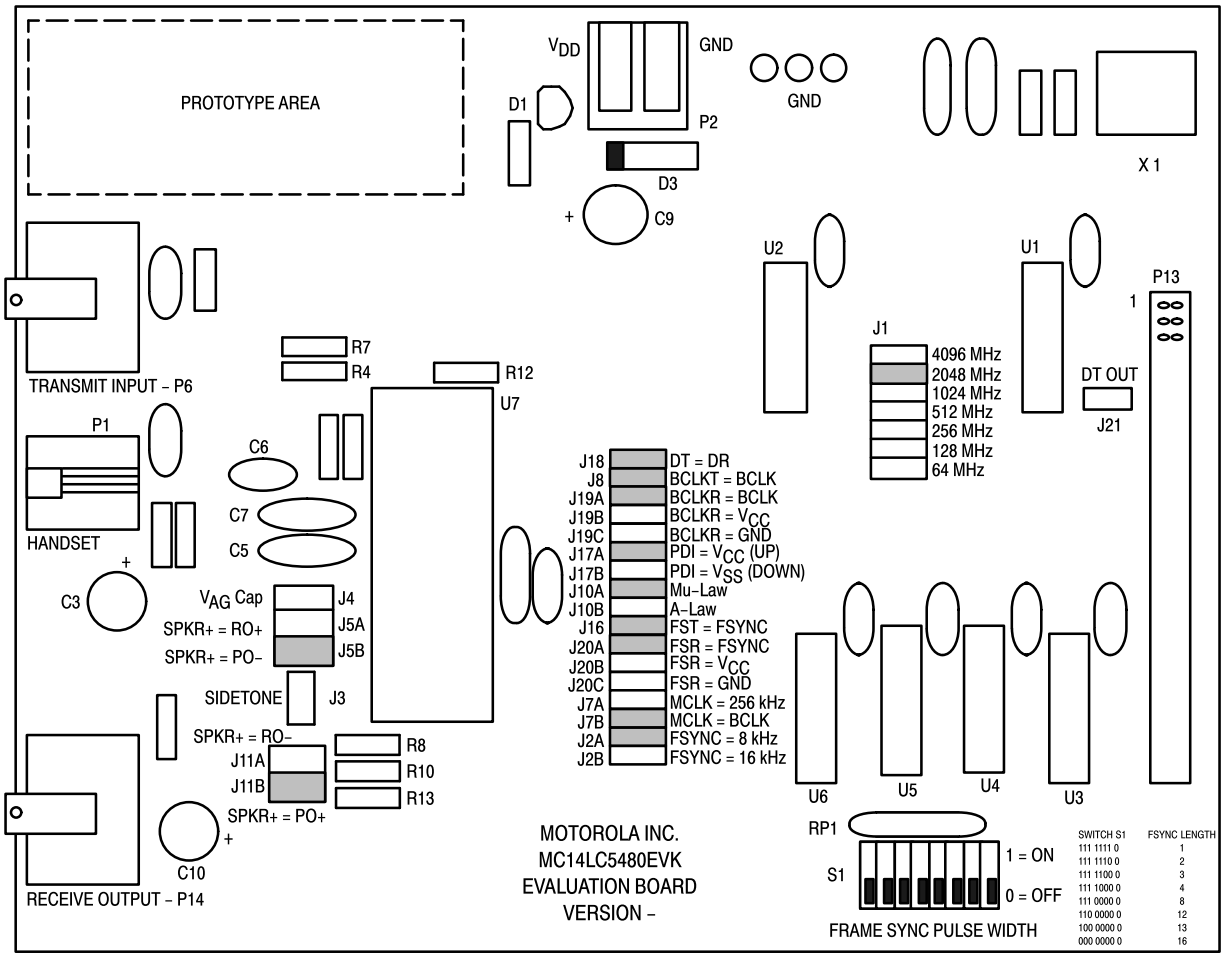

Figure 3–1. Jumper Positions for Standalone Operation

3.2 BACK–TO–BACK OPERATION

Figures 3–2 and 3–3 indicate the proper position of jumpers to operate two MC14LC5480EVKs back–to–back. When the jumpers are populated as shown and the boards are connected as in Figure 3–4, this signal path realizes a full “analog–to–analog”, “handset–to–handset” connection — passing data from PCM Codec–Filter to PCM Codec–Filter.

Board #1 acts as the system master, providing BCLK and FSYNC to board #2.

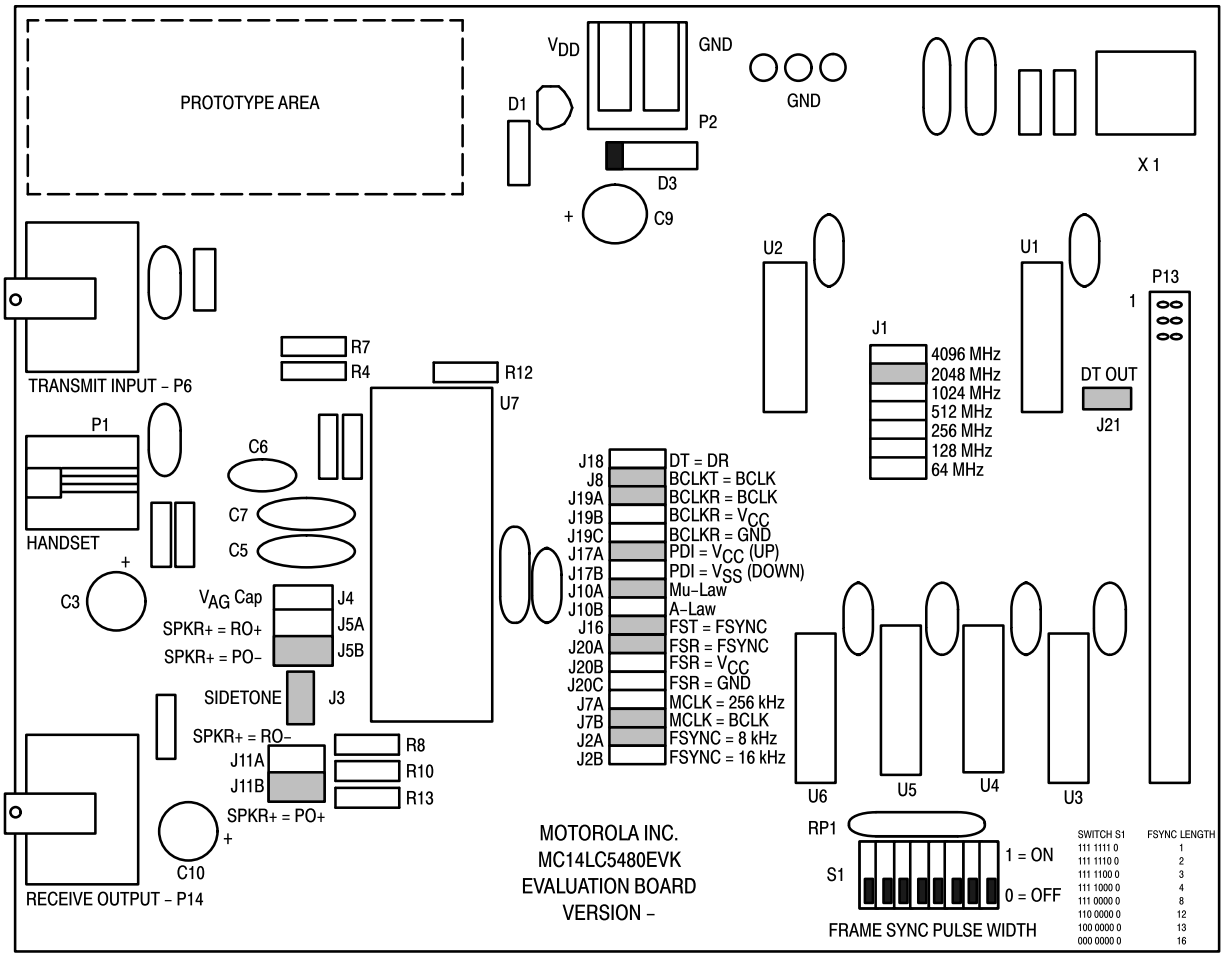

Figure 3–2. Jumper Positions for Back–to–Back Operation — MC14LC5480EVK #1

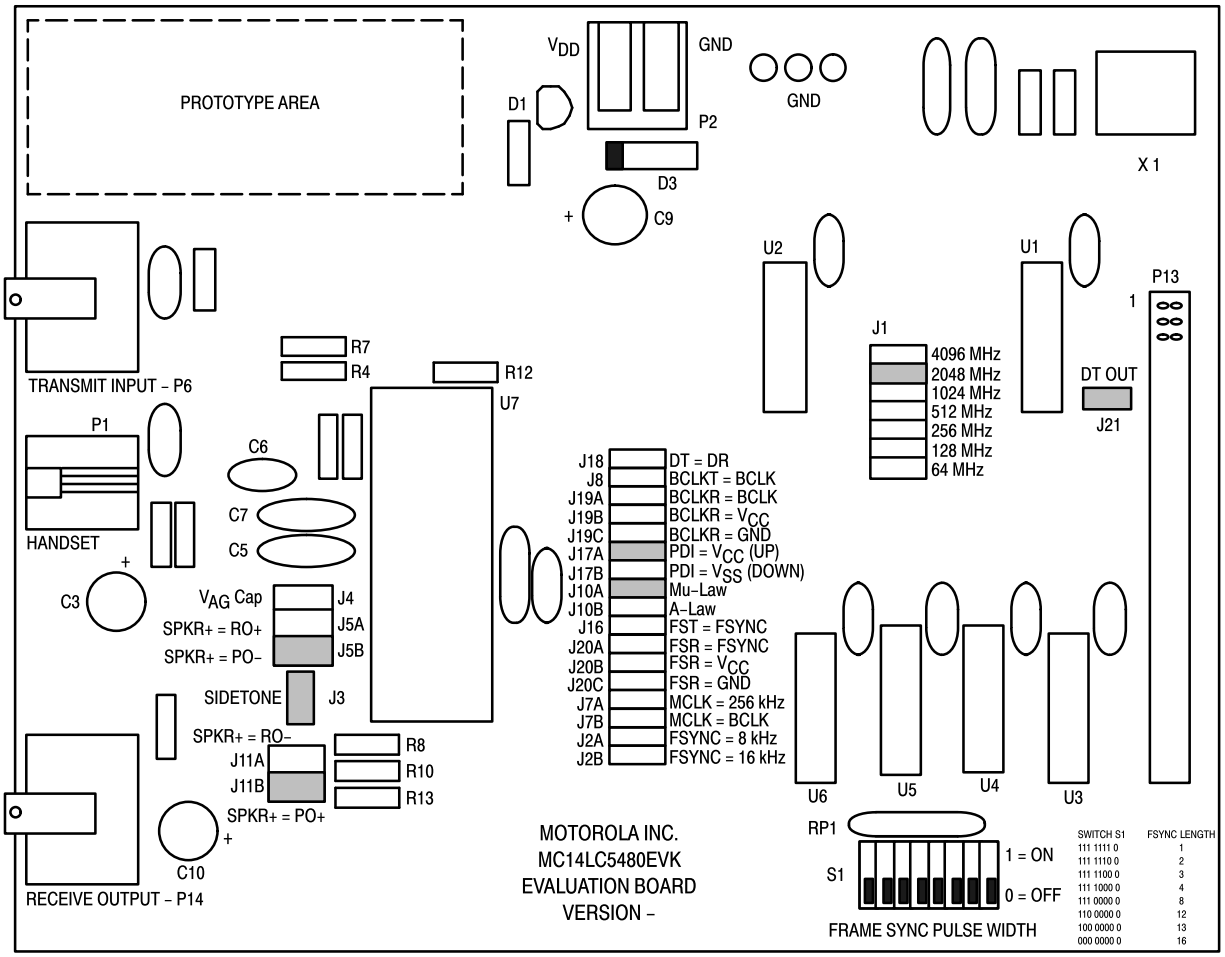

Figure 3–3. Jumper Positions for Back–to–Back Operation — MC14LC5480EVK #2

The MC14LC5480EVK was designed to connect back–to–back as shown in Figure 3–4. A 2x20 ribbon cable, 2–3 inches maximum in length, makes all necessary electrical connections, allowing a full “analog–to–analog”, “handset–to–handset” path to be established.

NOTE

Power and ground are bussed to the second MC14LC5480EVK. Do ***not*** connect a second power supply to board #2!

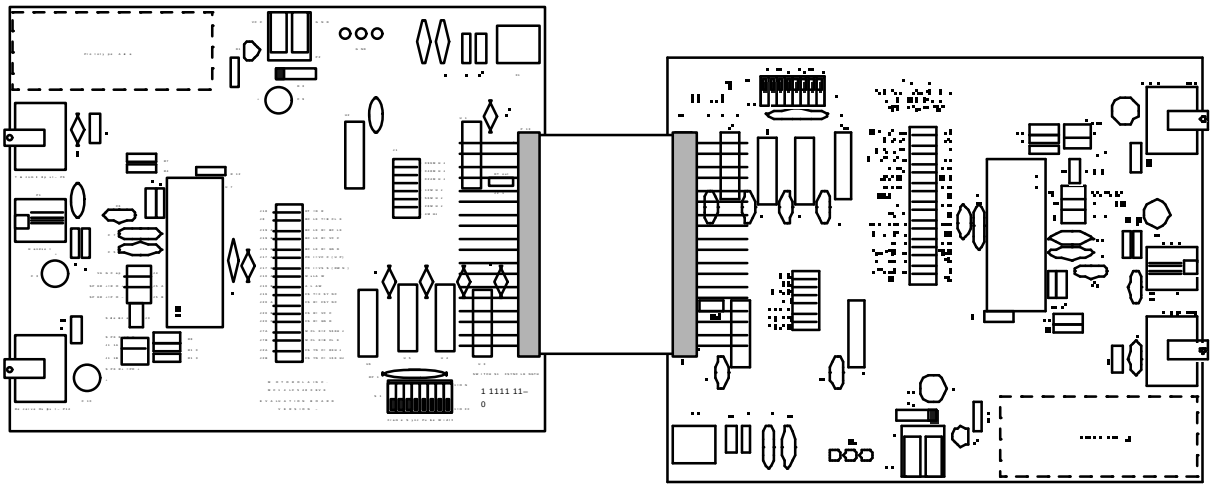

Figure 3–4. Recommended Cabling for Back–to–Back Operation

The preceding pages describe the “most common” configurations that the MC14LC5480EVK may operate. There are many modes of operation that have not been described in this document that the user may find useful. Please familiarize yourself with the included schematic diagram, as this may provide insight into a configuration that may prove beneficial for evaluating these parts in your application. If there are specific questions on a particular configuration that is not documented, do not hesitate to contact your local Motorola representative, or call the factory for assistance.

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