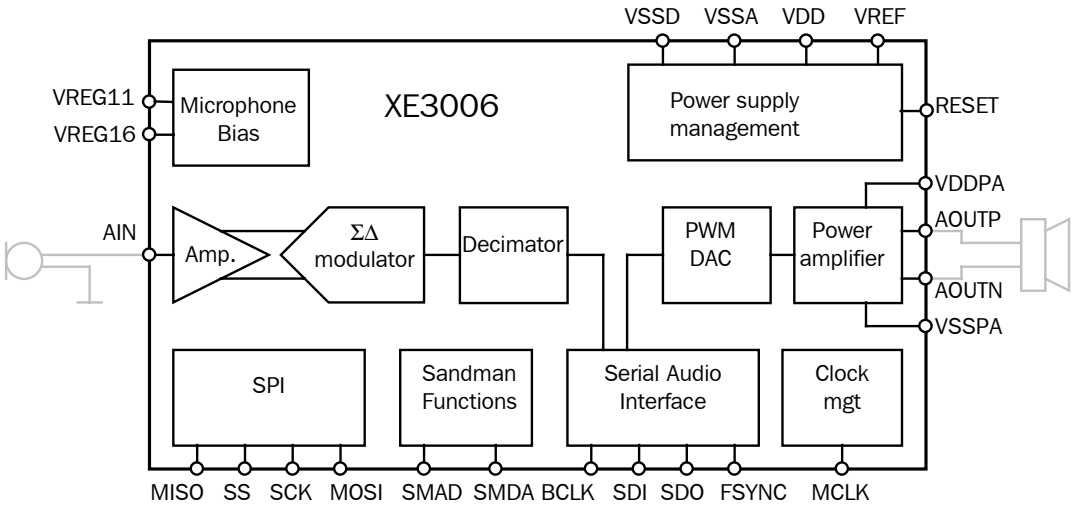

XE3005 / XE3006

Low-Power Audio CODEC

General Description

The XE3005/6 is an ultra low-power CODEC (Analog to Digital and Digital to Analog Converter) for voice and audio applications. It includes microphone supply, preamplifier, 16-bit ADC, 16-bit DAC, serial audio interface, power management, clock management and Sandman™ functions for the ADC and the DAC. The sampling frequency of the ADC and of the DAC can be adjusted from 4 kHz to 48kHz.

The XE3006 includes the Sandman™ function, which signals whether a relevant voice or audio signal is present in the ADC or DAC. This allows you to put other components in the application to sleep.

Applications

- Wireless Headset
- Bluetooth™ headset
- Digital music playback
- Hands-free telephony
- Digital hearing instruments
- Consumer and multimedia applications
- Battery-operated portable audio devices

Features

- Ultra low-power consumption, below 2 mW
- Low-voltage operation down to 1.8 V
- Sandman™ function to reduce system power consumption (XE3006)
- Single supply voltage
- Adjustable sampling frequency: 4 – 48 kHz
- Digital format: 16 bit 2s complement
- Only 2 low-cost external components
- Easy interfacing to various DSPs
- Direct connection to microphone and speaker
- Various programming options

Quick Reference Data

- supply voltage 1.8 – 3.3 V
- current consumption 0.4 mA (fs =20 kHz)
- sampling frequency 4 – 48 kHz
- peak output current 100 mA
- Typical dynamic range ADC 80 dB
- Typical dynamic range DAC 60 dB

Ordering Information

Part	Package	Ext. part no.	Temperature range
XE3005	TSSOP 20 pins	XE3005I033	-40 to 85° C
XE3006	TSSOP 24 pins	XE3006I019	-40 to 85° C

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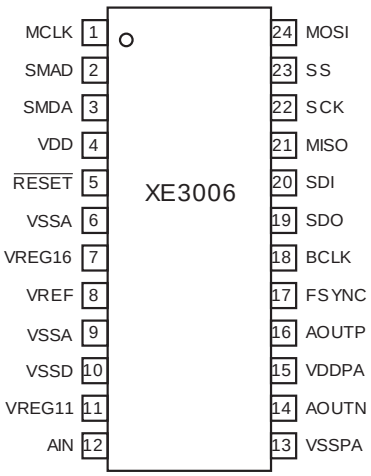
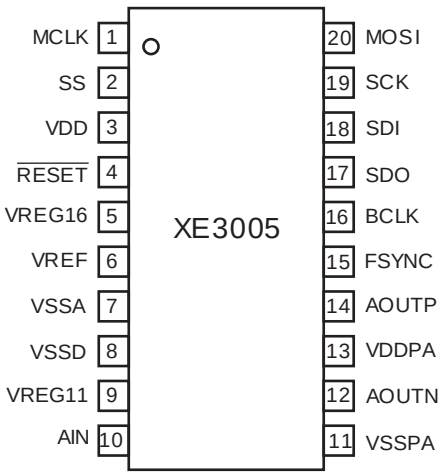
List of Illustrations

1 Device Description





1.1 Terminal Descriptions XE3005/6

Terminals			Type [1]	Description
XE3006	XE3005	Name		
1	1	MCLK	DI	Master Clock. MCLK derives the internal clocks of ADC and DAC
2	N/A	SMAD	DO	Sandman output ADC
3	N/A	SMDA	DO	Sandman output DAC
4	3	VDD	AI	Digital power supply
5	4	$\overline{\text{RESET}}$	ZI/O	The reset signal can be used as a hardware power down input. It will then initialize all the internal register to their default value
6	N/A	VSSA	AI	Analog ground
7	5	VREG16	AO	Regulator voltage 1.6 V. Can be used to supply microphone
8	6	VREF	AO	Reference voltage
9	7	VSSA	AI	Analog ground
10	8	VSSD	AI	Digital ground
11	9	VREG11	AO	ADC Regulated microphone output supply voltage 1.1 V
12	10	AIN	AI	ADC Analog input signal
13	11	VSSPA	AI	DAC Power Amplifier Ground
14	12	AOUTN	AO	DAC Analog Output negative
15	13	VDDPA	AI	DAC Power Amplifier Supply
16	14	AOUTP	AO	DAC Analog Output positive
17	15	FSYNC	DI/O	Serial audio interface Frame Synchronization
18	16	BCLK	DI/O	Serial audio interface Bit Clock
19	17	SDO	ZO	Serial audio interface Data Output
20	18	SDI	DI PD	Serial audio interface Data Input
21	N/A	MISO	ZO	SPI Master In Slave Out
22	19	SCK	DI PD	SPI Serial Clock
23	2	SS	DI PU	SPI Slave Select
24	20	MOSI	DI PD	SPI Master Out Slave In

Note: (1) AI = Analog Input AO = Analog Output
DI = Digital Input DO = Digital Output
DI/O = Digital In or Out ZO = Hi Impedance or Output
PU = internal Pull Up PD = internal Pull Down
ZI/O = Hi impedance In or Out

2 Functional Description

A detailed description of the registers can be found in section 8.

2.1 Device Functions

2.1.1 ADC Signal Channel

The ADC channel is a chain of programmable amplifier, band-pass filter, sigma-delta modulator and a decimation filter. Amplifier gain is programmable to 5x (default) and 20x through register E. The band-pass filter has cut-off frequencies proportional to the sampling rate. The sigma-delta modulator operates at 256 times oversampling rate. The decimator transmits data through the Serial Audio Interface in 16-bit wide 2's complement format. The protocol can be selected through register J.

With the default settings of the register C (0xF0), the ADC can run at a sampling frequency up to 20kHz. When used with a sampling frequency higher than 20kHz, the register C must be set to the value 0xC4 to guarantee the optimal performance. The whole ADC chain can be powered-down through register I.

2.1.2 DAC Signal Channel

The DAC channel is a pulse-width modulation (PWM) DAC followed by a differential power amplifier. The PWM DAC is based on a sigma-delta modulator, which operates at 32 times oversampling rate. A power amplifier follows the DAC. The DAC receives 16-bit wide 2's complement format through the Serial Audio Interface. The protocol can be selected through register J. The complete DAC and PA amplifier chain can be powered-down through register I.

2.1.3 MIC Input

The programmable pre-amplifier and the microphone bias sources VREG11 and VREG16 are optimized to operate with electret microphones. VREG11, providing 1.1 V / 50 uA typically and a power-supply rejection ratio of -90 dB, which is a superior performance over VREG16 which delivers 1.6 V / 1 mA typically for a power supply rejection ratio of -50 dB. An electret microphone can also be biased from a bias source external to the device. VREG11 is activated through control register E.

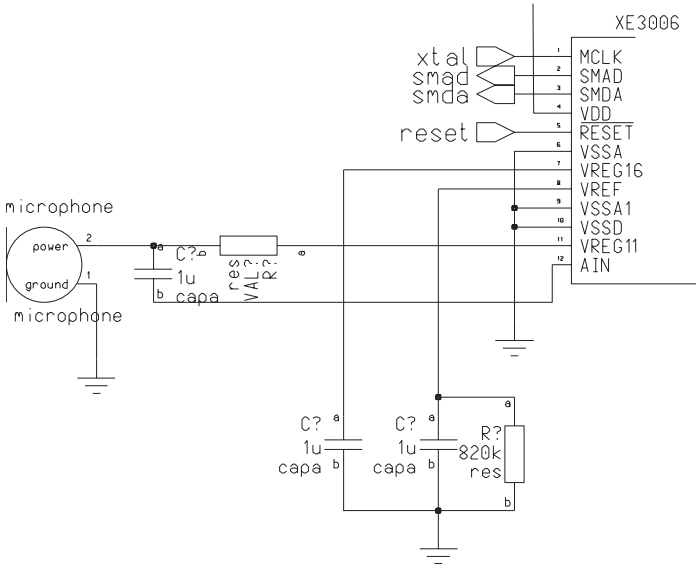


Figure 1: typical microphone interface (1.1 V / 50 uA bias through VREG11)

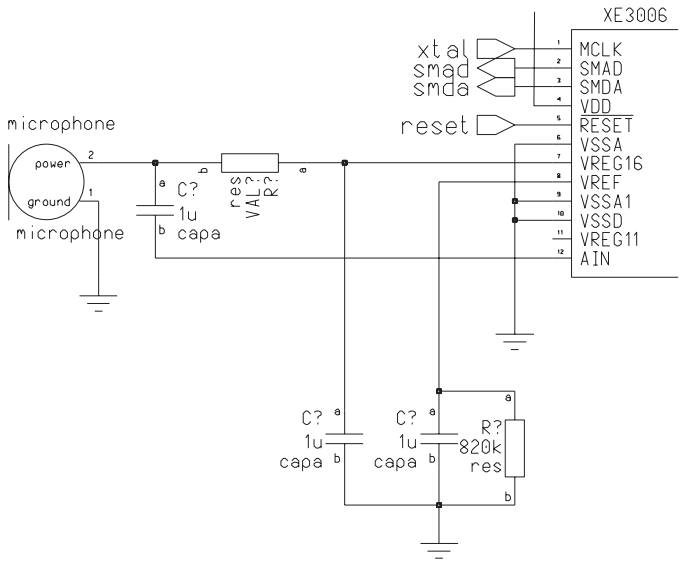


Figure 2: typical microphone interface (1.6 V / 1 mA bias through VREG16)

2.1.4 Power Amplifier

The Power Amplifier is a **Class D amplifier**, which is based on pulse-width modulators and offers higher efficiency than the traditional Class AB topologies. It uses a three-state unbalanced PWM. This means that both channels of the PA (AOUTP and AOUTN) will not toggle at the same time, therefore the outputs are not purely differential.

2.1.5 Digital Loopback

In digital loopback mode, the ADC output is routed directly to the DAC input. This allows in-circuit system level tests. The digital loopback mode can be selected through register J.

2.1.6 Operating Frequency

The sampling frequency represented by the signal FSYNC is derived from the master clock MCLK input with the following equation:

Fs = Sampling (conversion) frequency = MCLK/(256 x div_factor), div_factor = 1, 2, 3, 4

The inverse of the sampling frequency is the time between the falling edges of two successive primary frame-sync (FSYNC) signals. This time is the conversion period.

For example, to set the conversion rate to 8kHz, MCLK = 256 x div_factor x 8000

An external device supplies the master clock (MCLK). The clock frequency of the signal applied to the MCLK pin may vary between 1024 kHz minimum and 33.9 MHz maximum. The internal clock signal FINT is derived from MCLK by dividing it by 1 (default), 2, 3 or 4. The internal clock signal is used to operate the ADC signal channel and the DAC signal channel. The div_factor is selected through register I. The maximum internal clock signal frequency is 12.288 MHz.

The BCLK defines the time when the data must be presented to the serial audio interface and shifted into or out of the CODEC (pin SDI and SDO). The number of clocks into one FSYNC period is 32. 16 for the left audio channel and 16 for the right audio channel (however the device contains only a single audio channel).

The table below shows some example of the relationships between MCLK and FSYNC

MCLK	Div_factor (see reg I)	Min BCLK	FSYNC
2048 kHz	1	256 kHz	8 kHz
8192 kHz	4	256 kHz	8 kHz
5120 kHz	1	640 kHz	20 kHz
33868.8 kHz	3*	1411.2 kHz	44.1 kHz

*Not tested during production

2.1.7 Serial Audio Interface

The Serial Audio Interface is a 4-wire interface for bi-directional communication of audio data. It is a serial synchronous interface. It is operated on a bit serial clock BCLK and a frame synchronization signal FSYNC. Both signals are independent of MCLK; however, it is recommended to synchronize the Serial Audio Interface to the MCLK signal whenever the ADC and DAC signal chains are active. FSYNC and internal clock signal FINT (= MCLK divided by 1, 2, 3* or 4) must have a fixed ratio because FSYNC is the actual sampling frequency Fs of the 16-bit ADC and DAC codes.

Both Long Frame Sync (LFS) and Short Frame Sync (SFS) protocols are supported. The Serial Audio Interface can be used in slave or master mode. By default the Serial Audio Interface operates in slave mode. When operating in master mode, the LFS protocol is used with these parameters: FSYNC = Fs and BCLK = 32 x Fs. The device generates these two signals. See register J to toggle between the master and slave mode.

2.1.8 Mono / Stereo Operation

The device contains a single audio channel. However it can be used in a stereo system in which other devices are connected to the Serial Audio Interface. In such a system, the output of the audio interface (SDO) must be in high-impedance state whenever the device is not sending data. The SDO impedance is controlled through register J.

2.1.9 Serial Peripheral Interface - SPI

The SPI interface is used to control register values. It is a serial communications sub-system that is independent of the rest of the device. It allows the device to communicate synchronously with a microprocessor or DSP. This interface only implements the slave controller.

2.1.10 Sandman™ ADC Function

The Sandman™ function monitors the signals, which are processed in the ADC signal channel and the DAC signal channel. The logic output signal SMAD indicates whether the ADC signal channel has processed an audio signal or only noise, and for how long. A reference signal amplitude can be selected through register O, the time window parameters are the off time and on time (registers L, M and N).

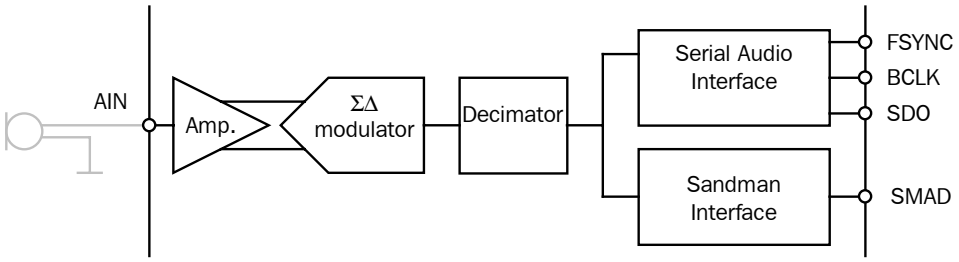


Figure 3: Implementation of the Sandman function for the ADC (SMAD)

The logic output SMAD can be used to power-down or reduce clock speed in other devices in the application, such as a microcontroller, DSP or wireless link. Also, SMAD can be used as phone pick-up indicator. The Sandman™ function is illustrated in Figure 4 and is valid for both SMAD (related to the ADC signal) and SMDA (related to the DAC signal). The illustration below is given for the SMAD signal.

Initially, SMAD is inactive (low), which means that “noise” is processed by the ADC, i.e. no audio signal amplitude above the Reference. The Sandman™ Interface compares every output sample of the ADC signal channel to the Reference value. If the signal is lower than the Reference value, SMAD remains inactive (low).

As soon as the signal passes the reference (time = 1), the on-time counter is started (see Figure 4). However, as the signal returns below the Reference (time = 2) (see Figure 4). before the on-time counter has reached the on time, the on-time counter is reset and the SMAD signal remains inactive (low).

The next time the signal gets higher than the Reference (time = 3) (see Figure 4), the on-time counter is started again and when it reaches the on time, the SMAD signal becomes active (high), indicating that an audio signal is present (time = 4). As long as the signal remains above the Reference, nothing happens and the SMAD signal remains active (high). When the signal falls below the Reference (time = 5) (see Figure 4), the off-time counter is started, but as it does not reach the off time before the signal passes again the Reference (time = 6) (see Figure 4), SMAD remains active (high). Also during the period from time = 7 to time = 8 (see Figure 4), the off time counter does not reach the off time.

When the signal falls below the Reference (time = 9) (see Figure 4) and remains below the Reference until the off-time counter has reached the off-time, the SMAD signal is changed into the inactive (low) state (time = 10) (see Figure 4).

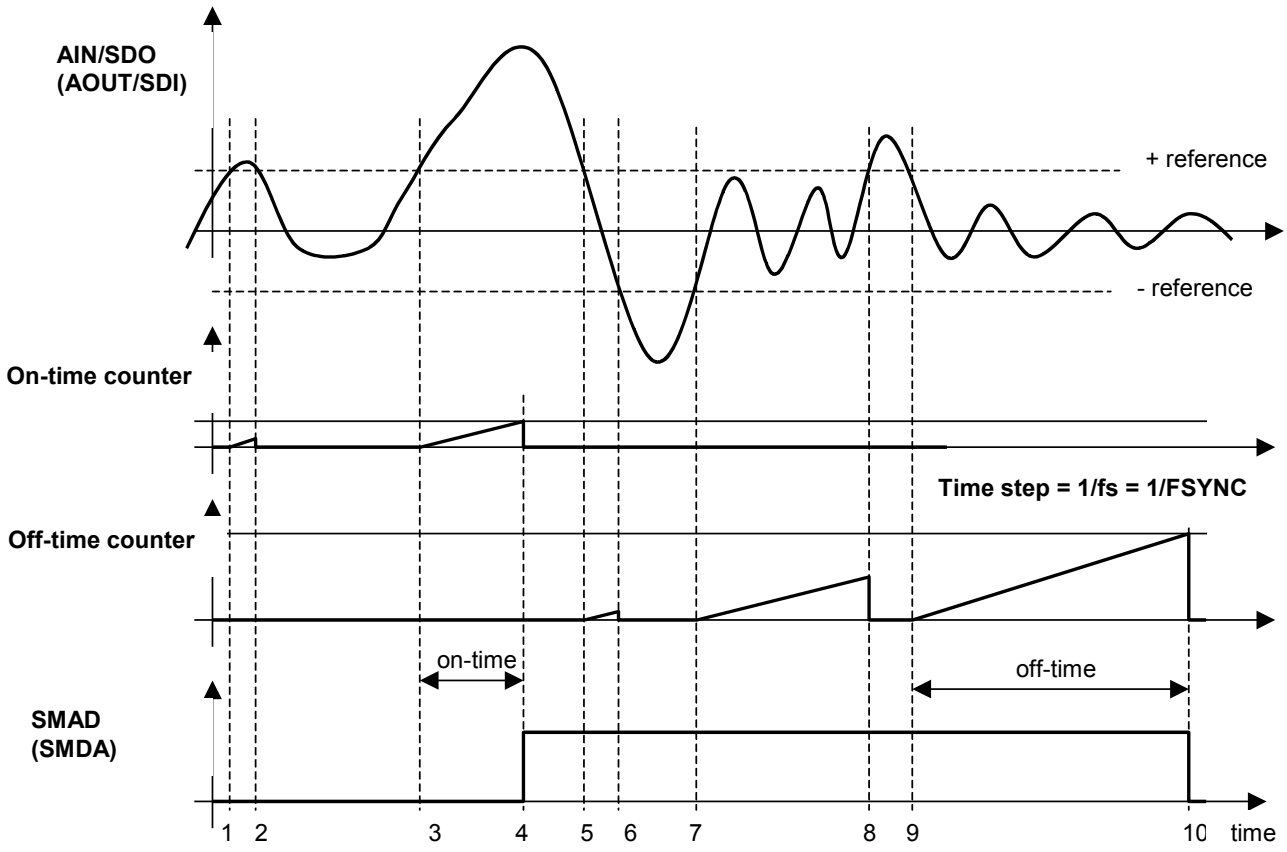


Figure 4: Illustration of the Sandman™ function.

The above illustration is valid for either the SMAD output as a result Of AIN/SDO or for the SMDA output as a function of AOUT/SDI.

2.1.11 Sandman™ DAC Function

The Sandman™ function monitors the signals, which are processed in the ADC signal, channel and the DAC signal channel. The logic output signal SMDA indicates whether the DAC signal channel processes an audio signal or only noise, and this for certain duration. A reference signal amplitude can be selected through register P, the time window parameters are the off time and on time (registers L, M and N).

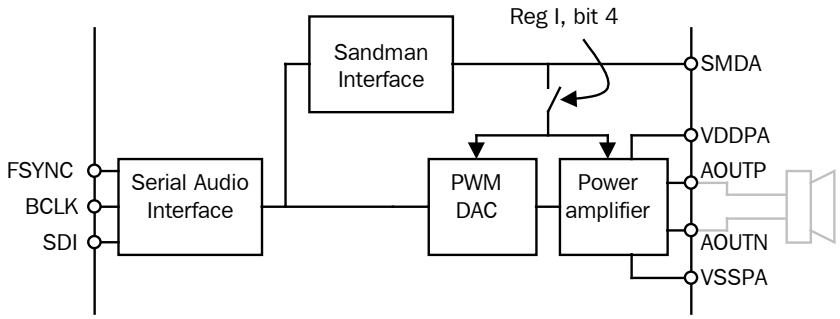


Figure 5: Implementation of the Sandman function for the DAC (SMDA)

The logic output SMDA can be employed to power-down other devices in the application, such as an external audio power amplifier. By setting bit 4 in register I, the on-chip DAC signal channel can be powered-down through SMDA too. The Sandman™ function is illustrated in Figure 4 and is valid for both SMAD (related to the ADC signal) and SMDA (related to the DAC signal).

2.2 Start-up and Initialization

The $\overline{\text{RESET}}$ signal is used to initialize the various blocks in the device and thus guarantees a correct start-up of the circuit. The start-up sequence that is automatically carried out upon power-up of the device is listed below and illustrated in Figure 6.

1) $\overline{\text{RESET}}$ is active (low) when the device is not powered and remains active (low) when VDD is applied (upper curve in Figure 6). The active (low) state remains until VDD, VREG16, VREF are stable.

2) As soon as the clock signal is present, a counter is activated that counts until 420 ms and then releases RESET in the inactive (high) state.

The overall $\overline{\text{RESET}}$ time from VDD going high until $\overline{\text{RESET}}$ turning inactive is maximum 500 ms.

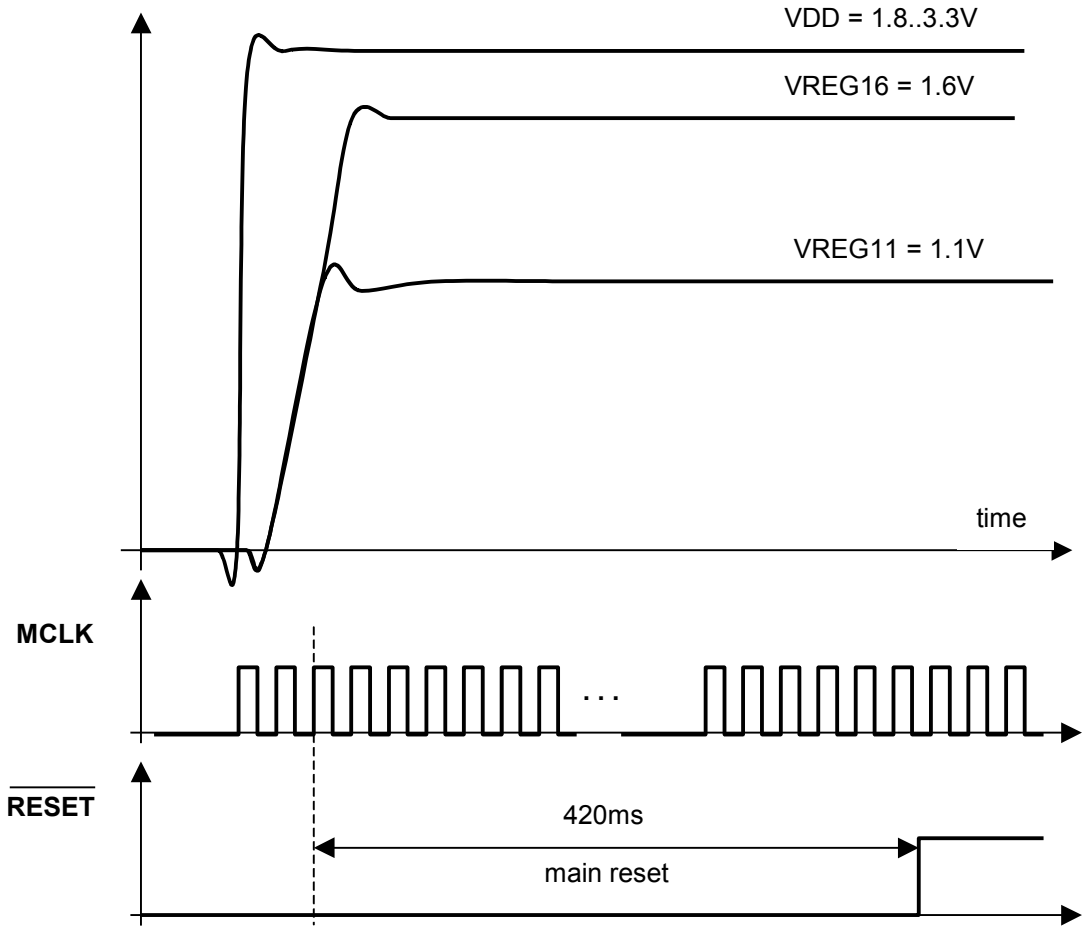


Figure 6: Startup sequence and RESET signal after power-on.

$\overline{\text{RESET}}$ is a high-impedance I/O terminal. It can be forced to "high" level by applying a logic 1 to the $\overline{\text{RESET}}$ terminal once the clock is running (any time during or after the "main reset" period indicated in Figure 6). In this way the start-up sequence of the device can be significantly reduced, however analog blocks may not yet fully comply with their specifications.

2.3 Power-Down Functions

2.3.1 Software Power-Down

Register I allows for the selective power down of the ADC signal channel or the DAC signal channel through SPI control. The wake-up time, after powering down the device totally or partially is 200us typ. The max. standby current is 96uA, this is highly dependant upon the Master clock (MCLK) see 5.3.5.2 Low Power Modes.

2.3.2 Hardware Power-Down

The device has no power-down pin. However, by holding down (Logic 0) the RESET pin (resetting the device) as well as the pins MCLK, BCLK and FSYNC, the power consumption will reach the standby current of typ.16uA. Use the standard procedure for power up (see start-up and initialization procedure) after a hardware power down and apply your registers setup procedure.

3 Serial Communications

3.1 Serial Audio Interface

The Serial Audio Interface is a 4-wire interface for bi-directional communication of audio data. It is a serial synchronous interface. The 4 terminals are listed below:

- BCLK: Bit serial clock, one clock cycle corresponds to one data bit transmitted or received.
- FSYNC: Frame Synchronization, synchronization signal indicating the start of a data word.
- SDI: Serial Data In, data received from external device and sent to DAC.
- SDO: Serial Data Out, data received from ADC and sent to external device.

The same clock (BCLK) and synchronization (FSYNC) signals are used for both sending and receiving. The synchronization signal FSYNC must have a fixed ratio with the master clock signal MCLK and equals the actual sampling frequency of the ADC and DAC.

The Serial Audio Interface supports two formats that are commonly used for audio/voice CODECs and that are referred to as SFS (Short Frame Synchronization) and LFS (Long Frame Synchronization). The two interface protocols are shown below.

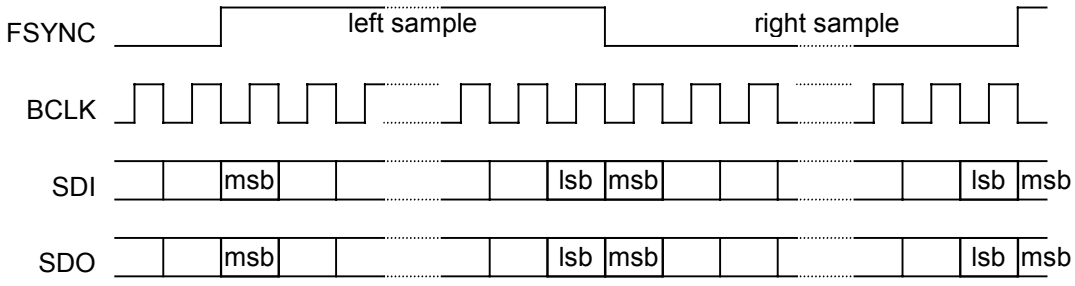


Figure 7: Audio interface signal timing in Long Frame Synchronization (LFS) mode.

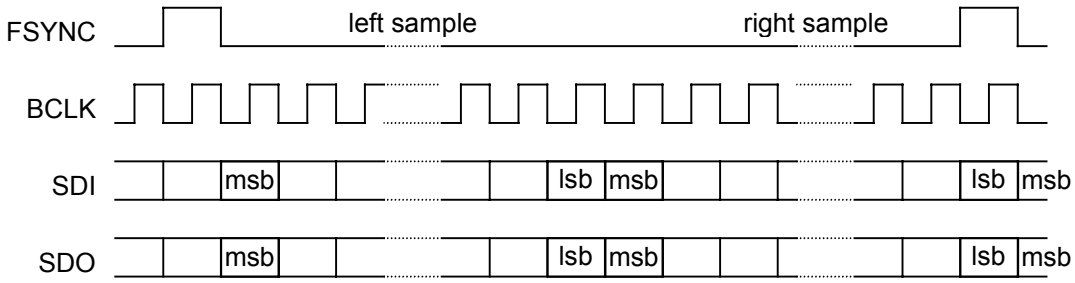


Figure 8: Audio interface signal timing in Short Frame Synchronization (SFS)mode.

In the default configuration, data is made available on the falling edge of BCLK and data is read on the rising edge of BCLK, ensuring data is always stable and correct, independent of propagation delays (as long as the clock specifications on BCLK are met).

When the bit INV_BCLK (bit 5 in register J) is set to logic 1, the active edges of the data and FSYNC are reversed: data is transmitted on the rising edge and received on the falling edge of BCLK. All data is transmitted with MSB first, and padded with '0' if necessary (i.e. when $F_{MCLK} > 16F_{sample}$). BCLK has to be synchronous with MCLK rising edge.

FSYNC selects the channel and is valid for transmission as well as reception. It is high for the left channel, and low for the right channel. The left sample is always sent first in Long and Short Frame Sync mode.

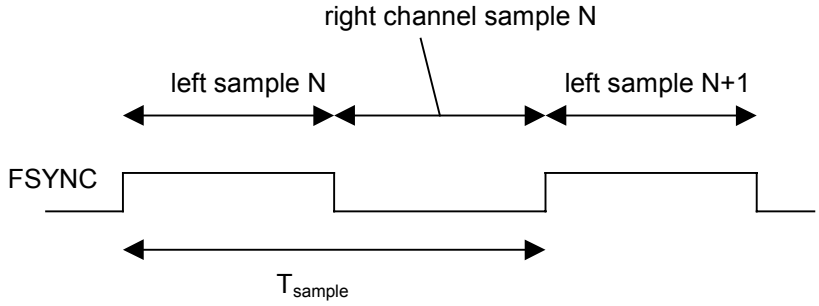


Figure 9: Left-right determination with FSYNC.

3.1.1 Recommendation when using the sync mode of the Serial Audio Interface

The minimum number of clocks (BCLK) during a sample time is at least of 32 for the Long Frame Sync mode and **fixed** to 32 for the Short Frame Sync mode. To prevent device failure do not put more than 32 clocks (BCLK) in Short Frame Sync Mode.

3.2 Serial Peripheral Interface - SPI

The serial peripheral interface (SPI), an independent serial communications sub-system, allows the device to communicate synchronously with other devices such as a microprocessor or a DSP. This interface only implements a slave controller and allows sending data from master to slave. This section describes the communication from master to slave (MOSI) and from slave to master (MISO).

Four lines are used to transmit data between the slave and master:
- MOSI (Master Out, Slave In) data from master to slave, synchronous with the SPI clock (SCK).
- MISO (Master In, Slave Out) data from slave to master, synchronous with the SPI clock (SCK).
- SCK (Serial Clock) synchronizes the data bits of MOSI and MISO.
- SS (Slave Select) Slave devices are selected by activating SS.

3.2.1 Protocol

During SPI communication, data is simultaneously transmitted and received. The interface implements the protocol with an active low clock and a clock phase 1 (slave select line doesn't have to rise between communications with the same slave).

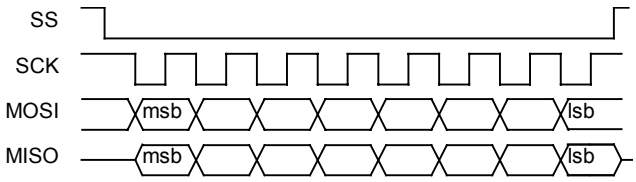


Figure 10: SPI signal timing

The master puts data on the MOSI line on the falling edge of SCK; the slave reads the data on the rising edge of SCK. The slave puts data on the MISO line on the falling edge of SCK; the master reads the data on the rising edge of SCK. Transmission in either direction is by bytes with MSB first.

There are three timing constraints:

- Recovery time ($t_{recovery}$) between the falling edge of SS and the falling edge of SCK.
- Disable time ($t_{disable}$) between the last rising edge of SCK and the rising edge of SS.
- SCK frequency (F_{SCK})

Delay	Min	Max	Unit	Comments
$t_{recover}$	125	-	ns	
$t_{disable}$	2 x T_{master}	-	Hz	T_{master} = clock period of the master clock MCLK
F_{SCK}		0.5 x F_{master}	ns	F_{master} = frequency of the master clock MCLK

3.2.2 Interface Modes

There are three interface modes: read mode, write mode and write_auto mode.

3.2.2.1 Read Mode

In this mode, a read request is sent on the MOSI line and the content of a register is dumped on the MISO line. The byte to transfer has the following format :

bit	7	6	5	4	3	2	1	0
	1	1	0	address(4:0)				

bit	7	6	5	4	3	2	1	0
	data(7:0)							

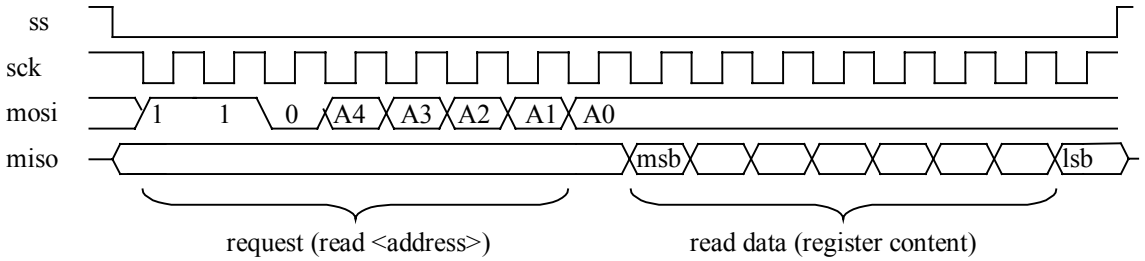


Figure 11: SPI signal timing in read mode

3.2.2.2 Write Mode

Write communication always takes place in pairs of bytes. The format of the 2 bytes is:

Bit	7	6	5	4	3	2	1	0
	1	0	0	address(4:0)				

Bit	7	6	5	4	3	2	1	0
	data(7:0)							

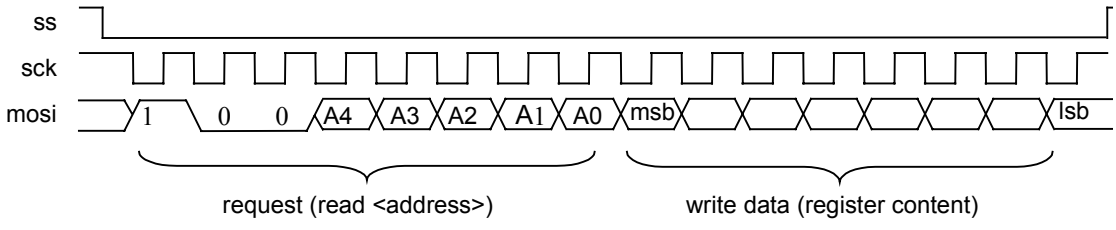


Figure 12: SPI signal timing in write mode

3.2.2.3 Write_Auto Mode

In this mode, the registers are written in sequence from a given start address to the last address b10111 (0x17). The format is :

bit	7	6	5	4	3	2	1	0
	1	0	1	start_address(4:0)				

bit	7	6	5	4	3	2	1	0
	data(7:0) for register start_address							

bit	7	6	5	4	3	2	1	0
	data(7:0) for register start_address + 1							

bit	7	6	5	4	3	2	1	0
	data(7:0) for register b10111 (0x17)							

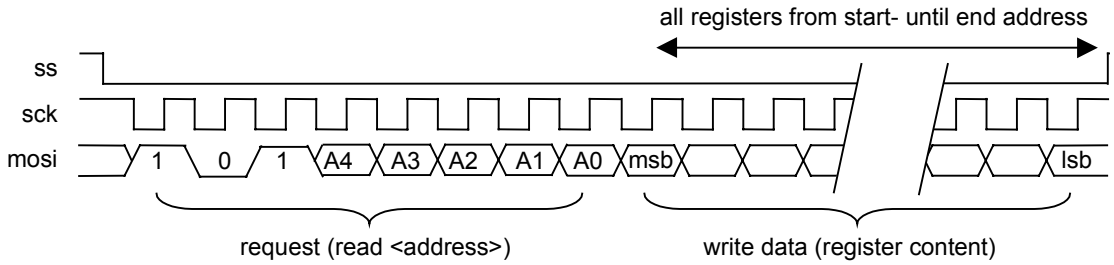


Figure 13: SPI signal timing in write_auto mode

Exit from write_auto mode happens only when address b10111 (0x17) is reached.

When using the write_auto mode fill the reserved registers with the default value in order to prevent any malfunction.

See the detailed register description provided in chapter 8.

3.3 Register Programming

The control registers set the configuration of the device and can bring the chip into various modes of operation. The control registers can be set in the following ways:

1) Default hard-coded value
The hardcode values are the default values of the registers as provided in this section. This hard-coded configuration can be customized by means of a metal mask. This option can lead to a reduced chip price for high-volume applications. Contact any XEMICS sales representative for more information on this option.

2) Values at SPI pins during power-up, overrules 1)
During power-up, the digital values at the SPI interface connections are read. If these pins are not forced externally to logic 1 or 0 value, the default values will be active. By actively forcing one or more of the SPI pins to a logic 1 or 0 value, three register values can be set, as explained in the table below.

SPI pin	Register and bit	default	Toggled
SS	Register I, bit 0	SS = 1, MCLKDIV0 = 0, division by 1	SS = 0, MCLKDIV0 = 1, division by 2
SCK	Register J, bit 0	SCK = 0, PROTOCOL = 1, SFS protocol	SCK = 1, PROTOCOL = 0, LFS protocol
MOSI	Register E, bit 2	MOSI = 0, PREAMP_GAIN = 0, gain x4	MOSI = 1, PREAMP_GAIN = 1, gain x20

3) Programming through SPI interface after power-up, overrules 1) and 2)
Once the device has been powered up, the configuration registers can be modified at all times (also when the device is active) through the SPI interface. See section on SPI.

3.3.1 Control Register Space Overview

The control register set consists of 24 registers. A detailed description is provided chapter 8.

4 Sandman™ Function (applies to XE3006)

The Sandman™ function analyzes the audio signals in the ADC and DAC. Its output signals indicate whether an audio signal is present in the ADC or DAC or if the processed signal is just noise. The threshold or reference value between noise and audio signal as well as the minimum duration of an audio signal is user-programmable through the SPI interface. If the XE3006 CODEC is used in a system that includes a microcontroller, a DSP or an RF link, the outputs of the Sandman Interface can be used to bring these devices into standby or sleep mode whenever no audio signal is being processed. In this way, the Sandman™ function contributes to significant additional power savings on the system level outside the XE3006 chip.

The Sandman™ Interface consists of 2 digital outputs:

- The SMAD detects whether the ADC processes an audio signal. The calculation is made with the digital data leaving the ADC.
- The SMDA detects whether an audio signal is processed by the DAC. The calculation is made with the digital data entering through the Audio Interface.

The Sandman™ Interface is implemented for the ADC and for the DAC in an identical way. It works with a set of 4 user-defined parameters: off time, on-time, ADC-reference and DAC-reference. The on time and the off time are the same for ADC and DAC. However, the reference values for the ADC and the DAC are adjusted separately, as indicated in the table below.

Input parameters	Register	Sandman ADC	Sandman DAC
Off-time1(7:0)	L	X	X
Off-time2(15:8)	M	X	X
On-time(7:0)	N	X	X
ADC_reference(7:0)	O	X	-
DAC_reference(7:0)	P	-	X

The Sandman™ Interface (for the ADC as well as for the DAC) is configured with three parameters:

- **Reference (7:0):** absolute value under which the signal is considered noise and above which the signal is considered to be an audio signal. The Sandman™ function is disabled (SMAD or SMDA at logic 1) if this parameter is zero. The ADC and the DAC have separate Reference values.
- **Off time (15:0):** time until power down. The number of sequential samples that have to be lower than the Reference for the power down signal to become active. The Sandman™ function is disabled (SMAD or SMDA at logic 1) if this parameter is zero. The ADC and DAC have one common Off-time value.
- **On time (7:0):** time until wakeup. The number of sequential samples that have to be higher than the Reference for the power down signal to become inactive. The Sandman™ function is disabled (SMAD or SMDA at logic 1) if this parameter is zero. The ADC and DAC have one common On-time value.

All these parameters are set in the registers L, M, N, O and P.

Reference(7:0)	On-time(7:0)	Off-time(15:0)	Sandman (SMAD or SMDA)	Comments
0	don't care	don't care	logic 1 (disable function)	Sandman disable
don't care	0	don't care	logic 1 (disable function)	Sandman disable
don't care	don't care	0	logic 1 (disable function)	Sandman disable
1.-.255 corresponds to 128.-.32640	1.-.255 corresponds to 50 µs – 12 ms	1 - 65535 corresponds to 50 µs - 3.2 sec	logic 1 (signal higher than ref) logic 0 (signal lower than ref)	all registers ≠ zero time for fs = 20kHz

The reference (7:0) value is related to the absolute value of the 16 bits input signal. The following format is used for the comparison:

- 16 bit inputs data (2's-complement) : 0**111'1111'1**111'1111 = 0x7FFF max positive value
- 8 bit reference (unsigned) : 0**111'1111'1**000'0000 = 0xFF00/2 reference max

So the reference is compared to the 8 most significant bits of the absolute value of the input signal:

reference(7:0)	Absolute reference	AIN (mV) if gain = 4	AIN (mV) if gain = 20
0	0	0.00	0.00
1	128	1.10	0.27
2	256	2.20	0.55
255	$255 \times 128 = 32640$	280	70

The values in this table are amplitude values, RMS values can be derived by dividing the numbers by $\sqrt{2}$.

The working mechanism of the Sandman™ function is the following:
The incoming data are compared to the reference after each time step (1/FSYNC = 50us if FSYNC = 20kHz):

- **During the on time phase**
  - If the input data is higher than the reference, a counter will be incremented else the counter is reset.
  - When the counter reaches the on time value, then the SMAD or SMDA signal is activated (high level)
- **During the off time phase**
  - If the input data is lower than the reference, a counter will be incremented else the counter is reset.
  - When the counter reaches the off time value, then the SMAD or SMDA signal is disactivated (low level)

In a first approximation, the following points are recommended:

- On time at least 1ms. If the on time is shorter than 1 ms, the Sandman™ function becomes sensitive to spikes in the audio input signal AIN.
- Off-time at least 10ms, the off time should be longer than $1/f_{min}$ = 10ms, (code = 200). f_{min} is the minimum audio frequency = 100Hz if FSYNC = 20kHz. The value of f_{min} scales proportionally with the sampling frequency FSYNC. A high-pass filter in the ADC filters out signals below 100Hz.
- Reference should be adjusted just above the noise level

The CODEC bandwidth is around 100Hz to 10kHz at the nominal system frequency (MCLK = 5MHz, CKDIV = 1, FSYNC = 20kHz).

In digital loopback mode, the data entering into the Audio Interface are not transferred to the DAC. However, the Sandman™ function (if activated) continues to output the SMDA signal based on the data entered into the Audio Interface (input terminal SDI).

5 Specifications

5.1 Absolute Maximum Ratings

Stresses above those listed in the following table may cause permanent failure. Exposure to absolute ratings for extended periods may affect device reliability.

The values are in accordance with the Absolute Maximum Rating System (IEC 134).
All voltages referenced to ground (VSSA and VSSD).
Analog and digital grounds are equal (VSSA = VSSD).

Symbol	Parameter	Conditions	Min	Max	Unit
VDD	Supply voltage		-0.3	3.65	V
Tstg	Storage temperature		-65	150	°C
TA	Operating free-air temperature, TA		-40	85	°C
Ves	Electrostatic discharge protection	1) and 2)		2000	V
Ilus	Static latchup current	3)	10	98	mA
Vlud	Dynamic latchup voltage	3)		50	V

1) Tested according MIL883C Method 3015.6 (Standardized Human Body Model: 100 pF, 1500 Ω, 3 pulses, protection related to substrate).
2) For startup purposes, VREF is not protected against positive discharges.
AOUTP and AOUTN are not protected against positive or negative discharges (ESD protection diodes are not possible on these output pins because they would potentially be forward-biased during regular operation).
3) Static and dynamic latchup values are valid at 27 °C.

5.2 Recommended Operating Conditions

All voltages referenced to ground (VSSA and VSSD)

	Min	Typ	Max	Unit
Supply voltage, VDD	1.8		3.65	V
Analog signal peak-to-peak input voltage, AIN (gain = 20x)			65	mV
Analog signal peak-to-peak input voltage, AIN (gain = 5x)			270	mV
Differential output load resistance	16			Ohm
Master clock frequency	1.024		33	MHz
ADC or DAC conversion rate			48	kHz
Operating free-air temperature, TA	-40		85	°C

5.3 Electrical Characteristics Over Recommended Operating Conditions, VDD = 3.0 V, T = 25°C

5.3.1 Digital Inputs and Outputs, Fs = 20 kHz, output not loaded

	Parameter	Test Conditions	Min	Typ	Max	Unit
VOH	High-level output voltage, DOUT	IO = -360uA	2.4		VDD+0.5	V
VOL	Low-level output voltage, DOUT	IO = 2mA	VSSD-0.5		0.4	V
IIH	High-level input current, any digital input	VIH = 3.3 V			10	uA
IIL	Low-level input current, any digital input	VIL = 0.6 V			10	uA
Ci	Input capacitance				10	pF
Co	Output capacitance				10	pF

5.3.2 ADC Dynamic Performance, Fs = 20 kHz

	Parameter	Test Conditions	Min	Typ	Max	Unit
SNR	Signal-to-noise ratio	Pre-amp gain = 5x Vin=250mV (full scale)	72	80		dB
THD	Total harmonic distortion	¼ full scale		0.5		%
Flo	Low cut-off frequency (-3 dB), See Note 1	FSYNC = 20 kHz	60	70	80	Hz
Fhi	High cut-off frequency (-3 dB), See Note 2	FSYNC = 20 kHz		10		kHz
GD	Group delay	FSYNC = 20 kHz			150	us

Note 1) Flo is proportional to FSYNC
Note 2) Fhi equals FSYNC / 2

5.3.3 ADC Channel Characteristics, Fs = 20 kHz

	Parameter	Test Conditions	Min	Typ	Max	Unit
Vipp	Peak-to-peak input voltage (single ended)	Pre-amp gain = 5x Pre-amp gain = 20x			270 65	mV
Vneq	Equivalent input noise	A-weighted, 100 Hz-10 kHz pre-amp gain = 20x			50	uV rms
	Dynamic range	Pre-amp gain = 20 Vin=250mV (full scale)		80		dB
PSRR	Power supply rejection ratio, input referred	Up to 1 kHz		60		dB
Rs	Input load resistance, See Note 1			4		KOhm
Rin	Input resistance VIN – VSSA		1			MOhm
Eg	gain error	VDD 1.8-3.3V		+/- 0.1		[%]
	offset error	VDD 1.8-3.3V		-60		LSB
	input noise	VDD 1.8-3.3V		6.7		LSB
INL	Integral non linearity	VDD 1.8-3.3V		+/- 5		LSB
DNL	Differential non linearity	VDD 1.8-3.3V		+/- 0.1		LSB

Note 1) Refers to electret microphone load

5.3.4 DAC Dynamic Performance, load is an LC filter at 10kHz

FSYNC = 20kHz, MCLK = 5MHz, for info on the LC filter see the application information

	Parameter	Test Conditions	Min	Typ	Max	Unit
SNR	Signal-to-noise ratio	Bandwidth 10kHz		60		dB
THD	Total harmonic distortion	¼ full scale		0.5		%
	Dynamic range	Bandwidth 10kHz		60		dB
GD	Group delay	FSYNC = 20 kHz			150	µs

Note 1) No filtering is applied to the DAC

5.3.5 Power Supply

5.3.5.1 Regulated supply characteristics @ T = 25°C

	Parameter	Test Conditions	Min	Typ	Max	Unit
VREF	Reference Voltage	1uF capa (1) Do not load		1.22		V
VREG11	Regulated Voltage 1.1V			1.07		V
VREG16	Regulated Voltage 1.6V	1uF capa 820K res (1)		1.63		V
VREF PSRR	Power supply rejection ratio, input referred	Up to 1 kHz		60		dB
VREG11 PSRR	Power supply rejection ratio, input referred	Up to 1 kHz		60		dB
VREG16 PSRR	Power supply rejection ratio, input referred	Up to 1 kHz		40		dB

Note 1): See external components required for optimal performances

5.3.5.2 Low power mode

Stand-by mode @ VDD = 3.3V, T = 25°C

	Parameter	Test Conditions	Min	Typ	Max	Unit
Istb1	Supply current in standby mode	ADC off, DAC off MCLK = 5 MHz,		28	56	µA
Istb2	Supply current in standby mode	ADC off, DAC off MCLK = 12.2880 MHz		48	96	µA
Istb3	Supply current in standby mode	RESET mode MCLK = 0		16	32	µA

Stand-by mode @ VDD = 1.8V, T = 25°C

	Parameter	Test Conditions	Min	Typ	Max	Unit
Istb1	Supply current in standby mode	ADC off, DAC off MCLK = 5 MHz,		25	50	µA
Istb2	Supply current in standby mode	ADC off, DAC off MCLK = 12.2880 MHz		31	62	µA
Istb3	Supply current in standby mode	RESET mode MCLK = 0		16	32	µA

5.3.5.3 Normal operation, output load consumption is not included.

Normal operations @ VDD = 3.3V, Fs = 20kHz, T = 25°C, Register C = 0xF0

	Parameter	Test Conditions	Min	Typ	Max	Unit
IDD	Supply current CODEC	ADC on, DAC on fs = 20 kHz, no load		350	700	µA
IADC	Supply current ADC	ADC on, DAC off fs = 20 kHz, no load		240	480	µA
IDAC	Supply current DAC	ADC off, DAC on fs = 20 kHz, no load		120	240	µA

Normal operations @ VDD = 3.3V, Fs = 48 kHz, T = 25°C, Register C = 0xD4

	Parameter	Test Conditions	Min	Typ	Max	Unit
IDD	Supply current CODEC	ADC on, DAC on fs = 48 kHz, no load		860	1720	µA
IADC	Supply current ADC	ADC on, DAC off fs = 48 kHz, no load		600	1200	µA
IDAC	Supply current DAC	ADC off, DAC on fs = 48 kHz, no load		280	560	µA

Normal operations @ VDD = 1.8V, Fs = 20kHz, T = 25°C, Register C = 0xF0

	Parameter	Test Conditions	Min	Typ	Max	Unit
IDD	Supply current CODEC	ADC on, DAC on fs = 20 kHz, no load		250	500	µA
IADC	Supply current ADC	ADC on, DAC off fs = 20 kHz, no load		200	400	µA
IDAC	Supply current DAC	ADC off, DAC on fs = 20 kHz, no load		65	130	µA

Normal operations @ VDD = 1.8V, Fs = 48 kHz, T = 25°C, Register C = 0xD4

	Parameter	Test Conditions	Min	Typ	Max	Unit
IDD	Supply current CODEC	ADC on, DAC on fs = 48 kHz, no load		625	1250	µA
IADC	Supply current ADC	ADC on, DAC off fs = 48 kHz, no load		505	1010	µA
IDAC	Supply current DAC	ADC off, DAC on fs = 48 kHz, no load		140	280	µA

5.3.6 Timing Requirements (see Parameter Measurement Information)

5.3.6.1 Serial Audio Interface Timing

Ref. No.	Characteristics	Test Conditions	Min	Typ	Max	Unit
1	Master Clock Frequency for MCLK = 1/ T	C_{Load} = 10pF	1024	5.12	33	MHz
1	MCLK Duty Cycle		45		55	%
2	Rise Time for All Digital Signals				10	ns
3	Fall Time for All Digital Signals				10	ns
4	Hold time BCLK or FSYNC high after MCLK low		T/4			ns
5	Setup time BCLK or FSYNC high to MCLK low		T/4			ns
6	Hold time BCLK or FSYNC low after MCLK low		T/4			ns
7	Setup time BCLK or FSYNC low to MCLK low		T/4			ns
8	Bit Clock Frequency for BCLK = 1 / T_{BCLK}			32xFs (1)	MCLK/2 (2)	MHz
9	Setup time data input SDI to BCLK low		T_{BCLK}/4			ns
10	Hold time data input SDI after BCLK low		T_{BCLK}/4			ns
11	Delay time SDO valid after BCLK high				T_{BCLK}/4	ns
12	Setup time data input FSYNC to BCLK low		T_{BCLK}/4			ns
13	Hold time data input FSYNC after BCLK low		T_{BCLK}/4			ns

Note 1) Fs = FSYNC: sampling frequency
Note 2) Only valid for Long Frame Sync mode

5.3.6.2 Serial Peripheral Interface SPI Timing

Ref. No.	Characteristics	Test Conditions	Min	Typ	Max	Unit
1	Serial Clock Frequency for SCK = 1 / T_{SCK}	C_{Load} = 10pF			MCLK/2	MHz
1	MCLK Duty Cycle		45		55	%
2	Recovery Time		125			ns
3	Disable Time		2T			ns
4	Setup time MISO valid to SCK high		T_{SCK}/4			ns
5	Hold time MISO valid after SCK high		T_{SCK}/4			ns
6	Delay time MOSI valid after SCK low		T_{SCK}/4			ns

6 Parameter Measurement Information

6.1 Serial Audio Interface in Long Frame Sync Mode

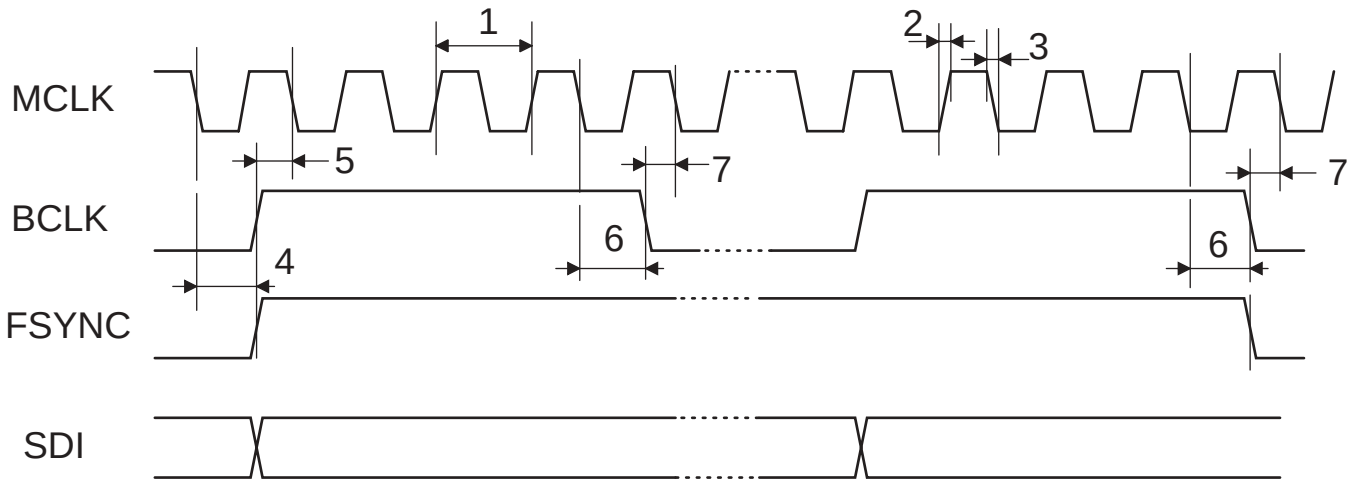


Figure 14: Long Frame Sync data valid on falling edge, MCLK vs BCLK and FSYNC

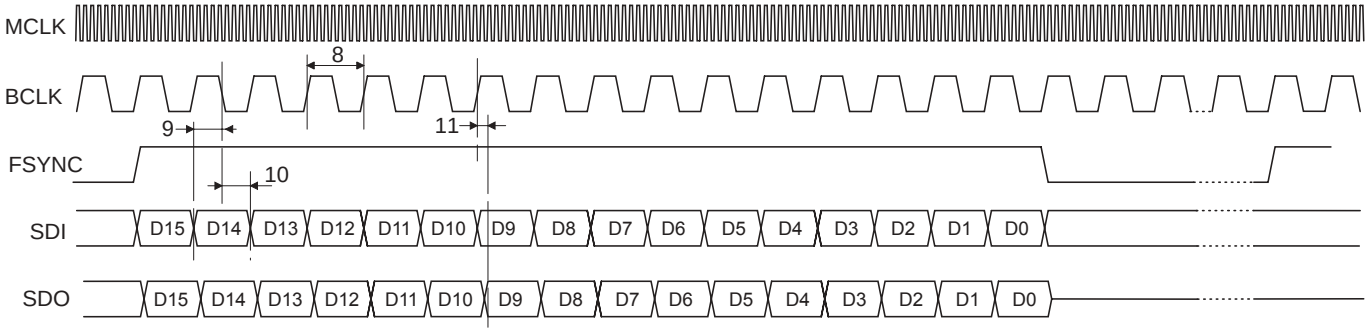


Figure 15: Long Frame Sync mode, Data valid on Falling Edge, BCLK vs Data IO

See register J for protocol settings and BCLK edge settings.

6.2 Serial Audio Interface in Short Frame Sync Mode

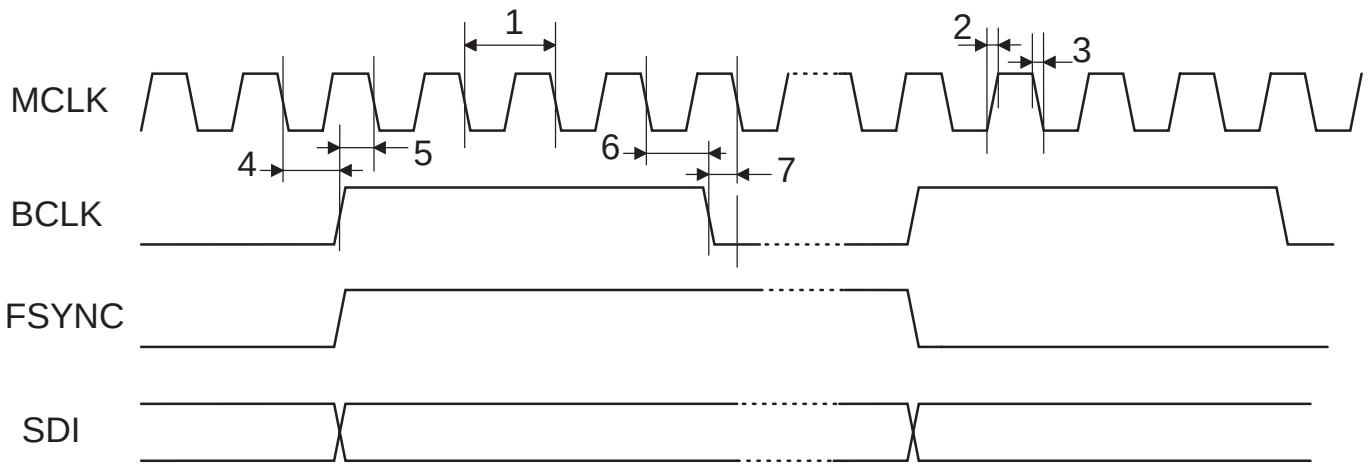


Figure 16: Short Frame Sync data valid on falling edge, MCLK vs BCLK

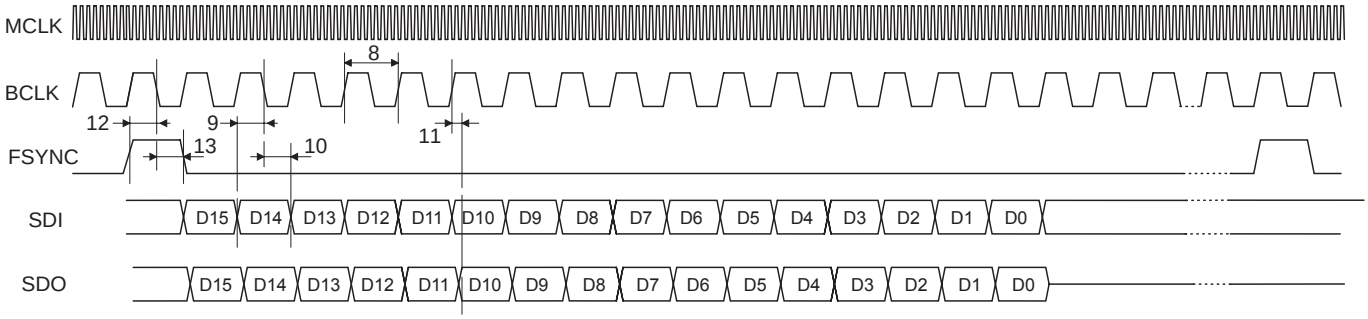


Figure 17: Short Frame Sync mode, Data valid on Falling Edge, BCLK vs FSYNC and Data IO

See register J for protocol settings and BCLK edge settings

6.3 Serial Peripheral Interface (SPI)

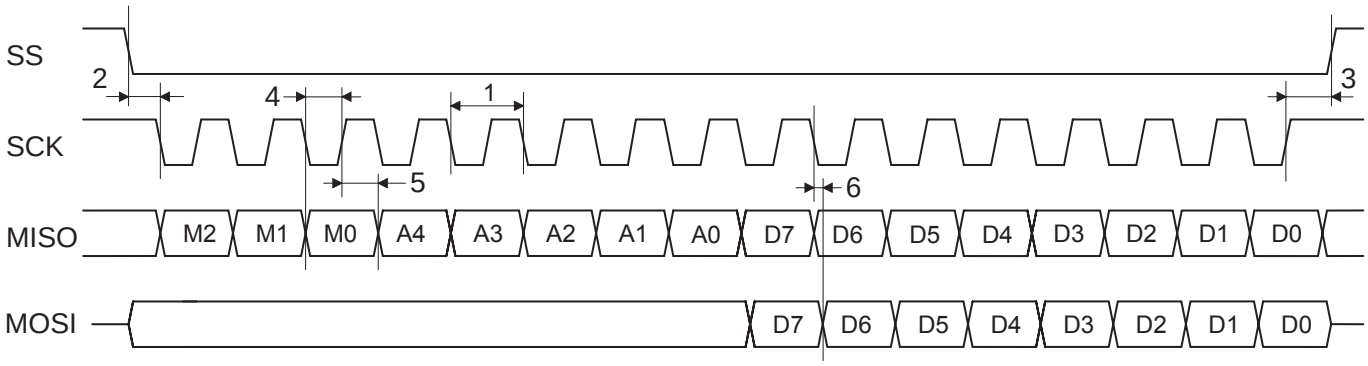


Figure 18: Serial Peripheral Interface general timing, data valid on rising edge

7 Application Information

7.1 Application Schematics

7.1.1 Typical Application

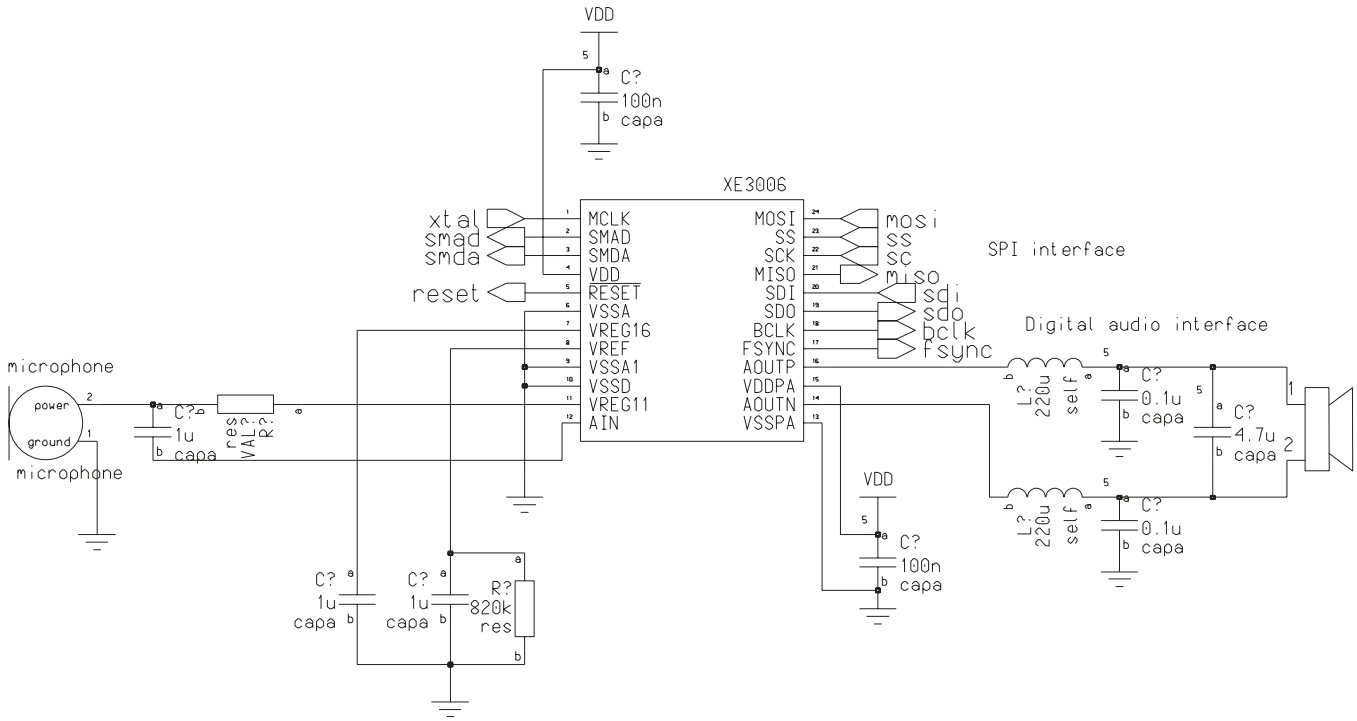


Figure 19: Typical Application with LC output Filter

7.1.2 External components required for optimal performances

The following minimum set-up of external components are required.

- Capacitor for Vref: 1uF
- Resistor for Vref: 820KΩ
- Capacitor for VREG16: 1uF

Recommendation for both capacitors Z5U or Y5V ceramic capacitor (0805, Rdc > 100MΩ).

The supply voltage and ground should be “clean”. Therefore, it is recommended to stabilize the supply voltage with a 100nF capacitor between VDD, VSSA/VSSD and VDDPA/VSSPA.

A ground plane should connect the different VSS pin as close as possible from these VSS pins

7.1.3 How to use the ADC when Fs > 20kHz

By default and in order to save power consumption, the ADC has been designed to run from 4kHz to 20kHz.

When used with a sampling frequency from 21kHz to 48kHz, the ADC default settings will need changing in order to get the best results.
To run the ADC chain with the same characteristics as it is used at a lower sampling frequency, it is necessary to tune the current reference used by the ADC using the register C.

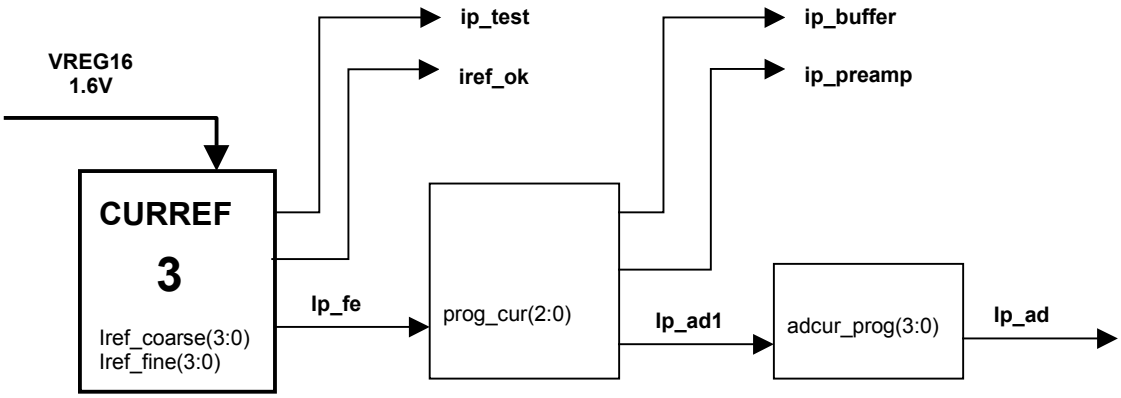


Figure 20: ADC internal current flow

The values for register C are:

Sampling Frequency = 4kHz to 20kHz, register C = Default value = 0xF0
Sampling Frequency = >20kHz to 48kHz register C = 0XD4

8 Register Description

8.1 Register Functional Summary

The following registers can be programmed by the SPI to configure the operation modes. See also section 3.3 Register Programming.

Register C	ADC current tuning. The data in this register has the following functions:
	• Adjust the ADC current for sampling frequency > 20kHz
	• C=0xF0 for Fs<= 20kHz, C=0xD4 for Fs > 20kHz.
Register E	Analog Input. The data in this register has the following functions:
	• Enable/disable microphone bias source of 1.1 V
	• Gain setting of pre-amplifier.
Register I	Function enable and clock division. The data in this register has the following functions:
	• Enable/disable Sandman function of DAC
	• Enable/disable DAC channel (DAC, power amplifier)
	• Enable/disable ADC channel (pre-amplifier, ADC, decimation filter)
	• Division of master clock
Register J	Audio Interface Configuration. The data in this register has the following functions:
	• Enable/disable digital loopback
	• Frame select receive
	• Select rising / falling edge validation of BCLK
	• Select master / slave mode
	• Output impedance
	• Frame select transmit
	• Select short / long frame sync
Register L	Sandman™ function, off-time, low byte. The data in this register has the following function:
	• Define off-time (low byte) of the Sandman™ function
Register M	Sandman™ function, off-time, high byte. The data in this register has the following function:
	• Define off-time (high byte) of the Sandman™ function
Register N	Sandman™ function, on time. The data in this register has the following function:
	• Define on-time of the Sandman™ function
Register O	Sandman™ function, reference for ADC. The data in this register has the following function:
	• Define reference amplitude for ADC for Sandman™ function
Register P	Sandman™ function, reference for DAC. The data in this register has the following function:
	• Define reference amplitude for DAC for Sandman™ function

8.2 Register Definitions XE3005

The complete register setup consists of 24 registers of 8 bits each, as shown in the table below. The “reserved” registers are preconfigured with the default values as given in the table below. The registers C, E, I and J can be used to configure the XE3005 as explained below.

Register	Address (hex)	Name	Default value (hex)
A	0x00	Reserved	0x48
B	0x01	Reserved	0x8F
C	0x02	ADC current tuning	0xF0
D	0x03	Reserved	0x00
E	0x04	Analog input and clock	0x08
F	0x05	Reserved	0x82
G	0x06	Reserved	0x00
H	0x07	Reserved	0x00
I	0x08	Block on/off and clock division	0x00
J	0x09	Audio interface configuration	0x25
K	0x0A	Reserved	0x00
L	0x0B	Reserved	0x00
M	0x0C	Reserved	0x00
N	0x0D	Reserved	0x00
O	0x0E	Reserved	0x00
P	0x0F	Reserved	0x00
Q	0x10	Reserved	0x3C
R	0x11	Reserved	0x00
S	0x12	Reserved	0x30
T	0x13	Reserved	0x00
U	0x14	Reserved	0xFF
V	0x15	Reserved	0x00
W	0x16	Reserved	0x00
X	0x17	Reserved	0x00

Register	Address (hex)	Name	Default value (hex)
C	0x03	ADC current tuning	0xF0

bit	Name	Default	Description
(7:4)	adcur_mir_prog (3:0)	1111	tune current of ADa (ip_ada). Default = 1111 current factor = {4-prog(0)-2prog(1)} / {4-prog(2)-2prog(3)} 0 4 8 **c** ¦¦ 4/4 4/3 4/2 **4/1** 1 5 9 **d** ¦¦ 3/4 3/3 3/2 **3/1** 2 6 a **e** ¦¦ 2/4 2/3 2/2 **2/1** 3 7 b **f** ¦¦ 1/4 1/3 1/2 **1/1**
(2:0)	prog_cur(2:0)	0	used for fe_cur: (currents for bufmic, AD, preamp) current factor = (2+prog_cur(2)) / (2+ prog_cur(1)+ prog_cur(0)) ½ -> (3) ¦¦ 2/3 -> (1,2) ¦¦ ¾ -> (7) ¦¦ 1x -> (0,5,6) ¦¦ 3/2 -> (4)

Register	Address (hex)	Name	Default value (hex)
E	0x04	Analog input and clock	0x08

Bit	Name	Default	Description
7	VMIC_EN	0	1: enables,0: disables the generation of the microphone supply VREG11
6:3		0001	Reserved
2	PREAMP_GAIN	0	Gain of preamplifier: 0: 5x (280 mV pp), 1: 20x (70 mV pp)
1:0		00	Reserved

Register	Address (hex)	Name	Default value (hex)
I	0x08	Block on/off and clock division	0x00

Bit	Name	Default	Description
7:4		0000	Reserved
3	EN_DAC	0	0: enable, 1: disable complete DA converter (DAC + PA)
2	EN_ADC	0	0: enable, 1: disable complete AD converter (Preamp + ADC + decimator)
1:0	MCLKDIV	00	Division factor of the master clock 00: 1, 01: 2, 10: 3*, 11: 4

*Not tested in production

Register	Address (hex)	Name	Default value (hex)
J	0x09	Audio interface configuration	0x25

Bit	Name	Default	Description
7	LOOPBACK	0	0: disable, 1: enable loopback => connect ADC output to DAC input
6	RX_FIRST_ SECOND	0	0: Receive audio data in the first 16-bit frame after the frame synchronization. 1: Receive audio data in the second 16-bit frame after the frame synchronization.
5	INV_BCLK	1	Inverse BCLK for Tx and Rx modes. 1: data valid on rising edge, 0: data valid on falling edge.
4	MASTER	0	1: enable audio interface in master mode: LFS protocol, SCK = 32 x Fs and FSYNC = Fs. 0: audio interface in slave mode.
3	SDO_HI_EN	0	0: SDO is continuously in output mode. 1: SDO is in output mode when transmitting data and is automatically. Switched into high-impedance state when no data is transmitted.
2	TX_FIRST	1	1: transmit the audio data in the first 16-bit frame after the frame synchronization. 0: do no transmit data in the first frame.
1	TX_SECOND	0	1: transmit the audio data in the second 16-bit frame after the frame synchronization. 0: do no transmit data in the second frame.
0	PROTOCOL	1	1: Short Frame Synchronization mode (inverse clock and slave mode). 0: Long Frame Synchronization mode (clock inverse or normal, mode master or slave).

8.3 Register Definitions XE3006

The control register space consists of 24 registers of 8 bits each, as shown in the table below. The “reserved” registers are preconfigured with the default values as given in the table below. The other registers (C, E, I, J, L, M, N, O, P) can be used to configure the XE3006 as explained below.

Register	Address (hex)	Name	Default value (hex)
A	0x00	Reserved	0x48
B	0x01	Reserved	0x8F
C	0x02	ADC current tuning	0xF0
D	0x03	Reserved	0x00
E	0x04	Analog input and clock	0x08
F	0x05	Reserved	0x82
G	0x06	Reserved	0x00
H	0x07	Reserved	0x00
I	0x08	Block on/off and clock division	0x00
J	0x09	Audio interface configuration	0x25
K	0x0A	Reserved	0x00
L	0x0B	Sandman function, off-time byte 1	0x00
M	0x0C	Sandman function, off-time byte 2	0x00
N	0x0D	Sandman function, on-time	0x00
O	0x0E	Sandman function, reference for ADC	0x00
P	0x0F	Sandman function, reference for DAC	0x00
Q	0x10	Reserved	0x3C
R	0x11	Reserved	0x00
S	0x12	Reserved	0x30
T	0x13	Reserved	0x00
U	0x14	Reserved	0xFF
V	0x15	Reserved	0x00
W	0x16	Reserved	0x00
X	0x17	Reserved	0x00

Additional Registers for XE3006

Register	Address (hex)	Name	Default value (hex)
C	0x03	ADC current tuning	0xF0

bit	Name	Default	Description
(7:4)	adcur_mir_prog (3:0)	1111	tune current of ADa (ip_ada). Default = 1111 current factor = {4-prog(0)-2prog(1)} / {4-prog(2)-2prog(3)} 0 4 8 **c** ¦¦ 4/4 4/3 4/2 **4/1** 1 5 9 **d** ¦¦ 3/4 3/3 3/2 **3/1** 2 6 a **e** ¦¦ 2/4 2/3 2/2 **2/1** 3 7 b **f** ¦¦ 1/4 1/3 1/2 **1/1**
(2:0)	prog_cur(2:0)	0	used for fe_cur: (currents for bufmic, AD, preamp) current factor = (2+prog_cur(2)) / (2+ prog_cur(1)+ prog_cur(0)) ½ -> (3) ¦¦ 2/3 -> (1,2) ¦¦ ¾ -> (7) ¦¦ 1x -> (0,5,6) ¦¦ 3/2 -> (4)

Register	Address (hex)	Name	Default value (hex)
E	0x04	Analog input and clock	0x08

Bit	Name	Default	Description
7	VMIC_EN	0	1: enables,0: disables the generation of the microphone supply VREG11
6:3		0001	Reserved
2	PREAMP_GAIN	0	Gain of preamplifier: 0: 5x (280 mV pp), 1: 20x (70 mV pp)
1:0		00	Reserved

Register	Address (hex)	Name	Default value (hex)
I	0x08	Block on/off and clock division	0x00

Bit	Name	Default	Description
7:5		000	Reserved
4	SMDA_EN	0	1: enable, 0: disable Sandman function for the DAC and PA
3	EN_DAC	0	0: enable, 1: disable complete DA converter (DAC + PA)
2	EN_ADC	0	0: enable, 1: disable complete AD converter (Preamp + ADC + decimator)
1:0	MCLKDIV	00	Division factor of the master clock 00: 1, 01: 2, 10: 3*, 11: 4

*Not tested in production

Register	Address (hex)	Name	Default value (hex)
J	0x09	Audio interface configuration	0x25

Bit	Name	Default	Description
7	LOOPBACK	0	0: disable, 1: enable loopback => connect ADC output to DAC input
6	RX_FIRST_ SECOND	0	0: Receive audio data in the first 16-bit frame after the frame synchronization. 1: Receive audio data in the second 16-bit frame after the frame synchronization.
5	INV_BCLK	1	Inverse BCLK for Tx and Rx modes. 1: data valid on rising edge, 0: data valid on falling edge.
4	MASTER	0	1: enable audio interface in master mode: LFS protocol, SCK = 32 x Fs and FSYNC = Fs. 0: audio interface in slave mode.
3	SDO_HI_EN	0	0: SDO is continuously in output mode. 1: SDO is in output mode when transmitting data and is automatically. Switched into high-impedance state when no data is transmitted.
2	TX_FIRST	1	1: transmit the audio data in the first 16-bit frame after the frame synchronization. 0: do no transmit data in the first frame.
1	TX_SECOND	0	1: transmit the audio data in the second 16-bit frame after the frame synchronization. 0: do no transmit data in the second frame.
0	PROTOCOL	1	1: Short Frame Synchronization mode (inverse clock and slave mode). 0: Long Frame Synchronization mode (clock inverse or normal, mode master or slave).

Register	Address (hex)	Name	Default value (hex)
L	0x0B	Sandman function, off-time least significant byte	0x00

Bit	Name	Default	Description
7:0	SM_OFF_LSB	00000000	Least significant byte of the off-time of the Sandman function

Register	Address (hex)	Name	Default value (hex)
M	0x0C	Sandman function, off-time most significant byte	0x00

Bit	Name	Default	Description
7:0	SM_OFF_MSB	00000000	Most significant byte of the off-time of the Sandman function

Register	Address (hex)	Name	Default value (hex)
N	0x0D	Sandman function, on-time	0x00

Bit	Name	Default	Description
7:0	SM_ON	00000000	On-time of the Sandman function

Register	Address (hex)	Name	Default value (hex)
O	0x0E	Sandman function, reference for ADC	0x00

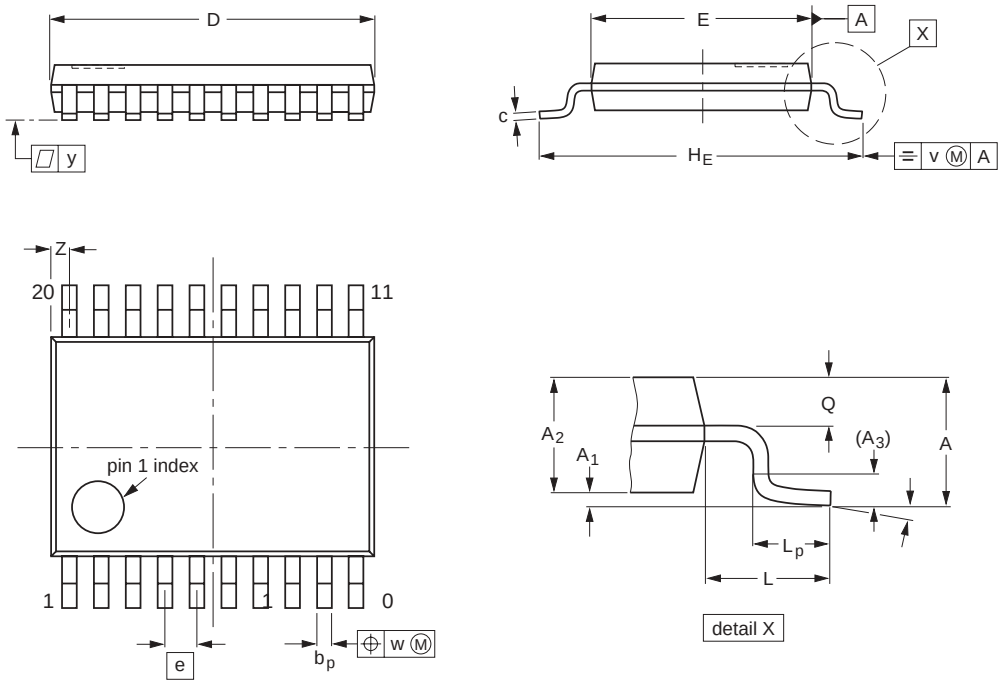
Bit	Name	Default	Description
7:0	SMAD_REF	00000000	Reference amplitude for ADC for Sandman function

Register	Address (hex)	Name	Default value (hex)
P	0x0F	Sandman function, reference for DAC	0x00

Bit	Name	Default	Description
7:0	SMDA _REF	00000000	Reference amplitude for DAC for Sandman function

9 Mechanical Information

9.1 XE3005 package size (TSSOP20)



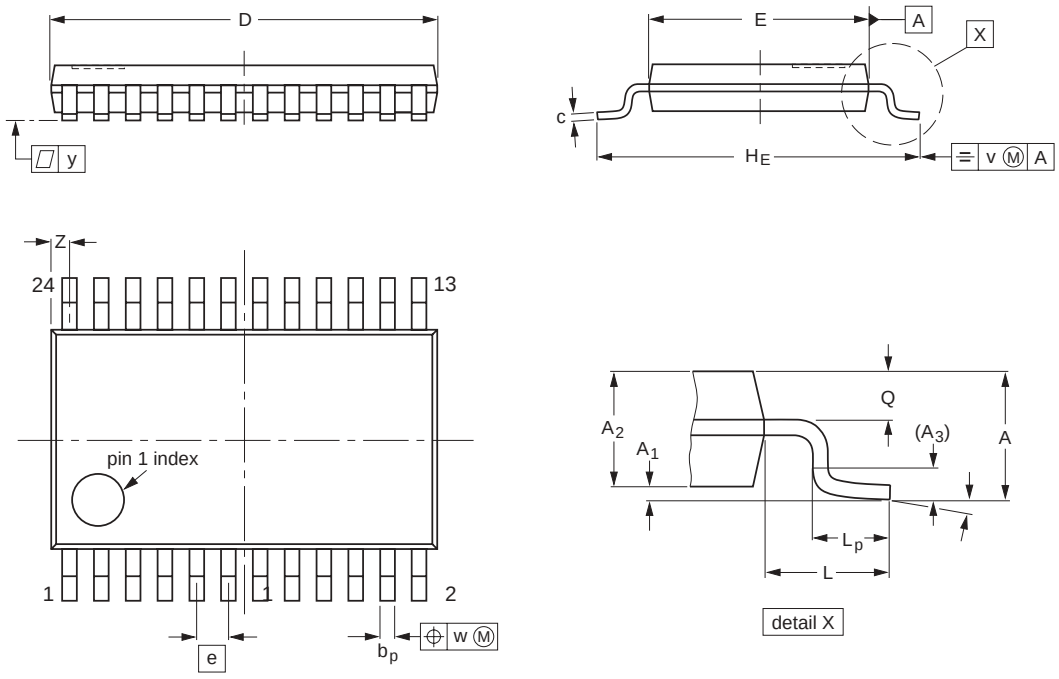
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D	E	e	H_E	L	L_p	Q	v	w	y	Z	
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Figure 21: TSSOP20

Plastic thin shrink small outline package; 20 leads; body width 4.4 mm

9.2 XE3006 Package size (TSSOP24)



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D	E	e	H_E	L	L_p	Q	v	w	y	Z	
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Figure 22: TSSOP24

Plastic thin shrink small outline package; 24 leads; body width 4.4 mm

Contact Information:
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