Beam-forming
Signal Processing IC for Ultra- Directional Microphone Effect

BU8332KV-M

Automotive Grade

●General Description

BU8332KV-M enables cardioid directivity through beam-forming technology using two omnidirectional microphones placed 10mm apart. Beam forming technology provides sharper directivity than unidirectional microphones. Features include selection of different polar patterns of response, adjustable sharpness of directivity via zoom function and switchable direction sensitivity. The processor enables hands-free calling and improves speech recognition in a variety of devices.

●Features

- Directional microphone function (Beam-forming)
- Microphone pitch: 10mm
- Selectable polar patterns of response
- Adjustable sharpness of directivity
- Switchable direction sensitivity
- Noise suppression
- Digital block powered by internal 1.5V regulator
- Built-in microphone bias and pre-amplifier
- Analog microphone inputs (Differential or Single ended） x 2ch
- Analog line input & line output
- PCM output
- Built-in ALC circuit
- 2-wire host interface（Slave address : 0x61）
- Stand-alone operation with external EEPROM

●Applications

- Hands-free operation / speech recognition in car navigation systems
- Portable devices such as mobile phones, smartphones, headset, or game machines
- Applications that require Voice Input

●Key Specifications

Operating power supply range :	3.0V to 3.6V
Operating temperature range :	-40℃ to +85℃
Operating current :	15mA(Typ.)
Deep standby current :	1µA(Typ.)
Polar pattern type :	“Cardioid”, “Bidirectional”, “Hyper-cardioid”

●Package

Package	W(Typ.) x D(Typ.) x H(Max.)
VQFP48	9.00mm x 9.00mm x 1.60mm

●Typical Application Circuit

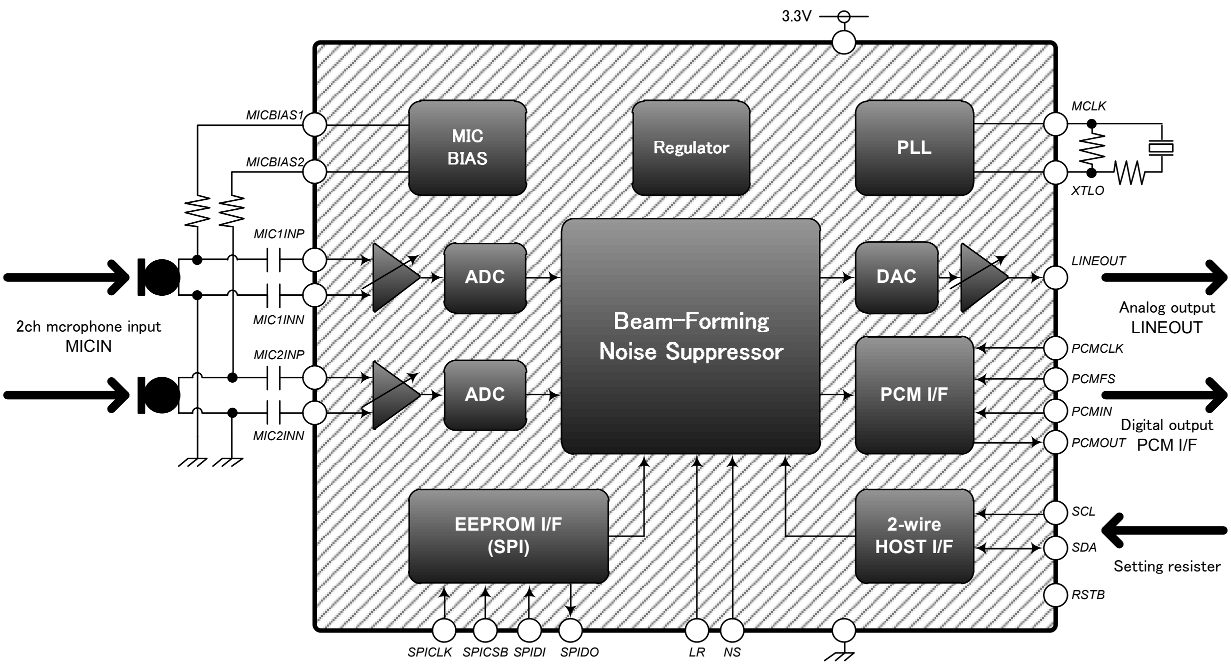


Figure 1 Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

●Pin Configuration

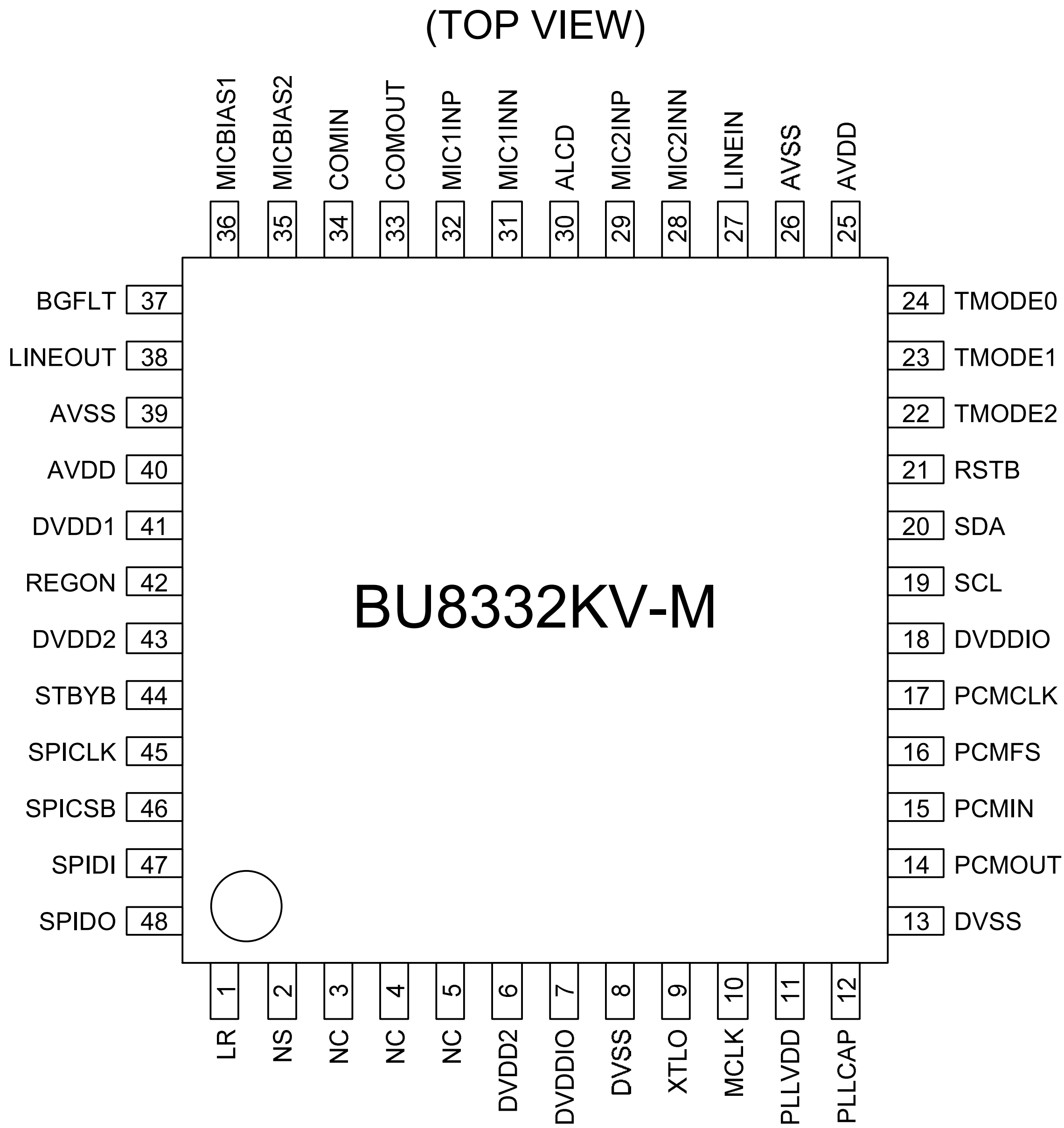


Figure 2 Pin Configuration

●Pin Description

Pin No.	Symbol	I/O	Function	Power supply system	I/O equal circuit
1	LR	I	To select directional axis (“L”: Left, ”Open”: Right)	DVDDIO	A
2	NS	I	To control noise suppression (“L”: NS=ON, ”Open”: NS=OFF)	DVDDIO	A
3	NC	-	NC	-	-
4	NC	-	NC	-	-
5	NC	-	NC	-	-
6	DVDD2	-	Digital power supply2 (Controlled by STBYB)	-	B
7	DVDDIO	-	I/O power supply	-	-
8	DVSS	-	Digital GND	-	-

Pin No.	Symbol	I/O	Function	Power supply system	I/O equal circuit
9	XTLO	O	Oscillator output	DVDDIO	C
10	MCLK	I	External clock input / Oscillator input	DVDDIO	C
11	PLLVDD	-	PLL power supply	-	-
12	PLLCAP	O	PLL filter pin (Recommended 56nF to DVSS)	PLLVDD	D
13	DVSS	-	Digital GND	-	-
14	PCMOUT	O	PCM signal output	DVDDIO	E
15	PCMIN	I	PCM signal input	DVDDIO	F
16	PCMFS	I	PCM frame signal input	DVDDIO	F
17	PCMCLK	I	PCM clock input	DVDDIO	F
18	DVDDIO	-	I/O power supply	-	-
19	SCL	I	Serial Clock input for 2-wire Host Interface	DVDDIO	G
20	SDA	I/O	Serial Data for 2-wire Host Interface (Data input or output)	DVDDIO	H
21	RSTB	I	Reset pin (“L” : Power down)	DVDDIO	G
22	TMODE2	I	Test pin (Connect to DVSS)	DVDDIO	F
23	TMODE1	I	Test pin (Connect to DVSS)	DVDDIO	F
24	TMODE0	I	Test pin (Connect to DVSS)	DVDDIO	F
25	AVDD	-	Analog power supply	-	-
26	AVSS	-	Analog GND	-	-
27	LINEIN	I	Line input (Reference signal)	AVDD	D
28	MIC2INN	I	Analog microphone input (2-)	AVDD	D
29	MIC2INP	I	Analog microphone input (2+)	AVDD	D
30	ALCD	O	ALC detection pin	AVDD	D
31	MIC1INN	I	Analog microphone input (1-)	AVDD	D
32	MIC1INP	I	Analog microphone input (1+)	AVDD	D
33	COMOUT	O	Analog reference voltage output (Recommended 1μF to AVSS)	AVDD	D
34	COMIN	I	Analog reference voltage (Recommended 1μF to AVSS)	AVDD	D
35	MICBIAS2	O	Microphone bias output2	AVDD	D
36	MICBIAS1	O	Microphone bias output1	AVDD	D
37	BGFLT	O	Bias filter pin (Recommended 0.1μF to AVSS)	AVDD	D
38	LINEOUT	O	Line output	AVDD	D
39	AVSS	-	Analog GND	-	-
40	AVDD	-	Analog power supply	-	-
41	DVDD1	-	Digital power supply1 (Direct input)	-	-
42	REGON	I	To control 1.5V regulator (“L”:OFF, “H”:ON)	DVDDIO	I
43	DVDD2	-	Digital power supply2 (Controlled by STBYB)	-	B
44	STBYB	I	To control standby (“L” : Power down, ”H” : Normal)	DVDDIO	I
45	SPICLK	O	SPI clock output	DVDDIO	E
46	SPICSB	O	SPI chip select output	DVDDIO	E
47	SPIDI	I	SPI data input	DVDDIO	F
48	SPIDO	O	SPI data output	DVDDIO	E

“H” level is voltage value of DVDDIO, ”L” level is voltage value of DVSS.

● Block Diagram

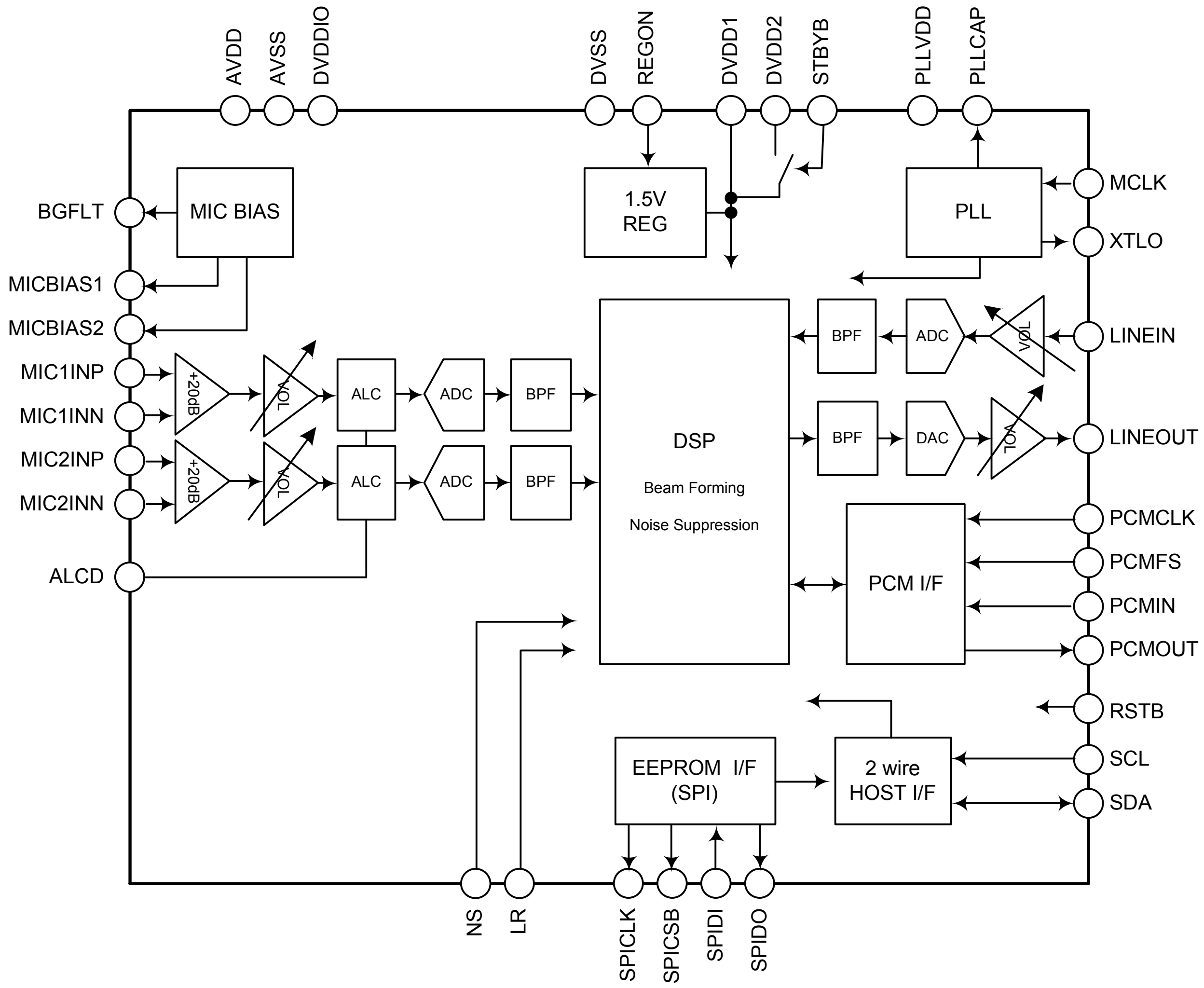


Figure 3 Block Diagram

●Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit.
Analog power supply	AVDD	-0.3 to 4.5	V
PLL power supply	PLLVDD	-0.3 to 4.5	V
I/O power supply	DVDDIO	-0.3 to 4.5	V
Digital power supply	DVDD1 DVDD2	-0.3 to 2.16	V
Analog input voltage	VTA	AVSS-0.3 to AVDD+0.3	V
Digital input voltage	VTD	DVSS-0.3 to DVDDIO+0.3	V
Input current	IIN	-10 to +10	mA
Storage temperature range	TS	-50 to 125	℃

●Recommended Operating Ratings

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Analog power supply	AVDD	3.0	3.3	3.6	V
PLL power supply	PLLVDD	3.0	3.3	3.6	V
I/O power supply	DVDDIO	DVDD1 DVDD2	3.3	3.6	V
Digital power supply	DVDD1	1.4	1.5	1.6	V
	DVDD2	1.45	1.5	1.6	V
Clock input frequency	FMCLK	4	-	8	MHz
Duty	DMCLK	40	50	60	%
Operating temperature range	Ta	-40	25	85	℃

●Electrical Characteristics

◆DC Characteristics

Application Circuit (Figure 42), Ta=25℃, AVDD=3.3V, PLLVDD=3.3V, REGON="H" unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Current *1	IST	-	10	90	μA	Standby (Setting register)
	IDST	-	1	5	μA	Deep standby (STBYB="L")
	IDD	-	15	30	mA	FS=16kHz,BF=ON,NS=ON
Digital Hi level input voltage	VIH	0.7* DVDDIO	-	-	V	-
Digital Low level input voltage	VIL	-	-	0.3* DVDDIO	V	-
Digital Hi level input current	IIH	-	-	1.0	μA	VIH=DVDDIO (Pull-down resistance input pins are excluded)
Digital Low level input current	IIL	-1.0	-	-	μA	VIL=DVSS
Digital Hi level output voltage	VOH	0.8* DVDDIO	-	-	V	IOH=-1mA
Digital Low level output voltage	VOL	0	-	0.2* DVDDIO	V	IOL=1mA
Digital Low level output voltage	VOL	0	-	0.2* DVDDIO	V	IOL=3mA (SDA)
Regulator output voltage	VREG	-	1.5	-	V	

*1 Digital and analog output pin is no-load.

◆CODEC Characteristics

Application Circuit (Figure 42), Ta=25℃, AVDD=3.3V, PLLVDD=3.3V, REGON=”H”, BF=OFF, NS=OFF
FS=16 kHz, MIC1VOL/MIC2VOL/LINVOL/LOUTVOL=0dB unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Transmit signal-to-distortion ratio + Noise MICIN(LINEIN) → PCMOUT	SDT	45	-	-	dB	Input signal：0dBm0, 1020Hz Using filter：20kHz LPF
Receive signal-to-distortion ratio + Noise PCMOUT → LINEOUT	SDR	45	-	-	dB	Input signal：0dBm0, 1020Hz Using filter：20kHz LPF
Transmit gain tracking (-10dBm0 reference) MICIN(LINEIN) → PCMOUT	GTX	-3.0	-	3.0	dB	Input signal：+3.0 to +0.5dBm0, 1020Hz Using filter：1020Hz BPF
		-1.0	-	1.0		Input signal：+0.5 to -40dBm0, 1020Hz Using filter：1020Hz BPF
		-2.0	-	2.0		Input signal：-40 to -55dBm0, 1020Hz Using filter：1020Hz BPF
Receive gain tracking (-10dBm0 reference) PCMIN → LINEOUT	GRX	-1.0	-	1.0	dB	Input signal：+3.0 to -40dBm0, 1020Hz Using filter：1020Hz BPF
		-2.0	-	2.0		Input signal：-40 to -55dBm0, 1020Hz Using filter：1020Hz BPF
Transmit reference level	VITX	0.037	0.050	0.068	Vrms	Input signal：0dBm0, 1020Hz Using filter：1020Hz BPF 20dB amplification in inside
Receive reference level	VORX	0.400	0.500	0.625	Vrms	Input signal：0dBm0, 1020Hz Using filter：1020Hz BPF
Transmit gain loss relative to frequency (1020Hz reference) MICIN(LINEIN) → PCMOUT	GRTX	24	-	-	dB	Input signal：0dBm0, 0.06kHz Using filter：BPF
		0	-	2.5		Input signal：0dBm0, 0.2kHz Using filter：BPF
		-1.0	-	1.0		Input signal：0dBm0, 0.3 to 6.8kHz Using filter：BPF
		0	-	-		Input signal：0dBm0, 7.2kHz Using filter：BPF
		6.5	-	-		Input signal：0dBm0, 7.56kHz Using filter：BPF
Receive gain loss relative to frequency (1020Hz reference) PCMIN → LINEOUT	GRRX	24	-	-	dB	Input signal：0dBm0, 0.06kHz Using filter：BPF
		0	-	2.5		Input signal：0dBm0, 0.2kHz Using filter：BPF
		-1.0	-	1.0		Input signal：0dBm0, 0.3 to 6.8kHz Using filter：BPF
		0	-	-		Input signal：0dBm0, 7.2kHz Using filter：BPF
		6.5	-	-		Input signal：0dBm0, 7.56kHz Using filter：BPF
Transmit noise level	VNTX	-	-	-73	dBFS	COMOUT input in MICIN Using filter：A-Weight
Receive noise level	VNRX	-	-	-85	dBV	PCMIN=“L” fixation Using filter：A-Weight

◆Transmit / Receive analog block

Application Circuit (Figure 42), Ta=25℃, AVDD=3.3V, PLLVDD=3.3V, REGON=”H”, f=1kHz unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Minimum load resistance	RALRT	600	-	-	Ω	Measurement Pin：LINEOUT
Maximum load capacitance	CALRX	-	-	50	pF	Measurement Pin：LINEOUT
Maximum output level	VAORX	1.9	-	-	Vpp	Measurement Pin：LINEOUT
Volume gain setting range MIC1/MIC2/LINEIN	GTVOL	-20	-	30	dB	Measurement Path：MICIN → PCMOUT
Volume step width MIC1/MIC2/LINEIN	GTSTEP	-	2	-	dB	Measurement Path：MICIN → PCMOUT
Volume gain setting range LINEOUT	GRVOL	-25	-	16	dB	Measurement Path：MICIN → LINEOUT
Volume step width LINEOUT	GRSTEP	-	1	-	dB	Measurement Path：MICIN → LINEOUT

◆Reference

Application Circuit (Figure 42), Ta=25℃, AVDD=3.3V, PLLVDD=3.3V, REGON=”H” unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Output voltage	VAG	0.45* AVDD	0.5* AVDD	0.55* AVDD	V	Measurement Pin：COMIN, COMOUT
Rise time *2	TAG	-	-	15	ms	RSTB=“L”→”H” 90%attainment time COMIN=1μF, COMOUT=1μF

*2 Rise time is affected to power supply, COMIN capacitance, and process. Please, have sufficient margin when value determination.

◆Microphone BIAS (MICBIAS)

Application Circuit (Figure 42), Ta=25℃, AVDD=3.3V, PLLVDD=3.3V, REGON=”H”, f=1kHz unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
MICBIAS output voltage	VMICB	2.2	2.5	2.8	V	Measurement Pin：MICBIAS1, MICBIAS2 Iload=1mA
MICBIAS output noise	VNOMICB	-	-95	-80	dBV	Measurement Pin：MICBIAS1, MICBIAS2 RL=2kΩ Using filter：A-Weight
PSRR	PSRMICB	40	-	-	dB	Measurement Pin：MICBIAS1, MICBIAS2 Using filter：1kHz BPF GMIC=0dB, Vrippl=100mVpp

◆ALC

Application Circuit (Figure 42), Ta=25℃, AVDD=3.3V, PLLVDD=3.3V, REGON=“H”, BF=OFF, NS=OFF, 2.2μF and 390Ω connect to ALCD Pin, Signal frequency=1kHz, 20kH LPF unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
ALC signal level	VALC	-8.5	-6	-3.5	dBV	Input signal：-26dBV
Maximum gain	GALC	18	20	23	dB	Input signal：-35dBV
Attack time	TATK	-	3	-	msec	Input signal：-30dBV → -10dBV
Signal-to-distortion ratio + Noise	THDALC	-	-40	-30	dB	Input signal：-26dBV
Noise level	NALC	-	-70	-50	dBV	Input signal：No signal Using filter：A-Weight

●Typical Performance Curve(s)

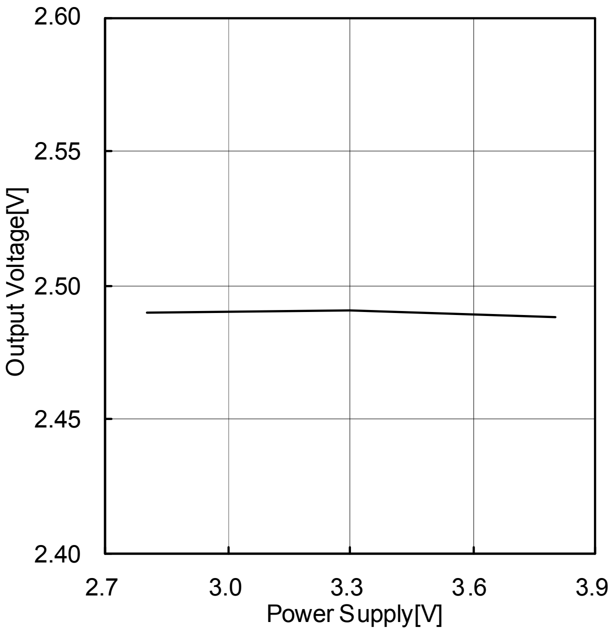


Figure 4 MICBIAS1 output voltage

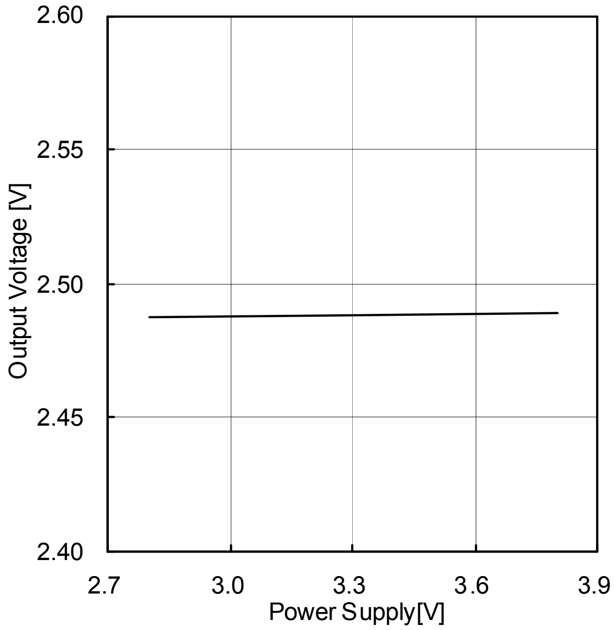


Figure 5 MICBIAS2 output voltage

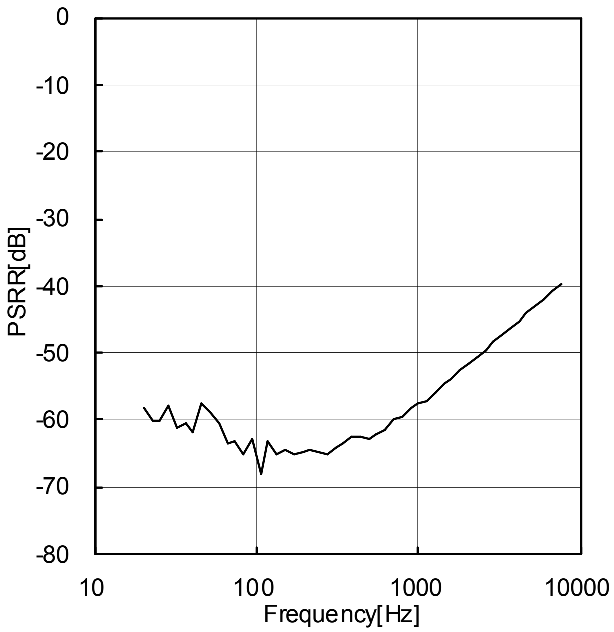


Figure 6 MICBIAS1PSRR

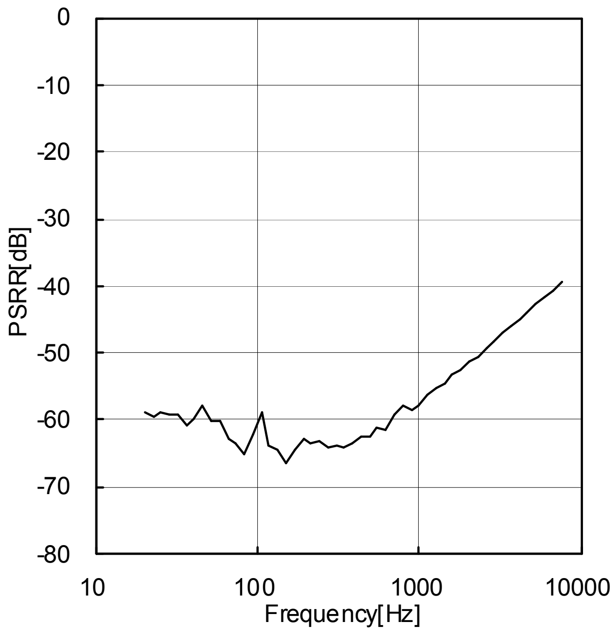


Figure 7 MICBIAS2PSRR

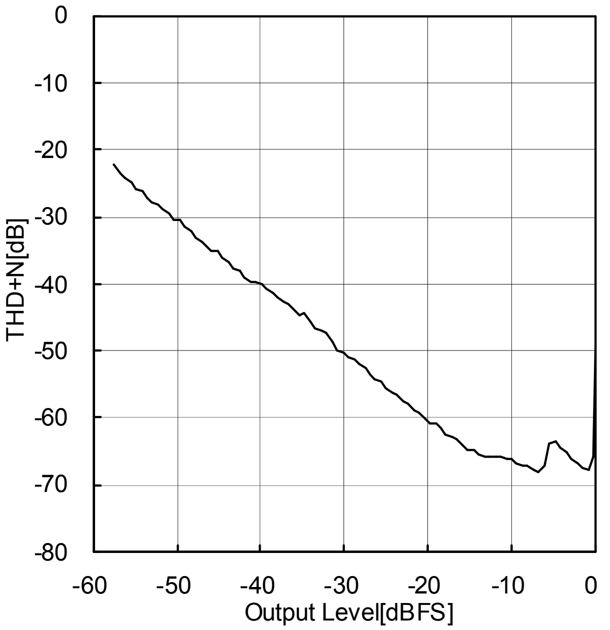


Figure 8 MIC1 signal-to-distortion ratio + Noise

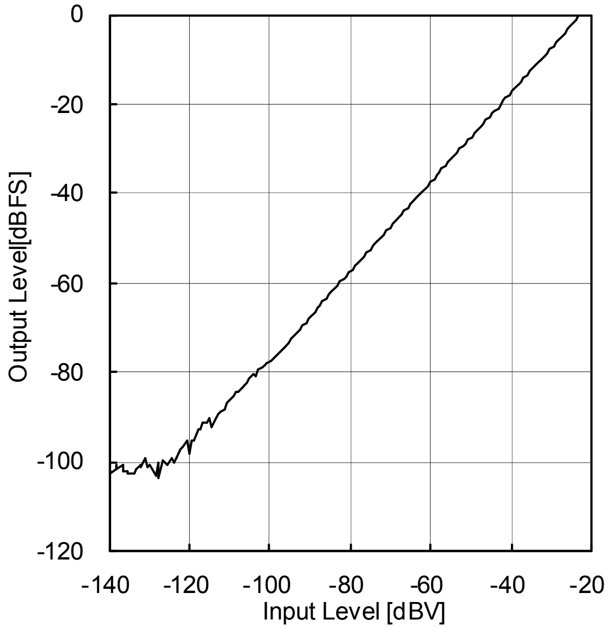


Figure 9 MIC1 signal level

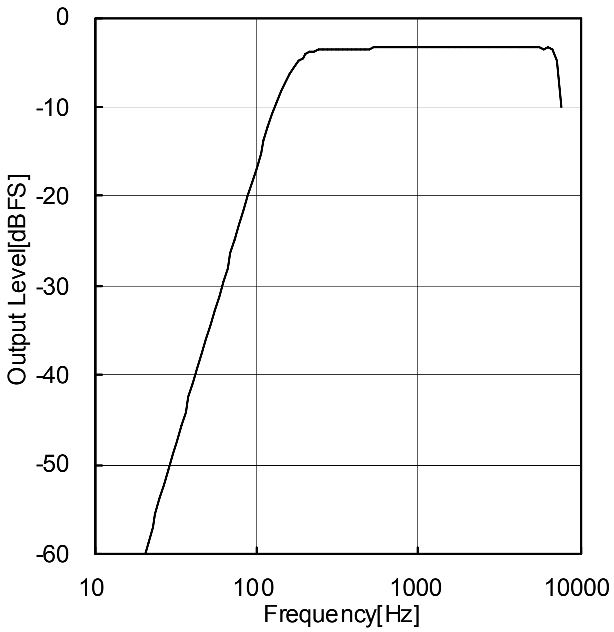


Figure 10 MIC1 gain loss relative to frequency

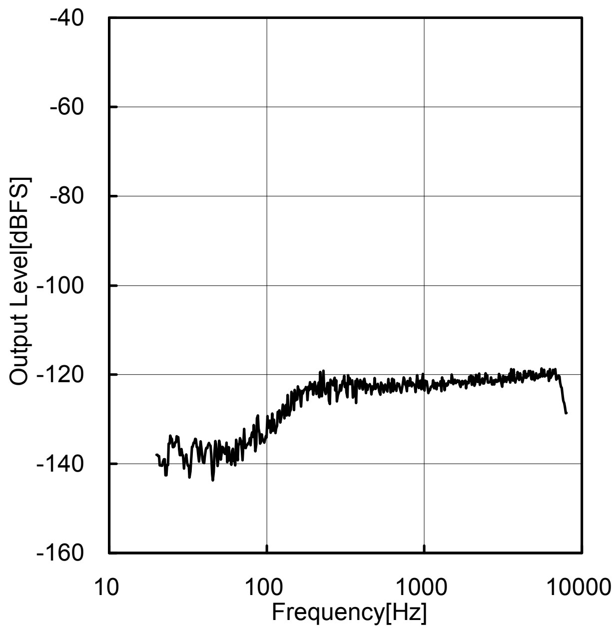


Figure 11 MIC1 noise level

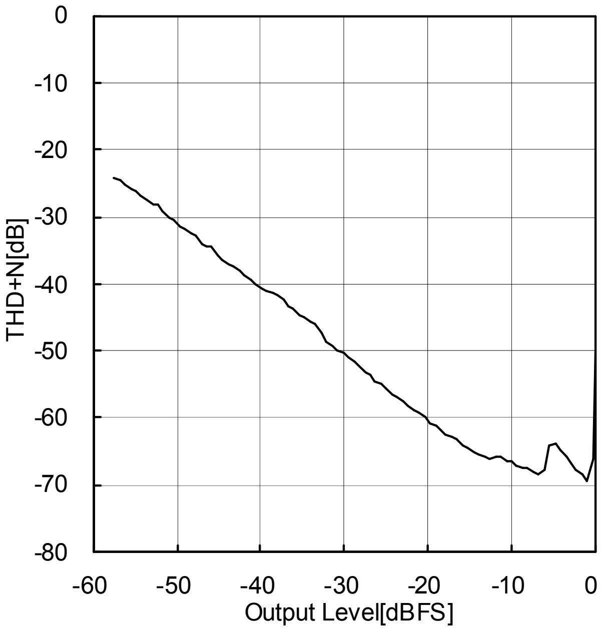


Figure 12 MIC2 signal-to-distortion ratio + Noise

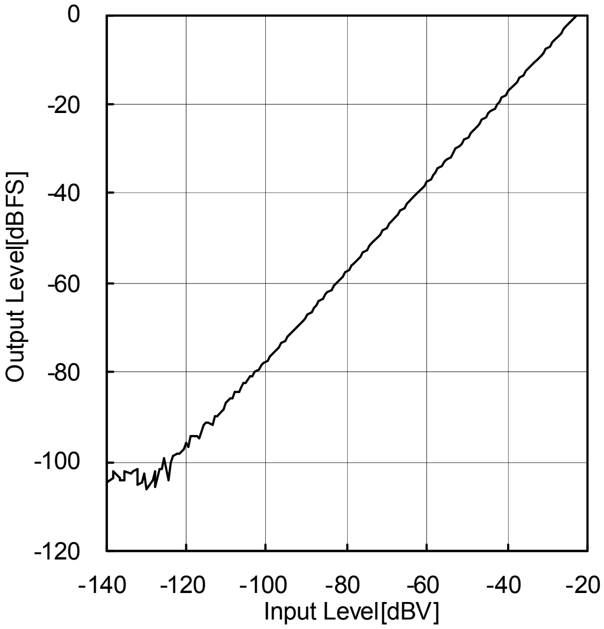


Figure 13 MIC2 signal level

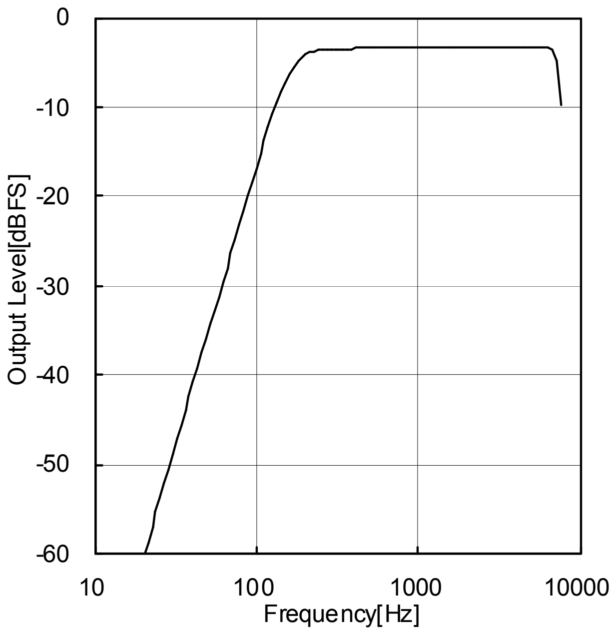


Figure 14 MIC2 gain loss relative to frequency

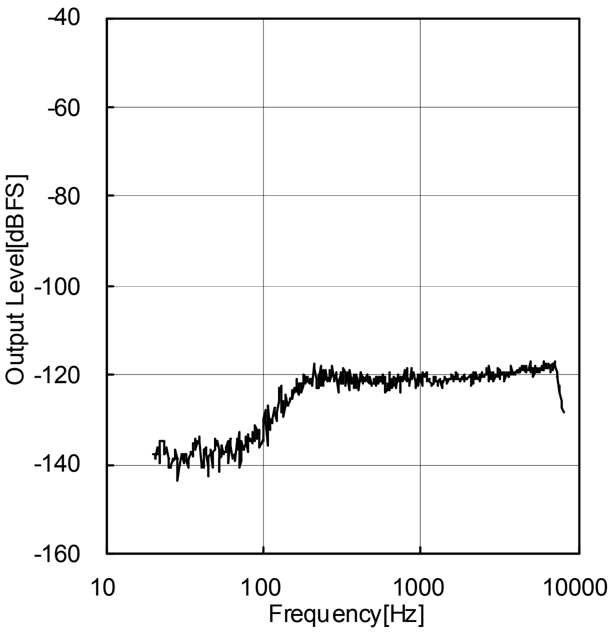


Figure 15 MIC2 noise level

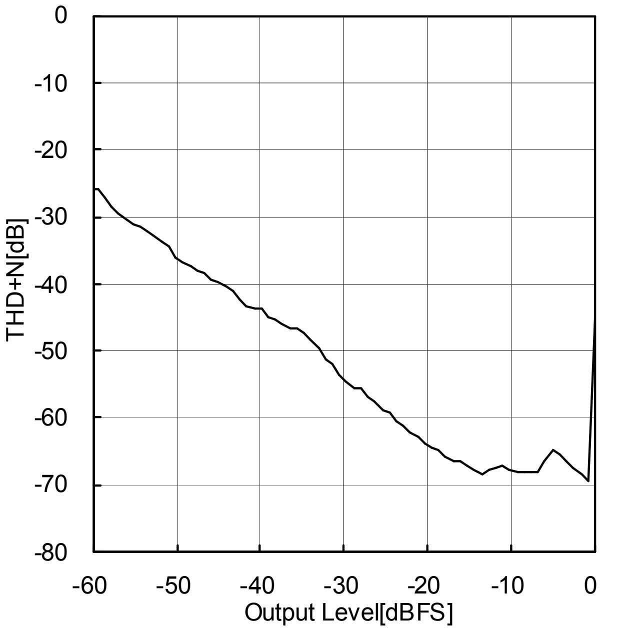


Figure 16 LINEIN signal-to-distortion ratio + Noise

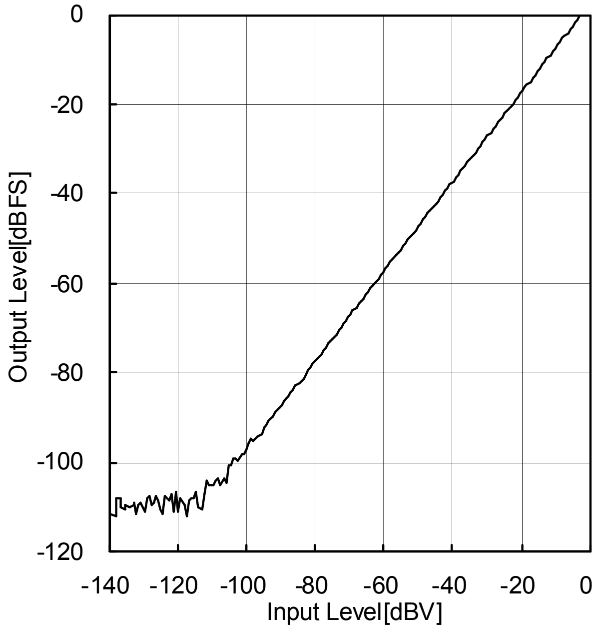


Figure 17 LINEIN signal level

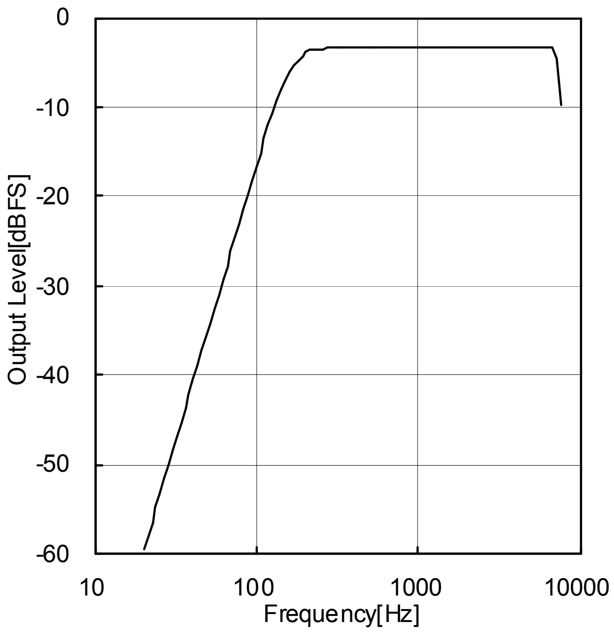


Figure 18 LINEIN gain loss relative to frequency

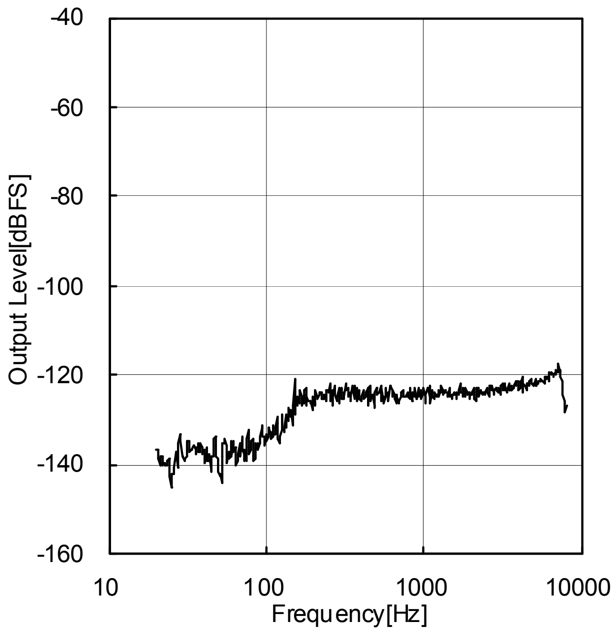


Figure 19 LINEIN noise level

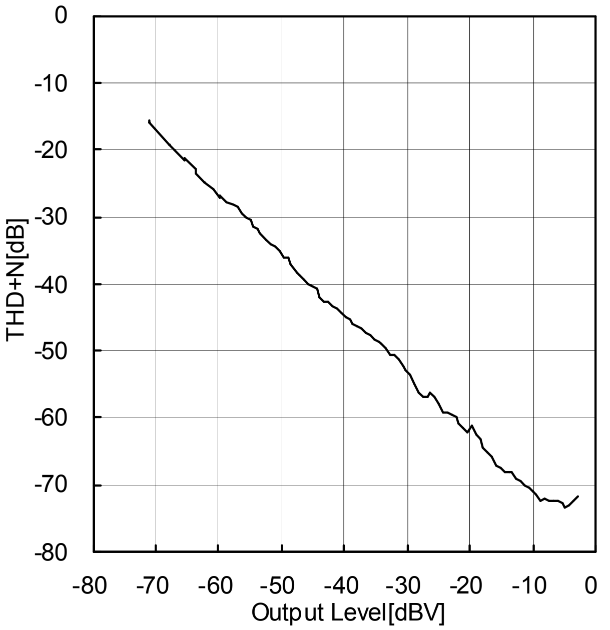


Figure 20 LINEOUT signal-to-distortion ratio + Noise

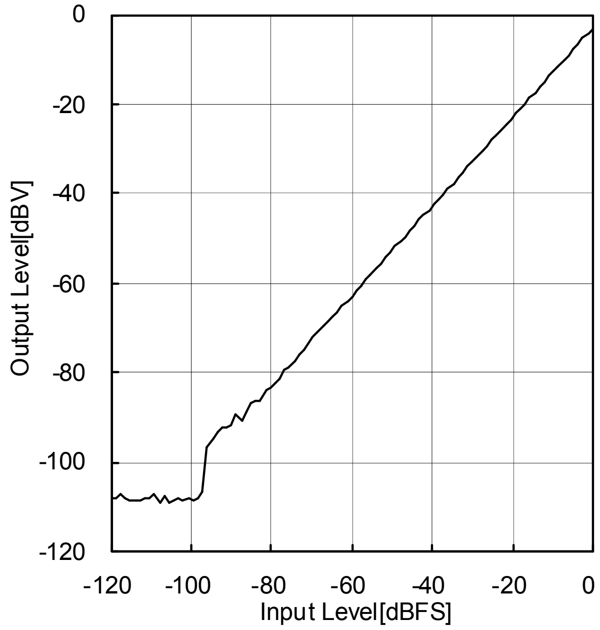


Figure 21 LINEOUT signal level

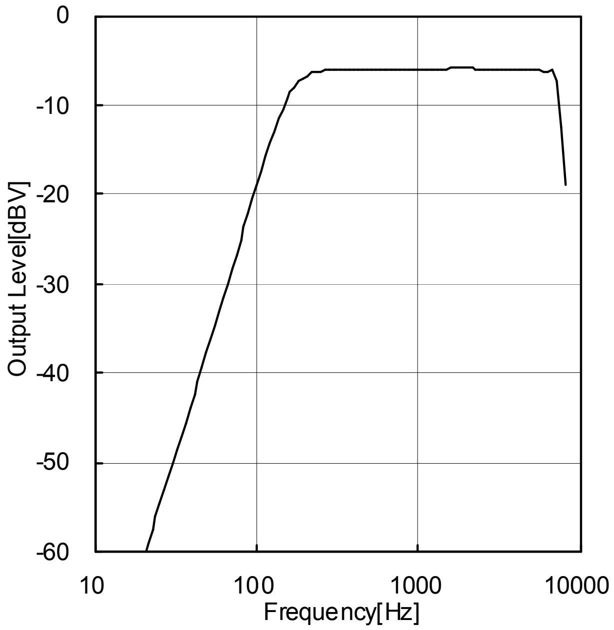


Figure 22 LINEOUT gain loss relative to frequency

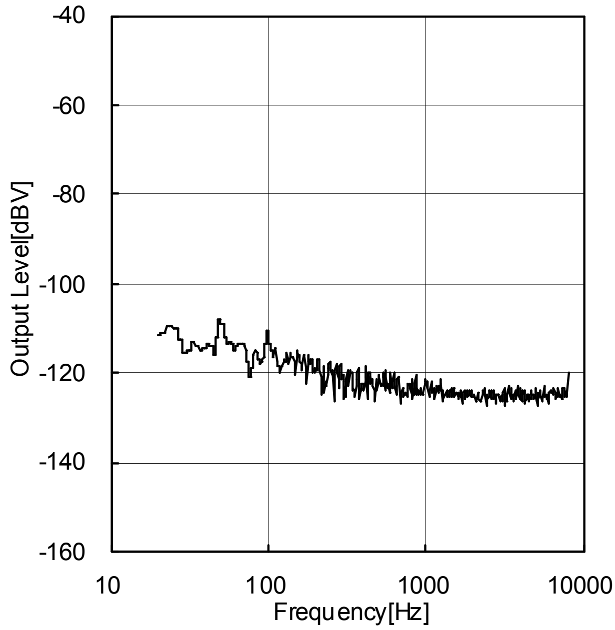


Figure 23 LINEOUT noise level

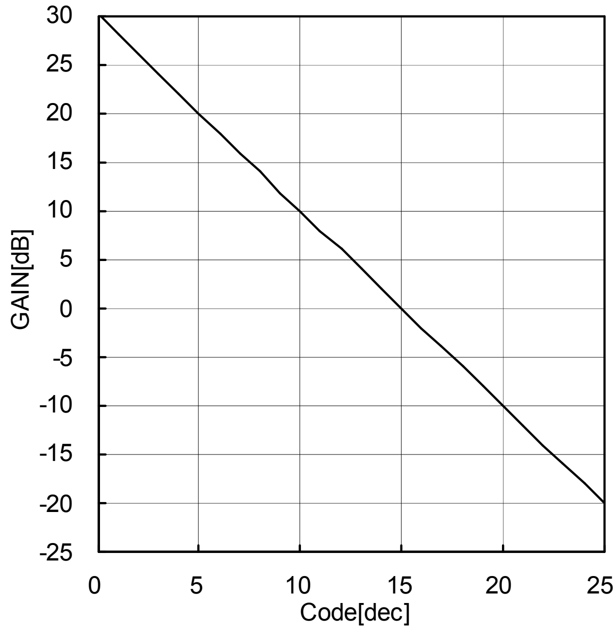


Figure 24 MIC1 Volume

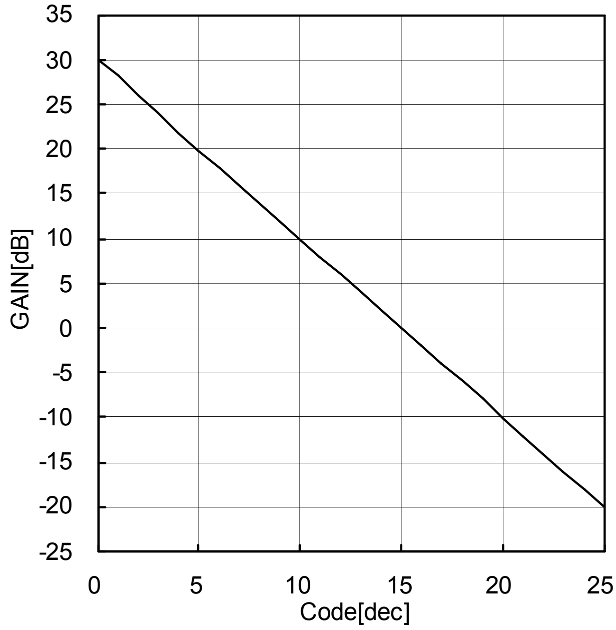


Figure 25 MIC2 Volume

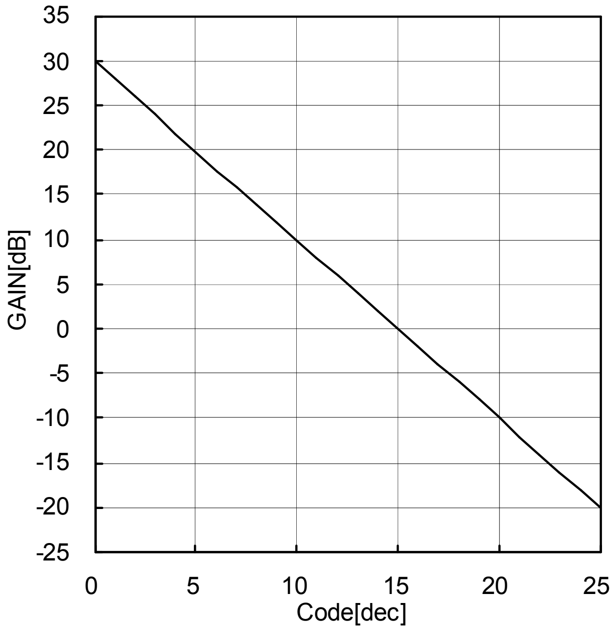


Figure 26 LINEIN Volume

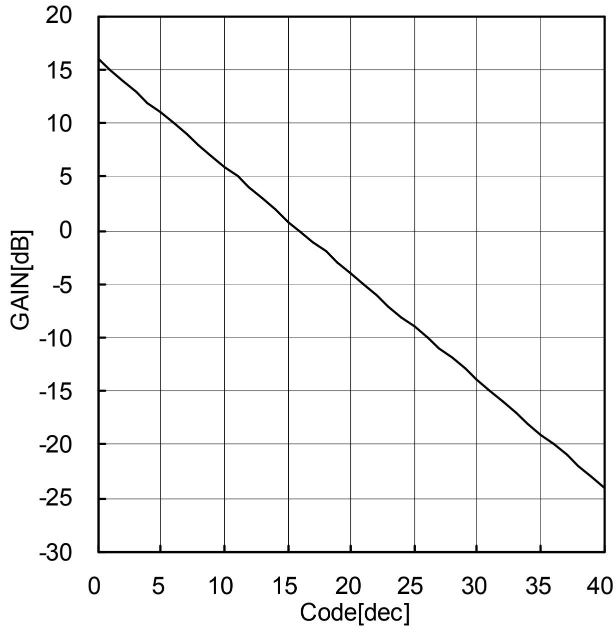


Figure 27 LINEOUT Volume

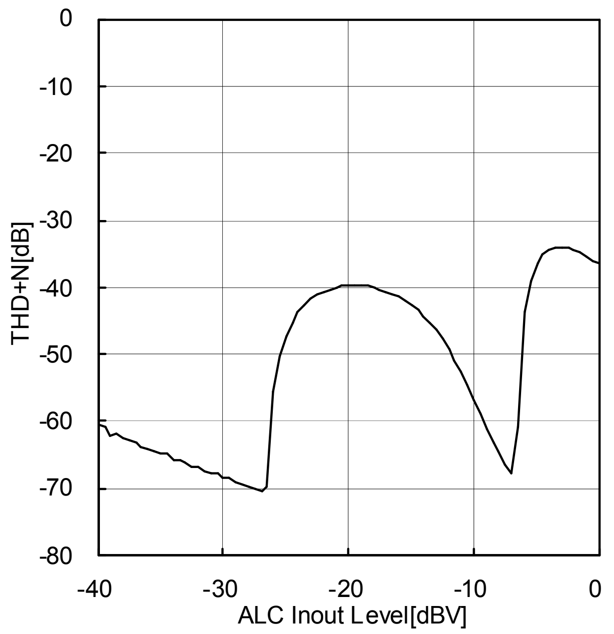


Figure 28 ALC Signal-to-distortion ratio+ Noise

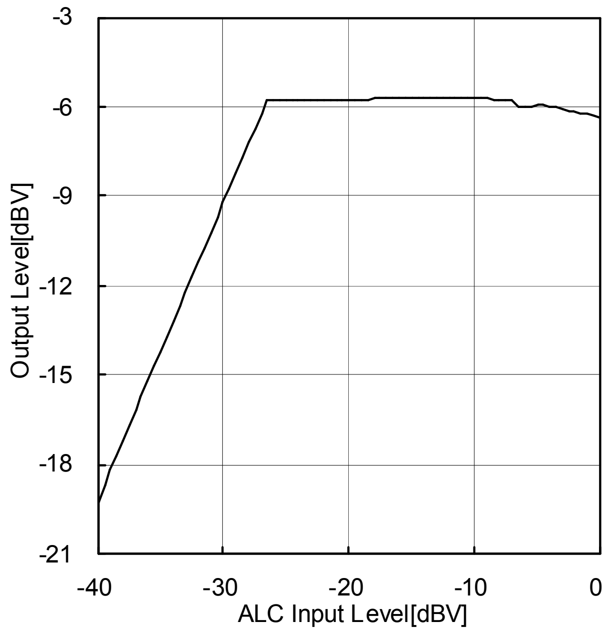


Figure 29 ALC signal level

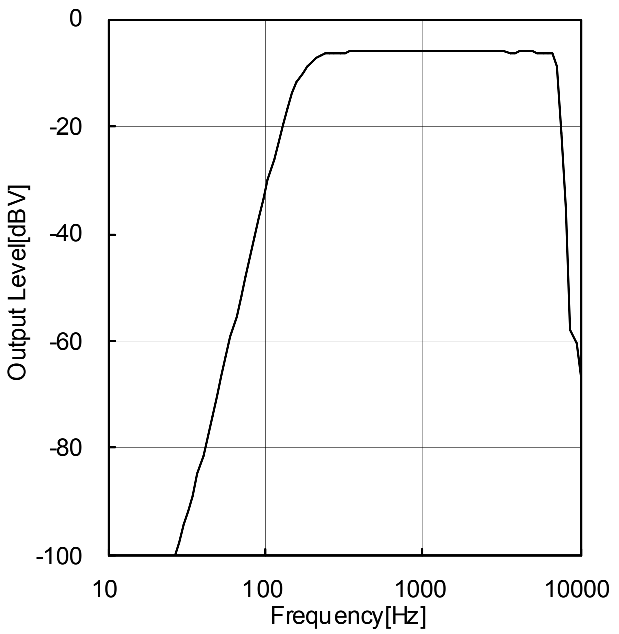


Figure 30 ALC gain loss relative to frequency

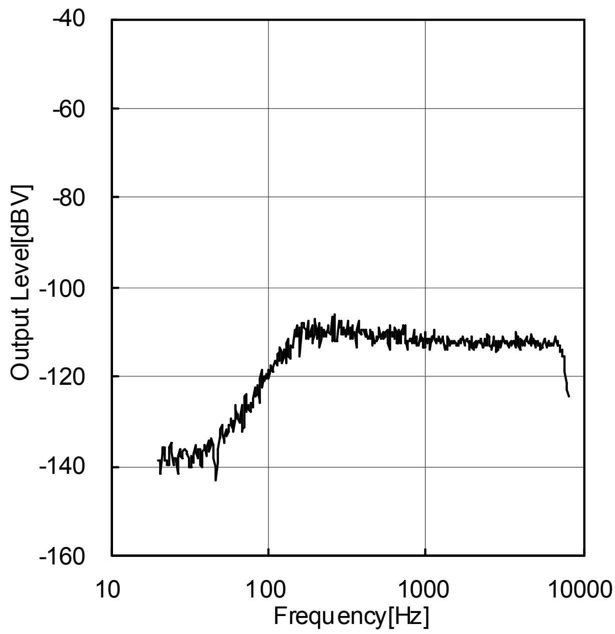


Figure 31 ALC noise level

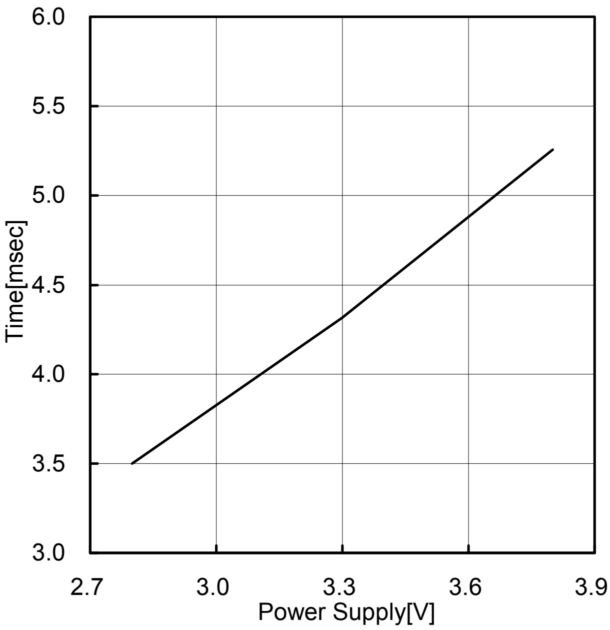


Figure 32 PLL pull-in time

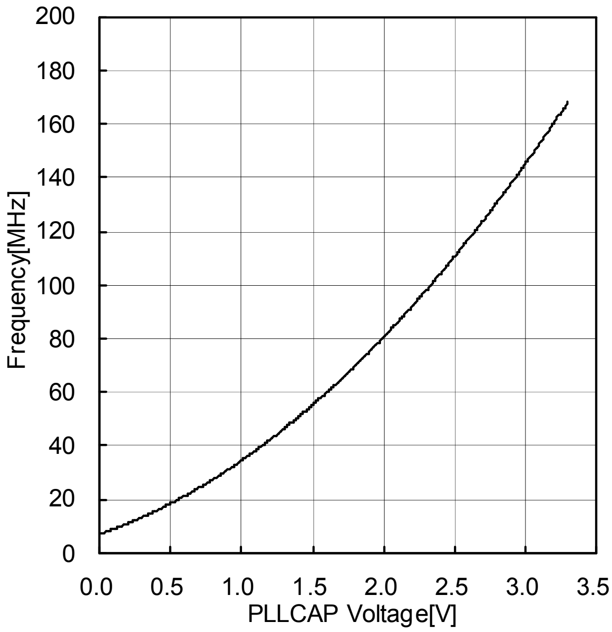


Figure 33 V-F characteristic

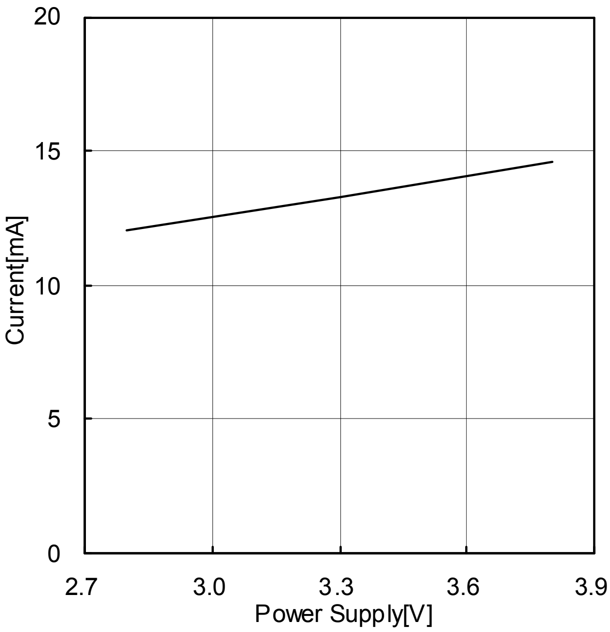


Figure 34 Operating Current

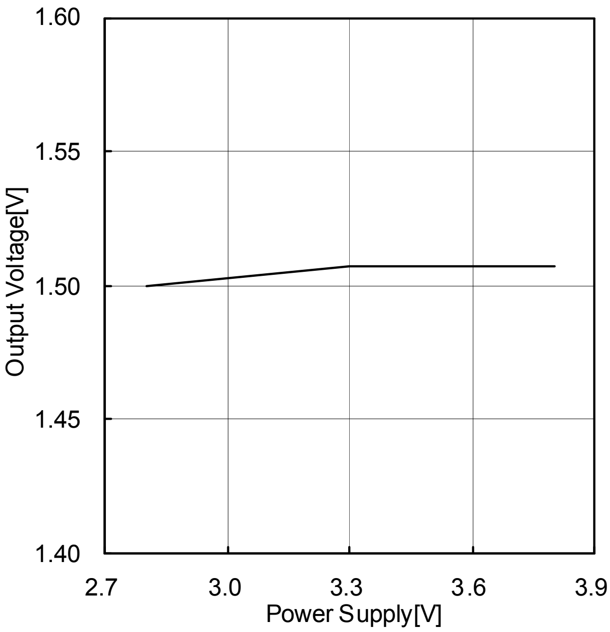


Figure 35 Regulator output voltage

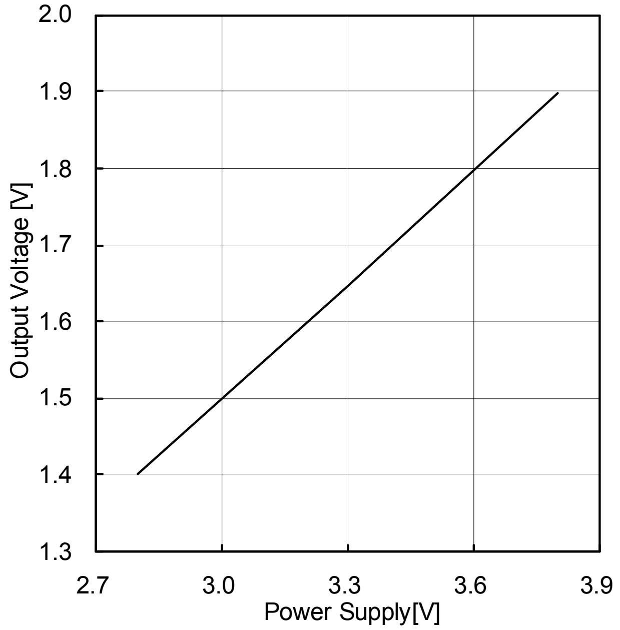


Figure 36 COMOUT output voltage

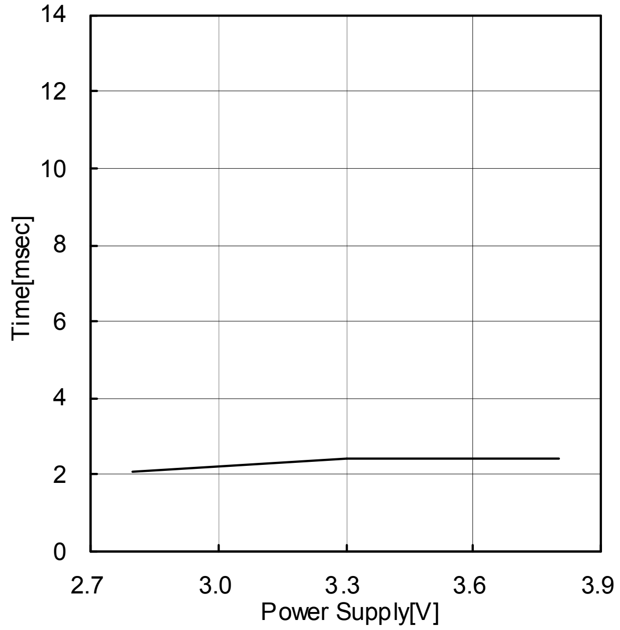


Figure 37 COMOUT rise time

● Digital interface characteristic

1. PCM interface

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Min.	
Clock frequency (PCMCLK)	f_{PCLK}	PCMFS=16kHz	256		2048	kHz
Clock duty	f_{DU}	-	40	-	60	%
Frame synchronization signal frequency(PMCFS)	f_{FS}	-	15.992	16	16.008	kHz
Digital input rise time	t_{IR}	DVDDIO*0.3→DVDDIO*0.7 PCKCLK, PCMFS, PCMIN	-	-	40	ns
Digital input fall time	t_{IF}	DVDDIO*0.7→DVDDIO*0.3 PCMCLK, PCMFS, PCMIN	-	-	40	ns
Transmit / Receive synchronization signal timing	t_{RS}	PCMIN setup time （vs. PCMCLK↓）	20	-	-	ns
	t_{RH}	PCMIN hold time （vs. PCMCLK↓）	0	-	-	ns
	t_{SR}	PCMCLK↓ vs. PCMFS↑	20	-	-	ns
	t_{SS}	PCMFS setup time （vs. PCMCLK↓）	20	-	-	ns
	t_{SH}	PCMFS hold time （vs. PCMCLK↓）	20	-	-	ns
	t_{SO}	PCMOUT determined time （vs. PCMFS↑）	-	-	30	ns
	t_{DO}	PCMOUT determined time （vs. PCMCLK↑）	-	-	30	ns

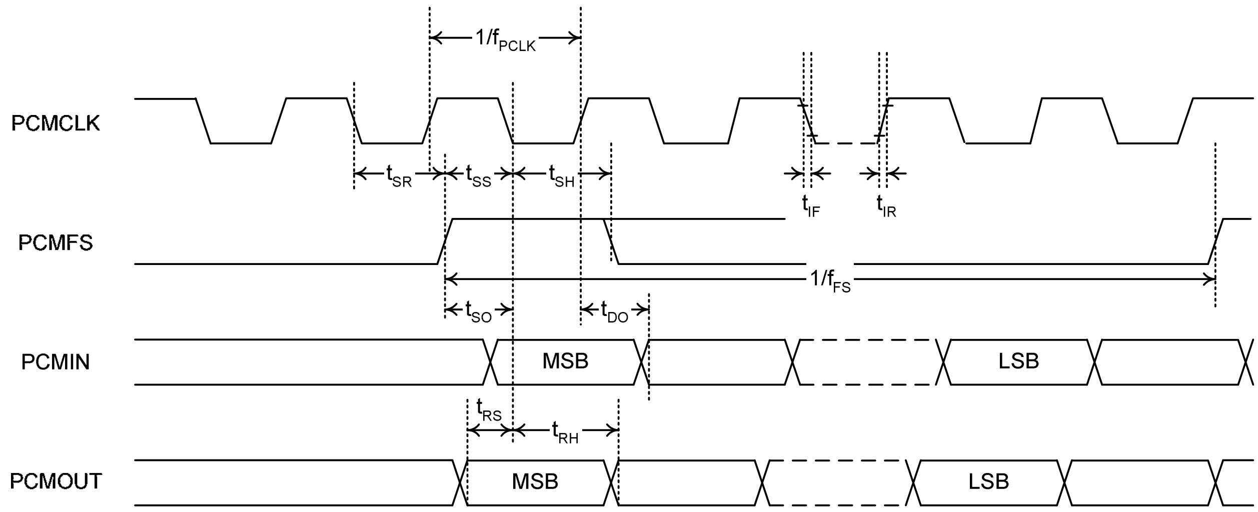


Figure 38 Timing of PCM long frame interface

2. 2-wire host interface (Slave)

Parameter	Symbol	Standard-mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
"H" level of SCL	t_{HI}	4.0	-	0.6	-	μs
"L" level of SCL	t_{LO}	4.7	-	1.2	-	μs
Setup time of repeat start condition	t_{SUSTA}	4.7	-	0.6	-	μs
Hold time of repeat start condition	t_{HDSTA}	4.0	-	0.6	-	μs
Data setup time	t_{SUDAT}	0.25	-	0.1	-	μs
Data hold time	t_{HDDAT}	0	3.5	0	0.9	μs
Setup time of Stop condition	t_{SUSTP}	4.0	-	0.6	-	μs
Bus release time of between stop condition and start condition	t_{BUF}	4.7	-	1.2	-	μs

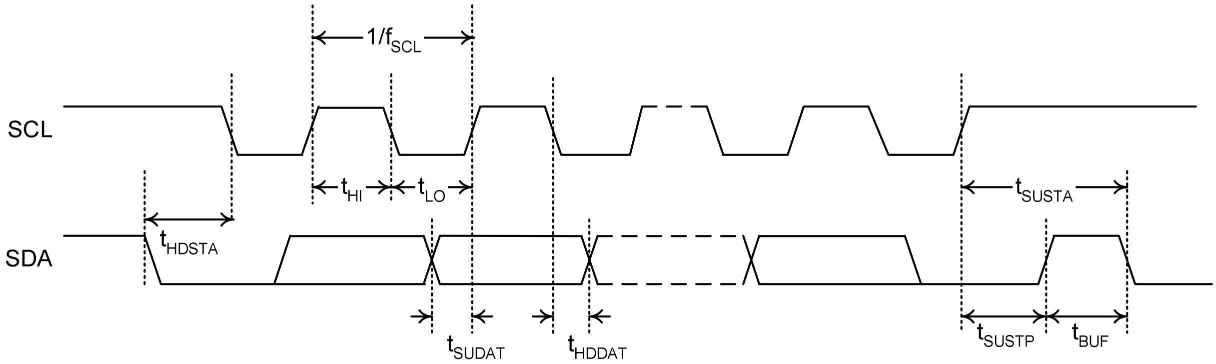


Figure 39 Timing of 2-wire host interface

3. EEPROM (SPI master) interface

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SPICLK clock frequency	f_{CK}	-	-	3.25	MHz
"H" time of SPICLK clock	t_{CK_HI}	100	-	-	ns
"L" time of SPICLK clock	t_{CK_LO}	100	-	-	ns
"H" time of SPICSB chip select	t_{CS_HI}	100	-	-	ns
Setup time of SPICSB chip select	t_{CS_SU}	100	-	-	ns
Enable hold time of SPICSB chip select	t_{CS_HD}	100	-	-	ns
Data output delay time of SPIDO	t_{DO_SU}	-	-	80	ns
Output hold time of SPIDO	t_{DO_HD}	0	-	-	ns
Setup time of SPIDI	t_{DI_SU}	20	-	-	ns
Hold time of SPIDI	t_{DI_SO}	40	-	-	ns

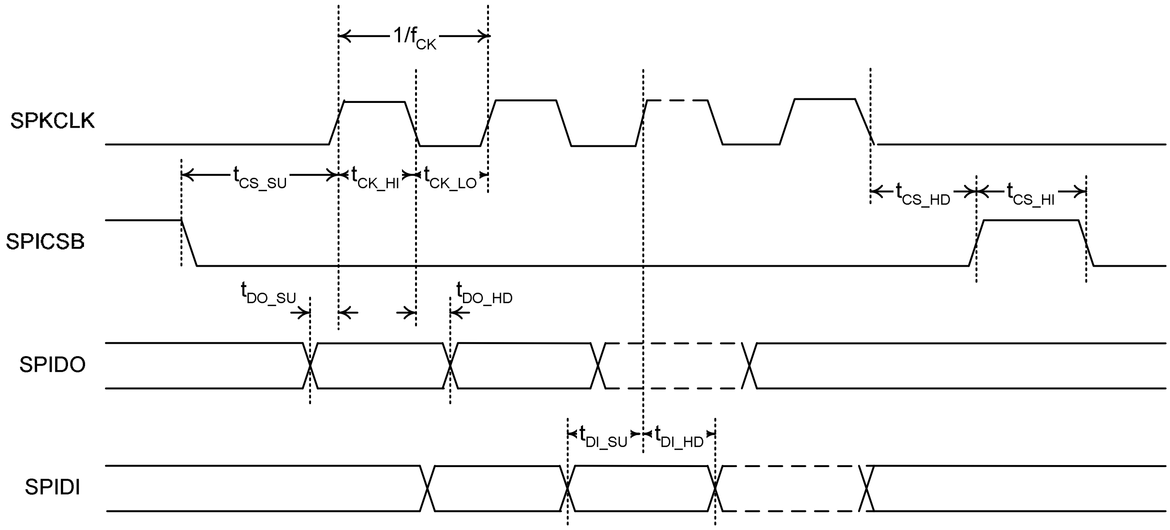


Figure 40 Timing of EEPROM (SPI) interface

●Timing Chart

Turn on AVDD and DVDDIO simultaneously and then turn on DVDD1 or DVDD2. Please note that DVDD1 can be supplied by internal voltage regulator. Please set REGON pin =”H” to use internal regulator.
It is necessary to input clock on MCLK, before reset (RSTB) is released.
Initial values of register are automatically downloaded from EEPROM and register is updated, after reset (RSTB) release. This processing is skipped when EEPROM is not connected.
Then, using via 2-wire host interface, please carry out required register setup.

2-wire host interface is compatible with I^2C bus specification, but is not 5V tolerant.

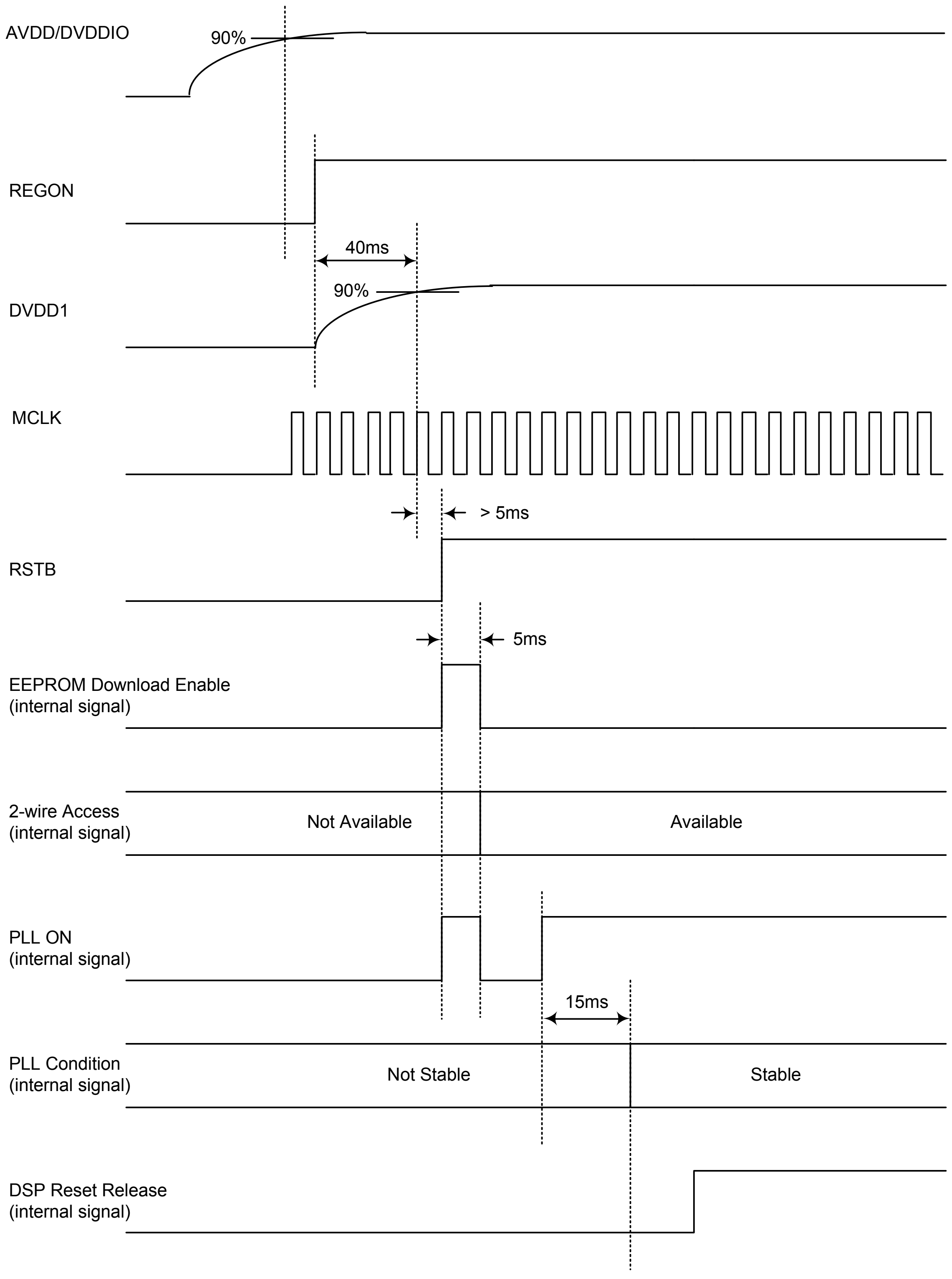


Figure 41 Timing Chart

●Application Example

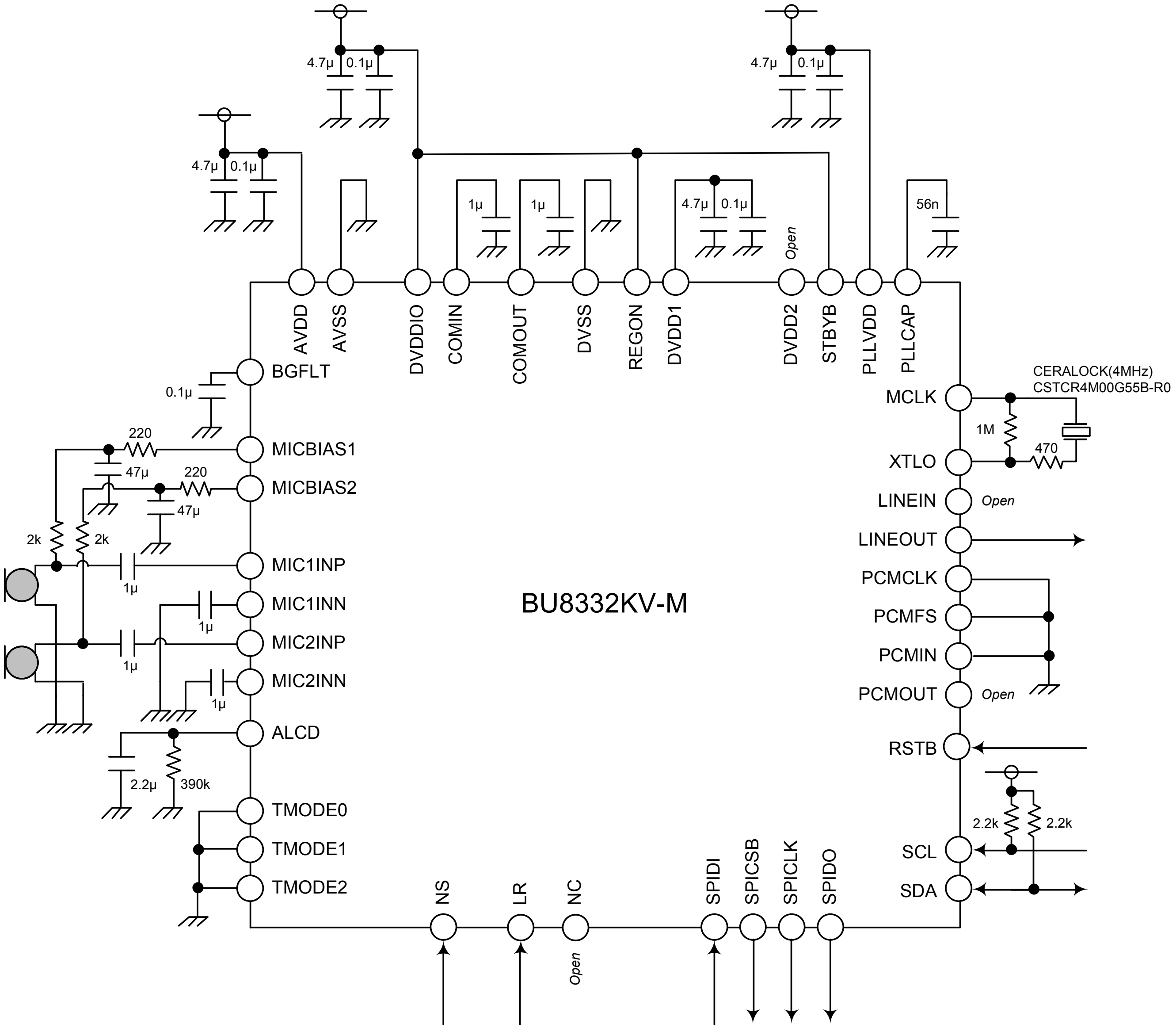


Figure 42 Application Circuit

Application circuit above shows line output. Please follow Timing Chart described earlier. DVDDIO should be selected depending on I/O interface voltage level requirement, without exceeding the maximum specification. PCM output may be used if required. An EEPROM may be connected to SPI BUS pins to load register values automatically upon reset.

●Power Dissipation

Power dissipation of BU8332KV-M is 900mW

For operating over 25℃, de-rate the value at 5.6mW/℃.

● I/O equivalent circuits

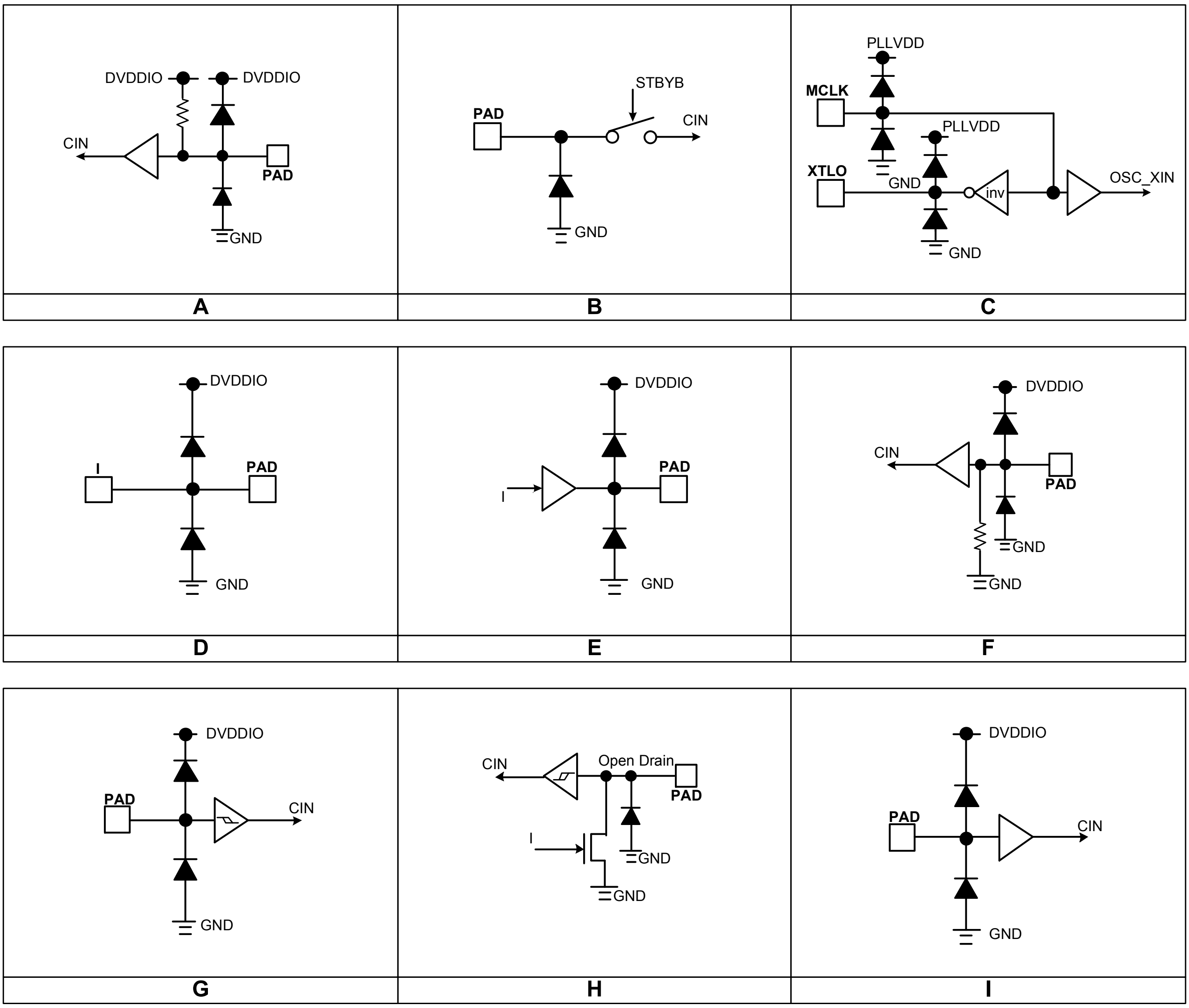


Figure 43 I/O equivalent circuits

●Operational Notes

1) Absolute Maximum Ratings
Exceeding the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify the damage mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

12) About the rush current
For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

13) Others
In case you decide to use this LSI, please contact Rohm for detailed documents like Functional description or Application note.

Status of this document
The Japanese version of this document is the formal specification. A customer may use this translated version only for reference to help understand the formal version.
If there are any differences in translation of this document, the formal version takes priority.

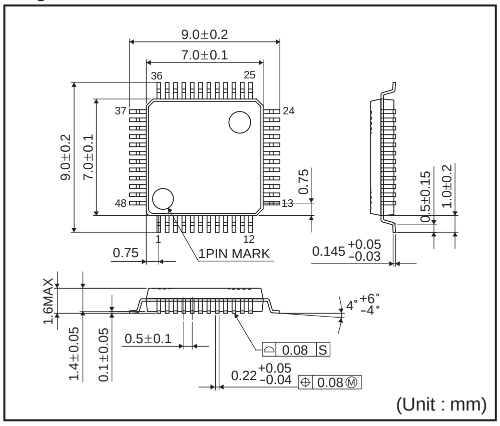
●Ordering Information

B U 8 3 3 2 K V - M E 2

- Part Number
- Package
  KV: VQFP48
- Packaging and forming specification
  E2: Embossed tape and reel

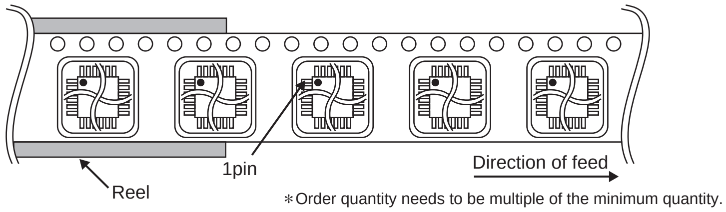
●Physical Dimension Tape and Reel Information

VQFP48



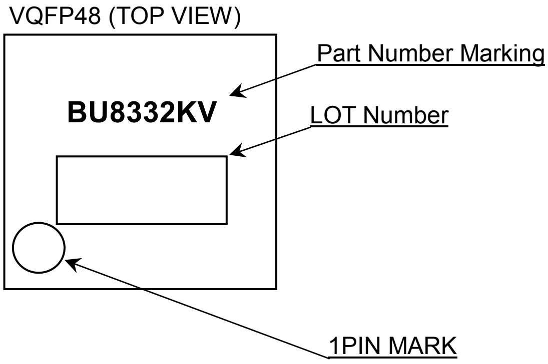
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram



● Revision history

Date	Revision	Changes
2012.10.23	001	New Release
2012.12.05	002	Title was modified. "Signal Processing IC for Ultra- Directional Microphone" →"Signal Processing IC for Ultra- Directional Microphone Effect"
		"Automotive Grade" was added in page 1.
		Typical Application Circuit of Figure 1 was modified.
		"Digital interface characteristic" was added in page 18 to 20.
		Product number of Ceralock in Figure 42 was modified. CSTCR4M0DG55B-R0→CSTCR4M00G55B-R0
		Connection of resister (470Ω) in Figure 42 was modified.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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