



Product Technical Specification & Customer Design Guidelines

AirPrime Q2698



SIERRA
WIRELESS

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Contact Information

Sales Desk:	Phone:	1-604-232-1488
	Hours:	8:00 AM to 5:00 PM Pacific Time
	E-mail:	sales@sierrawireless.com
Post:	Sierra Wireless 13811 Wireless Way Richmond, BC Canada V6V 3A4	
Technical Support:	support@sierrawireless.com	
RMA Support:	repairs@sierrawireless.com	
Fax:	1-604-231-1109	
Web:	www.sierrawireless.com	

Consult our website for up-to-date product descriptions, documentation, application notes, firmware upgrades, troubleshooting tips, and press releases: www.sierrawireless.com

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1. Introduction

The AirPrime Q2698 is an industrial grade penta-band 3G HSPA+ and GPS wireless embedded module. It supports 3G HSPA+ on 5 frequency bands (800/850/900/1900/2100) with dual antenna receive diversity, along with support for 2G GSM/GPRS/EDGE on 4 frequency bands (850/900/1800/1900). It offers a wide range of interfaces including analog and digital audio through its industrial-grade board-to-board connector. It is footprint compatible with other modules from the AirPrime Q26 Series of embedded modules.

The AirPrime Q2698 embedded module supports the Open AT Application Framework, the world's most comprehensive cellular development environment which allows standard ANSI C applications to be natively executed directly on the embedded module.

Once the AirPrime Q2698 embedded module is deployed on the field, it can be monitored and upgraded via the management services of the AirVantage M2M Cloud platform.

1.1. Overall Dimensions

- Dimension:
 - Length: 40 mm
 - Width: 32.2 mm
 - Thickness: 6.2 mm
 - Weight: 11.8 g
- X/Y form-factor compatible with Q2686 and Q2687 embedded modules

1.2. Interfaces

- Digital section running under 2.8 volts and 1.8 volts
- 3V/1V8 UICC/SIM interface
- Complete interfacing:
 - Power supply
 - 45 GPIOs
 - 2 Serial interfaces:
 - 2 SPI Buses
 - I²C Bus
 - 2 Serial links:
 - UART1 (8-wires)
 - UART2 (4-wires)
 - USIM/SIM card
 - USB 2.0 slave HS
 - Analog audio which comprise of:
 - 1 Microphone
 - 1 Speaker
 - PCM digital audio
 - 3 ADCs
 - Buzzer
 - 3 External Interrupts

1.2.1. Connectivity

The AirPrime Q2698 embedded module has the following external connections:

- Three solutions for the main RF antenna, diversity RF antenna and GPS RF antenna connections
 - UFL connector
 - Soldered connection
 - Precidip connection
- Analog and digital interfaces
 - 100 pin I/O connector

1.2.2. Application

The AirPrime Q2698 embedded module includes an application processor, ARM1136 (running up to 480MHz), opened to customers which is supported with the Open AT Application Framework. The Open AT Application Framework includes an extensive set of Libraries, supported by Developer Studio, enabling the creation of natively executed code in C.

The AirPrime Q2698 supports the complete family of software Libraries provided within the Open AT Application Framework (TCP-IP, Internet, GPS, Security).

Note: The operating system allows for the AirPrime Q2698 Embedded Module to be controlled by AT commands. However, some interfaces in the AirPrime Q2698 module may still not be available with AT commands.

1.2.3. Telecom Features

- 3GPP FDD Release 6 HSPA Compliant.
- Penta-Band UMTS/HSPA (WCDMA/FDD) 2100/1900/850/800/900 MHz (band I, II, V, VI, VIII)
 - Downlink data rates up to HSDPA Category 10 (14.4 Mbps).
 - Uplink data rates up to HSUPA Category 6 (5.76 Mbps)
 - Advanced Type III receiver technology supporting simultaneous Receive Diversity and Equalization.
- Quad-Band GSM GPRS EDGE 850/900/1800/1900 MHz
 - GPRS class 12
 - EDGE (E-GPRS) multi-slot class 12
- Dual mode with fully automated handover between 2G and 3G networks
- Voice: HR, FR and EFR; Adaptive multi-rate AMR in GSM & UMTS.

1.2.4. Approvals & Quality

- EU Directive 2002/95/EC on RoHS
 - The AirPrime Q2698 embedded module is compliant with RoHS (Restriction of Hazardous Substances in Electrical and Electronic Equipment) Directive 2002/95/EC which sets limits for the use of certain restricted hazardous substances.
 - This directive states that “from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE)”.
- Regulatory: CE, GCF-CC, PTCRB, FCC/IC (refer to section 8 Certification Compliance and Recommended Standards for more information)
- Manufacturing: ISO/TS 16949

2. Functional Specification

2.1. Functional Architecture

The global architecture of the AirPrime Q2698 embedded module is described in the figure below.

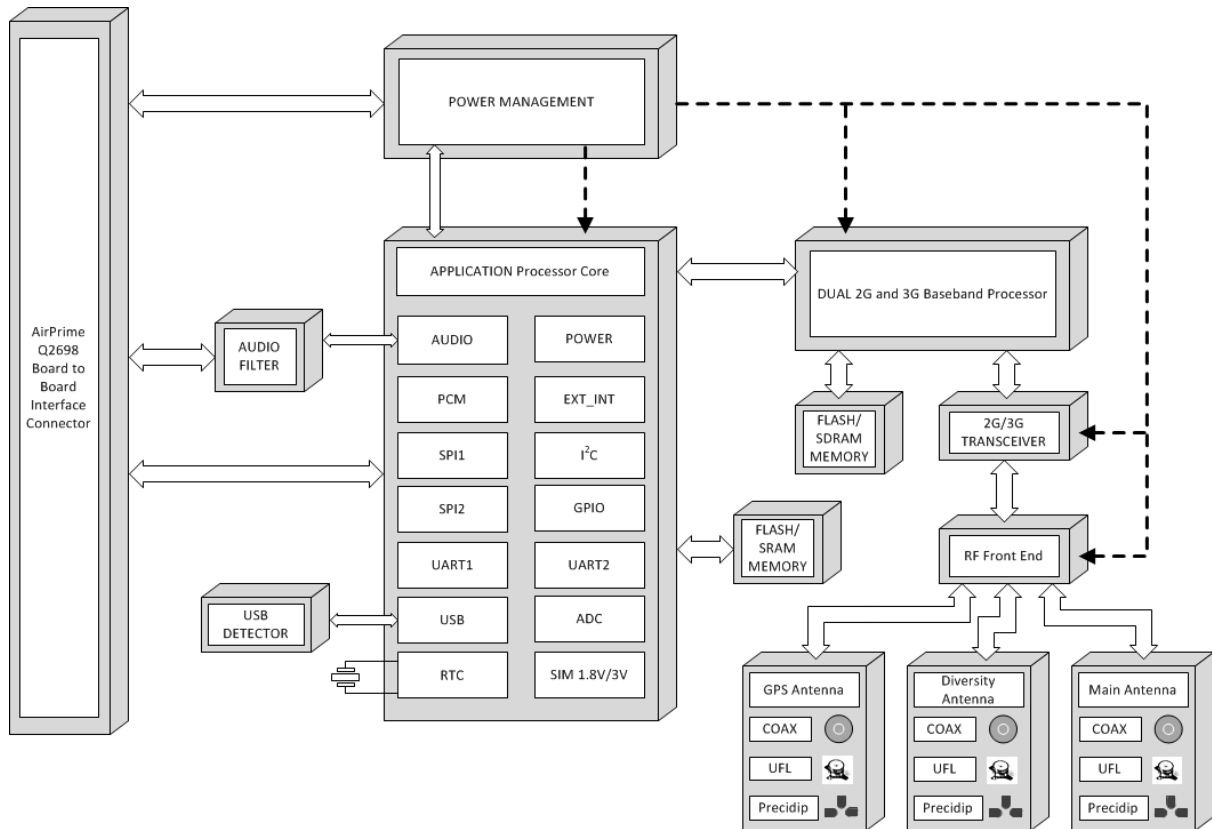


Figure 1. Functional Architecture

2.1.1. RF Functionalities

The Radio Frequency (RF) range complies with the Phase II EGSM 900/DCS 1800 and GSM 850/PCS 1900 recommendations. The frequency range for the transmit band and receive band are given in the table below.

Table 1. RF Frequency Ranges

RF Bandwidth	Transmit Band (Tx)	Receive Band (Rx)
GSM 850	824 to 849 MHz	869 to 894 MHz
E-GSM 900	880 to 915 MHz	925 to 960 MHz
DCS 1800	1710 to 1785 MHz	1805 to 1880 MHz
PSC 1900	1850 to 1910 MHz	1930 to 1990 MHz
WCDMA Band I	1920 to 1980 MHz	2110 to 2170 MHz
WCDMA Band II	1850 to 1910 MHz	1930 to 1990 MHz
WCDMA Band V	824 to 849 MHz	869 to 894 MHz

RF Bandwidth	Transmit Band (Tx)	Receive Band (Rx)
WCDMA Band VI	830 to 840 MHz	875 to 885 MHz
WCDMA Band VIII	880 to 915 MHz	925 to 960 MHz

The Radio Frequency (RF) part is based on a specific multi-band chip with:

- RadioOne ZIF architecture – direct downconversion from RF to analog baseband and direct upconversion from analog baseband to RF
- RadioOne RF transceiver functions
 - Rx and Tx direct conversions, both eliminating their intermediate frequency (IF) components
 - All Rx interstage. SAW filters are eliminated; none required
 - Most Tx interstage. SAW filters are eliminated
- Complete Tx LO source – oscillator and PLL circuits that support all RF operating bands
- Primary and diversity receive paths are designed for equivalent noise-figure performance
- Multiple receiver paths and LO circuits support advanced Rx modes

2.2. Application Framework

The AirPrime Q2698 Embedded Module is Open AT Application Framework compliant. With the Open AT Application Framework, customers can embed their own applications with the AirPrime Q2698 embedded module and turn the AirPrime Q2698 embedded module into a solution for their specific market need.

The operating system allows for the AirPrime Q2698 Embedded Module to be controlled by AT commands. However, some interfaces in the AirPrime Q2698 module may still not be available even with AT command control as these interfaces are dependent on the peripheral devices connected to the AirPrime Q2698 embedded module.



3. Technical Specifications

3.1. Power Supply

The power supply is one of the key issues in the design of a GSM terminal. Due to the burst emission in GSM/GPRS/EGPRS, the power supply must be able to deliver high current peaks in a short time. During these peaks, the ripple (U_{ripp}) on the supply voltage must not exceed a certain limit (refer to Table 2 Input Power Supply Voltage).

Listed below are the corresponding radio burst rates in connected mode:

- GSM/GPRS class 2 terminals emit 577 μ s radio bursts every 4.615ms (see Figure 2 Power Supply During Burst Emission)
- GPRS class 10 terminals emit 1154 μ s radio bursts every 4.615ms

In connected mode, the RF Power Amplifier current (2.1A peak in GSM /GPRS mode) flows with a ratio of:

- 1/8 of the time (577 μ s every 4.615ms for GSM /GPRS cl. 2)
 - 2/8 of the time (1154 μ s every 4.615ms for GSM /GPRS cl. 10)
- and
- 4/8 of the time (2302 μ s every 4.615ms for GSM /GPRS cl. 12)
- with the rising time at around 10 μ s.

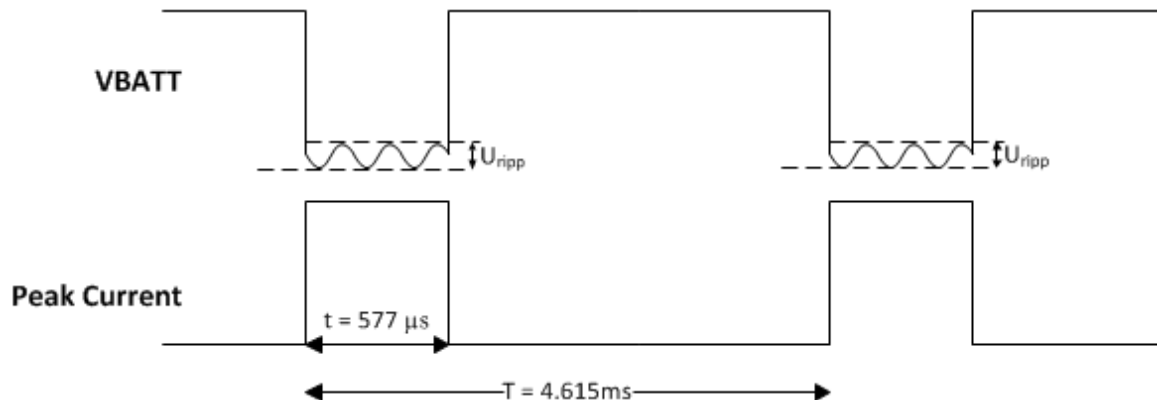


Figure 2. Power Supply During Burst Emission

Only the VBATT input is necessary to supply the Q2698 embedded module. VBATT also provides for the following functions:

- Directly supplies the RF components with 3.8V. (Note that it is essential to keep a minimum voltage ripple at this connection in order to avoid any phase error or spectrum modulation degradation. On the other hand, insufficient power supply could dramatically affect some RF performances such as TX power, modulation spectrum, EMC performance, spurious emission and frequency error.)
- Internally used to provide through several regulators, power supplies VCC_2V8 and VCC_1V8, which are needed for the baseband signals.

The Q2698 embedded module shielding case is the grounding. The ground must be connected on the motherboard through a complete layer on the PCB.

The following table describes the electrical characteristics of the input power supply voltage that will guarantee nominal functioning of the Q2698 embedded module.

Table 2. Input Power Supply Voltage

	V _{MIN}	V _{NOM}	V _{MAX}	I _{AVERAGE Max}	I _{PEAK Max}
VBATT ^{1,2}	3.4V	3.8V	4.2V	1.1A	2.1A

1 This value must be guaranteed during the burst (with 2.1A Peak in GSM or GPRS mode)

2 Max operating Voltage Stationary Wave Ratio (VSWR) 2:1

As the radio power amplifier is directly connected to VBATT, the embedded module is sensitive to any Alternative Current on lines. When a DC/DC converter is used, Sierra Wireless recommends setting the converter frequency in such a way that the resulting voltage does not exceed the values in following table.

Table 3. Maximum Voltage Ripple (U_{ripp}) vs. Frequency

Frequency (Hz)	U _{ripp Max} (mVpp)
f ≤ 300	80
300 < f ≤ 800	10
800 < f ≤ 1100	30
f > 1100	60

When the embedded module is supplied with a battery, the total impedance (battery + protections + PCB) should be < 150mΩ.

When the embedded module is in Alarm/Off mode, no voltage has to be applied on any pin of the 100-pin connector, except on VBATT (pins 1 to 4), BAT-RTC (pin 7) for RTC operation or ON/~OFF (pin 19) to power-ON the embedded module.

3.1.1. Power Supply Pin-Out

Table 4. Power Supply Pin-Out

Signal	Pin Number
VBATT	1, 2, 3, 4
GND	Shielding, 82, 97, 98, 99, 100

The grounding connection is made through the shielding; therefore, the four leads must be soldered to the ground plane.

3.1.2. Decoupling of Power Supply Signals

Decoupling capacitors on VBATT lines are embedded in the AirPrime Q2698 embedded module. Hence, it should not be necessary to add decoupling capacitors close to the embedded module.

However, in case of EMI/RFI problems, the VBATT signal may require some EMI/RFI decoupling – parallel 33pF capacitor close to the embedded module or a serial ferrite bead (or both to get better results). Low frequency decoupling capacitors (22μF to 100μF) may be used to reduce TDMA noise (217Hz).

Caution: *When ferrite beads are used, the recommendation given for the power supply connection must be followed with care (as high current capacity and low impedance).*

3.2. Mechanical Specifications

3.2.1. Physical Characteristics

The AirPrime Q2698 embedded module has a complete self-contained shield.

- Overall dimensions : 32.2x40x6.2 mm (except shielding pins)
- Weight : 11.8 g

3.2.2. Mechanical Drawings

The mechanical specifications of the AirPrime Q2698 embedded module are shown in the following figures.

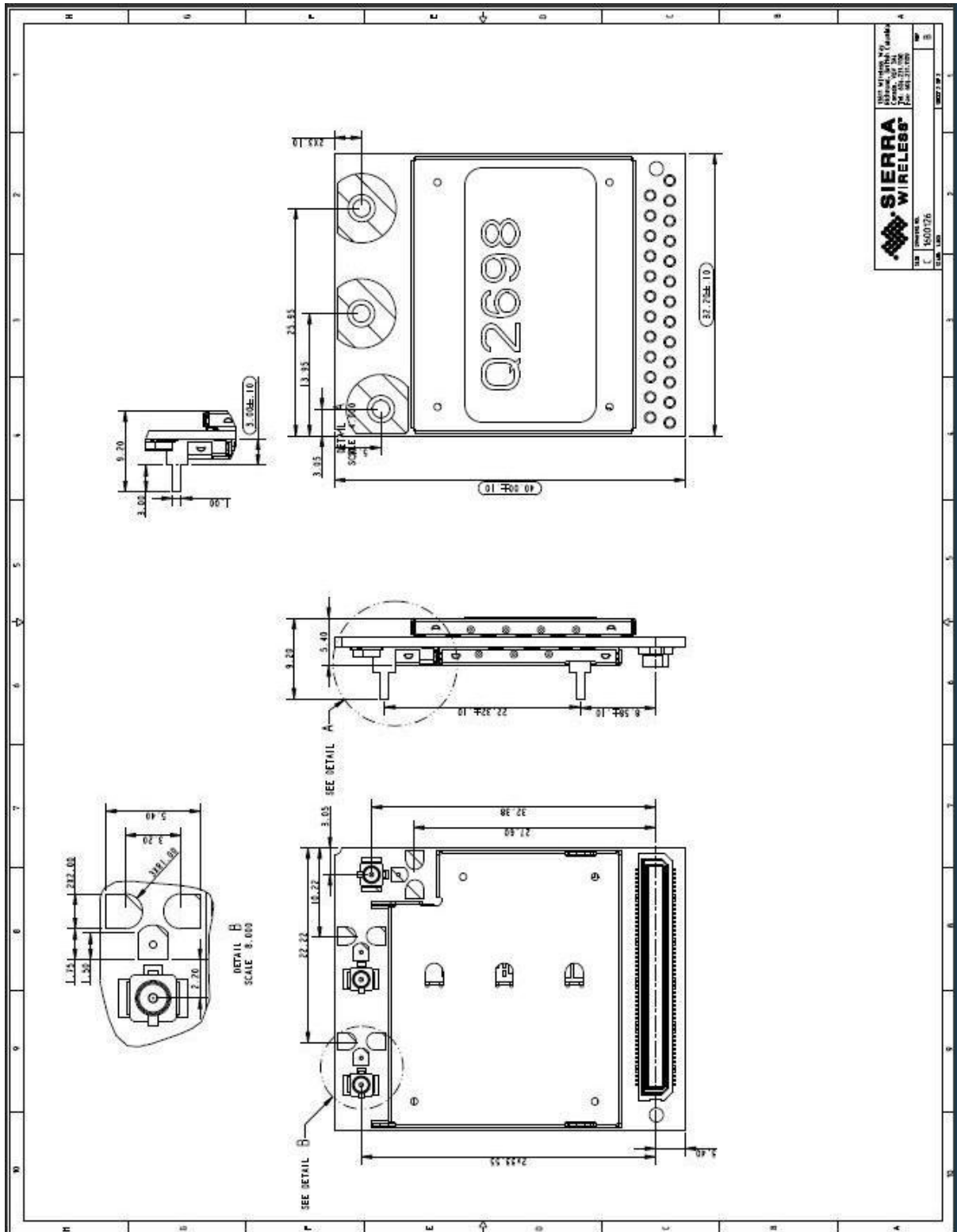


Figure 3. Mechanical Drawing

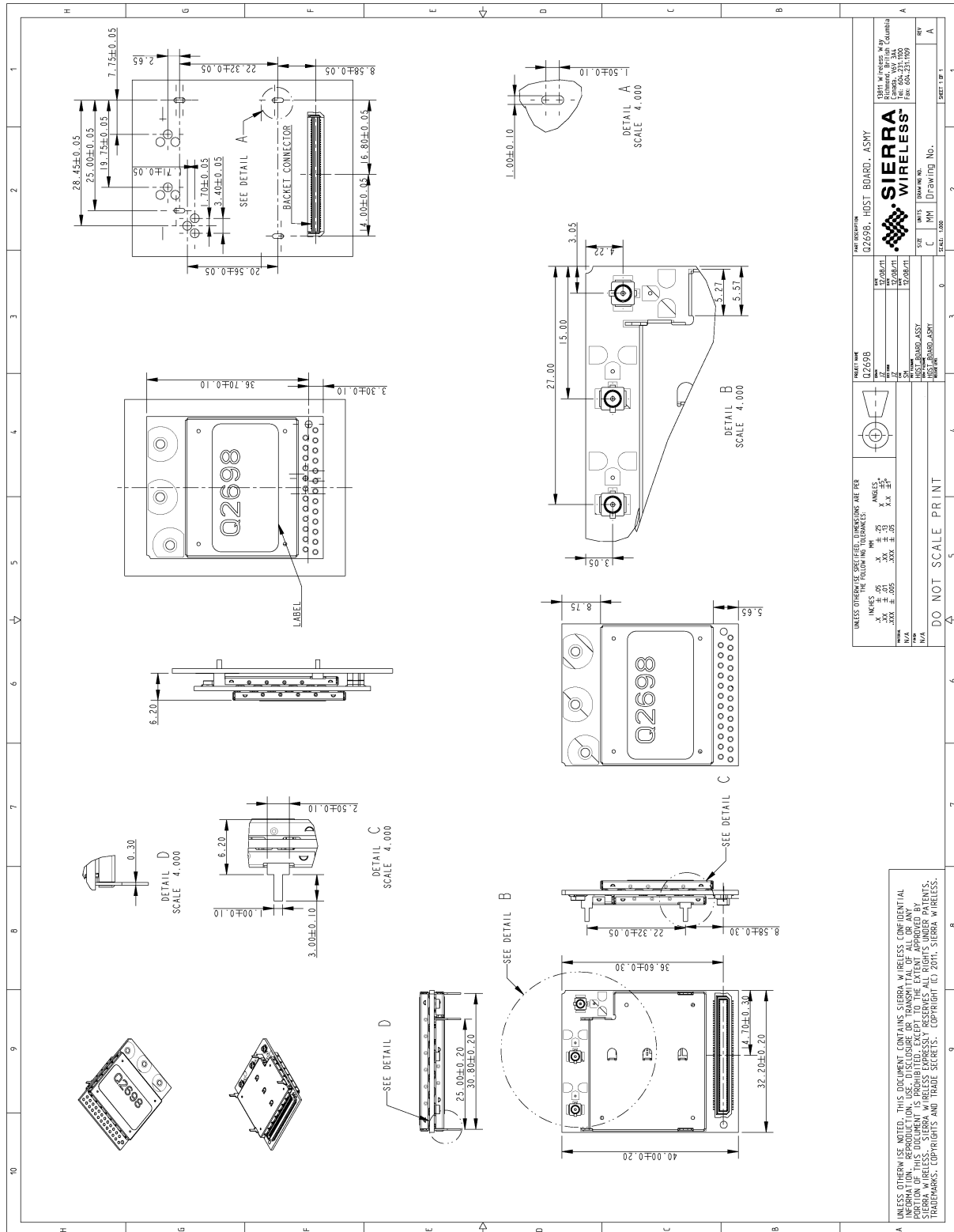


Figure 4. Maximum Bulk Occupied on the Host Board

PART NO.		Q2698	
REV		0	
DATE		12/20/11	
DRAWN BY		C. L. LIND	
CHECKED BY		P. H. DREWING NO.	
APPROVED BY		N/A	
TITLE		HOST BOARD ASSY	
SHEET NO.		1	
SHEET TOTAL		1	

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE PER THE FOLLOWING TOLERANCES ARE PER:

X INCHES	±.05	MM	±.25
ANGLES	±.10	X.X	±.1
XX	±.01	XX	±.05
XXX	±.005	XXX	±.03

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4. Interfaces

Note: Some of the Embedded Module interface signals are multiplexed in order to limit the number of pins but this architecture includes some restrictions.

4.1. General Purpose Connector

The AirPrime Q2698 embedded module is interfaced to the application board through a 100-pin connector.

The following table lists the interfaces and signals available from the general purpose connector and specifies whether these interfaces and signals are driven by AT commands, Open AT, or both.

Table 5. Available Interfaces and Signals

Name	Driven by AT Commands	Driven by Open AT
Analog Audio Interface	✓	✓
Analog to Digital Converter	✓	✓
Auxiliary Serial Link	✓	✓
BAT-RTC (Backup Battery)		
Battery Charging Interface		
Buzzer Output	✓	✓
Digital Audio Interface (PCM)		✓
External Interruption	✓	✓
General Purpose IO	✓	✓
Keyboard Interface		
LED0 signal	✓	✓
Main Serial Link	✓	✓
Serial Interface		✓
USB 2.0 Interface	✓	✓
USIM Interface	✓	✓
VCC_2V8 and VCC_1V8		

4.1.1. Pin Configuration

The following figure shows the pin configuration of the AirPrime Q2698 embedded module; pin assignments are enumerated and described in section 4.1.2 Pin Description.

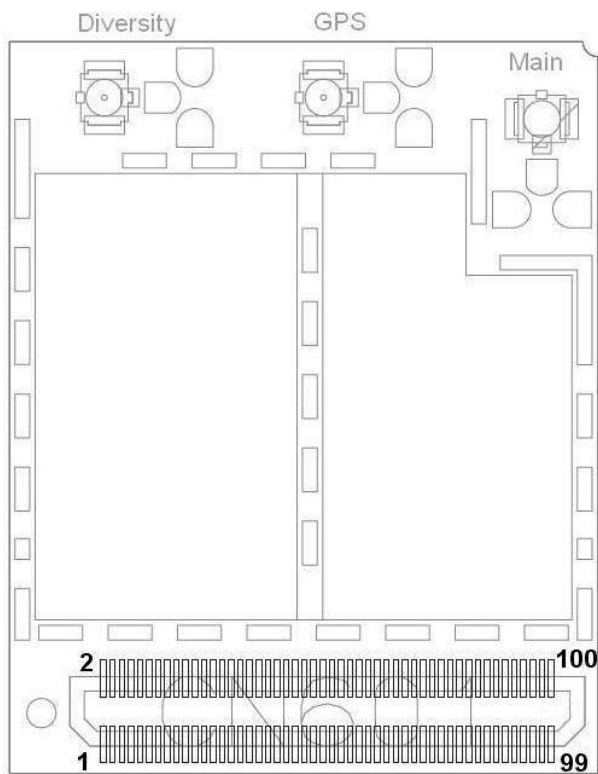


Figure 5. AirPrime Q2698 Pin Configuration

4.1.2. Pin Description

Refer to the following table for the pin description of the general purpose connector.

Table 6. General Purpose Connector Pin Description

Pin #	Signal Name		Voltage	I/O*	Description
	Nominal	Mux			
1	VBATT		3.4V~4.2V	I	Power Supply
2	VBATT		3.4V~4.2V	I	Power Supply
3	VBATT		3.4V~4.2V	I	Power Supply
4	VBATT		3.4V~4.2V	I	Power Supply
5	VCC_1V8		VCC_1V8	O	1.8V Supply Output
6	NC				Not Connected
7	BAT-RTC		BAT-RTC	I/O	RTC Battery connection
8	NC				Not Connected
9	SIM-VCC		1V8 or 3V	O	USIM Power Supply
10	VCC_2V8		VCC_2V8	O	2.8V Supply Output
11	SIM-IO		1V8 or 3V	O	USIM Data
12	SIMPRES	GPIO18	VCC_1V8	I	USIM Detection

Pin #	Signal Name		Voltage	I/O*	Description
	Nominal	Mux			
13	~SIM-RST		1V8 or 3V	O	USIM Reset
14	SIM-CLK		1V8 or 3V	O	USIM Clock
15	BUZZER0		Open Drain	O	Buzzer Output
16	NC				Not Connected
17	LED0		Open Drain	O	LED0 Output
18	~RESET		VCC_1V8	I/O	RESET Input
19	ON/~OFF		VBATT	I	ON / ~OFF Control
20	ADC1		Analog	I	Analog temperature
21	ADC2		Analog	I	Analog to Digital Input
22	GPIO31		VCC_2V8	I/O	General Purpose Input / Output
23	SPI1-CLK	GPIO28	VCC_2V8	O	SPI1 Clock
24	SPI1-I	GPIO30	VCC_2V8	I	SPI1 Data Input
25	SPI1-IO	GPIO29	VCC_2V8	I/O	SPI1 Data Input / Output
26	SPI2-CLK	GPIO32	VCC_2V8	O	SPI2 Clock
27	SPI2-IO	GPIO33	VCC_2V8	I/O	SPI2 Data Input / Output
28	GPIO35		VCC_2V8	I/O	General Purpose Input / Output
29	SPI2-I	GPIO34	VCC_2V8	I	SPI2 Data Input
30	GPIO15	CT104-RXD2	VCC_1V8	I/O	General Purpose Input / Output
31	GPIO14	CT103-TXD2	VCC_1V8	I/O	General Purpose Input / Output
32	GPIO16	~CT106-CTS2	VCC_1V8	I/O	General Purpose Input / Output
33	GPIO17	~CT105-RTS2	VCC_1V8	I/O	General Purpose Input / Output
34	NC				Not Connected
35	SPK1P		Analog	O	Speaker 1 Output Positive
36	NC				Not Connected
37	SPK1N		Analog	O	Speaker 1 Output Negative
38	MIC1N		Analog	I	Micro 1 Input Negative
39	NC				Not Connected
40	MIC1P		Analog	I	Micro 1 Input Positive
41	NC				Not Connected
42	ADC3		Analog	I	Analog to Digital Input
43	GPIO0		VCC_2V8	I/O	General Purpose Input / Output
44	SCL1	GPIO26	Open Drain	O	I ² C Clock
45	SPI1_CS	GPIO19	VCC_2V8	O	SPI_1 Chip Select
46	SDA1	GPIO27	Open Drain	I/O	I ² C Data
47	SPI2_CS	GPIO21	VCC_2V8	I/O	SPI_2 Chip Select
48	GPIO20		VCC_2V8	I/O	General Purpose Input / Output
49	INT1	GPIO25	VCC_2V8	I/O	External Interrupt
50	INT0	GPIO3	VCC_1V8	I/O	External Interrupt
51	INT2	GPIO1	VCC_1V8	I/O	External Interrupt
52	VPAD-USB		VPAD-USB	I	USB Power supply input

Pin #	Signal Name		Voltage	I/O*	Description
	Nominal	Mux			
53	GPIO2		VCC_1V8	I/O	General Purpose Input / Output
54	USB-DP		VPAD-USB	I/O	USB Data
55	GPIO23		VCC_2V8	I/O	General Purpose Input / Output
56	USB-DM		VPAD-USB	I/O	USB Data
57	GPIO22		VCC_2V8	I/O	General Purpose Input / Output
58	GPIO24		VCC_2V8	I/O	General Purpose Input / Output
59	GPIO4		VCC_1V8	I/O	General Purpose Input / Output
60	GPIO5		VCC_1V8	I/O	General Purpose Input / Output
61	GPIO6		VCC_1V8	I/O	General Purpose Input / Output
62	GPIO7		VCC_1V8	I/O	General Purpose Input / Output
63	GPIO8		VCC_1V8	I/O	General Purpose Input / Output
64	GPIO13	TX_Burst	VCC_1V8	O	General Purpose Input / Output; TX Burst Signal Output
65	GPIO12		VCC_1V8	I/O	General Purpose Input / Output
66	GPIO11		VCC_1V8	I/O	General Purpose Input / Output
67	GPIO10		VCC_1V8	I/O	General Purpose Input / Output
68	GPIO9		VCC_1V8	I/O	General Purpose Input / Output
69	~CT125-RI	GPIO42	VCC_2V8	O	Main RS232 Ring
70	~CT109-DCD1	GPIO43	VCC_2V8	O	Main RS232 Data
71	CT103-TXD1	GPIO36	VCC_2V8	I	Main RS232 Transmit
72	~CT105-RTS1	GPIO38	VCC_2V8	I	Main RS232 Request To Send
73	CT104-RXD1	GPIO37	VCC_2V8	O	Main RS232 Receive
74	~CT107-DSR1	GPIO40	VCC_2V8	O	Main RS232 Data Set Ready
75	~CT106-CTS1	GPIO39	VCC_2V8	O	Main RS232 Clear To Send
76	~CT108-2-DTR1	GPIO41	VCC_2V8	I	Main RS232 Data Terminal Ready
77	PCM-SYNC		VCC_1V8	O	PCM Frame Synchro
78	PCM-IN		VCC_1V8	I	PCM Data Input
79	PCM-CLK		VCC_1V8	O	PCM Clock
80	PCM-OUT		VCC_1V8	O	PCM Data Output
81	NC				Not Connected
82	GND		GND		Ground
83	GPIO44		VCC_1V8	I/O	General Purpose Input / Output
84	NC				Not Connected
85	NC				Not Connected
86	NC				Not Connected
87	NC				Not Connected
88	NC				Not Connected
89	NC				Not Connected
90	NC				Not Connected
91	NC				Not Connected
92	NC				Not Connected
93	NC				Not Connected
94	NC				Not Connected

Pin #	Signal Name		Voltage	I/O*	Description
	Nominal	Mux			
95	NC				Not Connected
96	NC				Not Connected
97	GND		GND		Ground
98	GND		GND		Ground
99	GND		GND		Ground
100	GND		GND		Ground

* The I/O direction information is only for the nominal signal. When the signal is configured in GPIO, it can always be an Input or an Output.

Caution: *Unused pins must be left open.*

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

4.2. Electrical Information for Digital I/O

There are three types of digital I/O on the AirPrime Q2698 embedded module:

- 2.8Volt CMOS
- 1.8Volt CMOS
- Open drain

Refer to the tables below for the electrical characteristics of these three digital I/Os.

Table 7. Electrical Characteristics of a 2.8 Volts Type (2V8) Digital I/O

Parameter	I/O Type	Minimum	Typical	Maximum	Condition	
Internal 2.8V power supply	VCC_2V8	2.74V	2.8V	2.86V		
Input / Output pin	V _{IL}	CMOS	-0.5V*	0.6V		
	V _{IH}	CMOS	1.96V	3.2V*		
	V _{OL}	CMOS		0.4V	I _{OL} = - 1 mA	
	V _{OH}	CMOS	2.0V		I _{OH} = 150 μA	
	I _{OH}				TBC	
	I _{OL}				TBC	

* Absolute maximum ratings

All 2.8V I/O pins do not accept input signal voltage above the maximum voltage specified above.

Table 8. Electrical Characteristics of a 1.8 Volts Type (1V8) Digital I/O

Parameter		I/O Type	Minimum	Typical	Maximum	Condition
Internal 1V8 power supply		VCC_1V8	1.76V	1.8V	1.94V	
Input / Output pin	V _{IL}	CMOS	-0.5V*		0.54V	
	V _{IH}	CMOS	1.33V		2.2V*	
	V _{OL}	CMOS			0.4V	I _{OL} = - 4 mA
	V _{OH}	CMOS	1.4V			I _{OH} = 4 mA
	I _{OH}				4mA	
	I _{OL}				- 4mA	

* Absolute maximum ratings

Table 9. Electrical Characteristics of an Open Drain Output Type

Signal Name	Parameter	I/O Type	Minimum	Typical	Maximum	Condition
LED0	V _{OL}	Open Drain			0.4V	
	I _{OL}	Open Drain			8mA	
BUZZER0	V _{OL}	Open Drain			0.4V	
	I _{OL}	Open Drain			100mA	
SDA1/ GPIO27 and SCL1/ GPIO26	V _{TOL}	Open Drain			3.3V	Tolerated voltage
	V _{IH}	Open Drain	2V			
	V _{IL}	Open Drain			0.8V	
	V _{OL}	Open Drain			0.4V	
	I _{OL}	Open Drain			3mA	

The reset states of the I/Os are given in each interface description chapter. Definitions of these states are given in the table below.

Table 10. Reset State Definition

Parameter	Definition
0	Set to GND
1	Set to supply 1V8 or 2V8 depending on I/O type
Pull-down	Internal pull-down with ~100kΩ resistor.
Pull-up	Internal pull-up with ~100kΩ resistor to supply 1V8 or 2V8 depending on I/O type.
Z	High impedance
Undefined	Caution: <i>Undefined must not be used in an application if a special state is required at reset. These pins may be toggling a signal during reset.</i>

4.3. General Purpose Input/Output

The AirPrime Q2698 embedded module provides up to 45 General Purpose I/Os, used to control any external device.

4.3.1. Pin Description

Refer to the following table for the pin description of the GPIO interface.

Table 11. GPIO Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Multiplexed with
GPIO0	43	I/O	2V8	Z	Not mux
GPIO1	51	I/O	1V8	Z	INT2
GPIO2	53	I/O	1V8	Z	Not mux
GPIO3	50	I/O	1V8	Z	INT0
GPIO4	59	I/O	1V8	Z	Not mux
GPIO5	60	I/O	1V8	Z	Not mux
GPIO6	61	I/O	1V8	Z	Not mux
GPIO7	62	I/O	1V8	Z	Not mux
GPIO8	63	I/O	1V8	Z	Not mux
GPIO9	68	I/O	1V8	Z	Not mux
GPIO10	67	I/O	1V8	Z	Not mux
GPIO11	66	I/O	1V8	Z	Not mux
GPIO12	65	I/O	1V8	Z	Not mux
GPIO13*	64	I/O	1V8	Z	TX_Burst
GPIO14	31	I/O	1V8	Z	CT103-TXD2
GPIO15	30	I/O	1V8	Z	CT104-RXD2
GPIO16	32	I/O	1V8	Z	~CT106-CTS2
GPIO17	33	I/O	1V8	Z	~CT105-RTS2
GPIO18	12	I/O	1V8	Z	SIMPRES
GPIO19	45	I/O	2V8	Z	SPI1_CS
GPIO20	48	I/O	2V8	Z	Not mux
GPIO21	47	I/O	2V8	Z	SPI2_CS
GPIO22	57	I/O	2V8	Z	Not mux
GPIO23	55	I/O	2V8	Z	Not mux
GPIO24	58	I/O	2V8	Z	Not mux
GPIO25	49	I/O	2V8	Z	INT1
GPIO26	44	I/O	Open drain	Z	SCL1
GPIO27	46	I/O	Open drain	Z	SDA1
GPIO28	23	I/O	2V8	Z	SPI1-CLK
GPIO29	25	I/O	2V8	Z	SPI1-IO
GPIO30	24	I/O	2V8	Z	SP1-I
GPIO31	22	I/O	2V8	Z	Not mux
GPIO32	26	I/O	2V8	Z	SPI2-CLK
GPIO33	27	I/O	2V8	Z	SPI2-IO

Signal	Pin #	I/O	I/O Type	Reset State	Multiplexed with
GPIO34	29	I/O	2V8	Z	SPI2-I
GPIO35	28	I/O	2V8	Z	Not mux
GPIO36	71	I/O	2V8	Z	CT103-TXD1
GPIO37	73	I/O	2V8	Z	CT104-RXD1
GPIO38	72	I/O	2V8	Z	~CT105-RTS1
GPIO39	75	I/O	2V8	Z	~CT106-CTS1
GPIO40	74	I/O	2V8	Z	~CT107-DSR1
GPIO41	76	I/O	2V8	Z	~CT108-2-DTR1
GPIO42	69	I/O	2V8	Z	~CT125-RI1
GPIO43	70	I/O	2V8	Z	~CT109-DCD1
GPIO44	83	I/O	2V8	Z	Not mux

* GPIO13 is the associated GPIO used with **AT+WTBI** to monitor TX bursts. Refer to section 5.7 TX Burst Indication for more information about TX bursts and document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information about **AT+WTBI**.

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

4.4. Serial Interface

The AirPrime Q2698 embedded module provides two SPI bus (4-wire interface) and an I²C bus (2-wire interface).

4.4.1. SPI Bus

Both SPI bus interface includes:

- A CLK signal
- An O signal
- An I signal
- A CS (Chip Select) signal

4.4.1.1. Characteristics

The following lists the features available on the SPI bus.

- Master mode operation
- SPI speed is from 128 kbit/s to 13 Mbit/s in master mode operation
- 4-wire interface
- 4 to 32 bits data length

4.4.1.2. SPI Configuration

Table 12. SPI Configuration

Operation	Maximum Speed	SPI-Mode	Duplex	4-wire Type
Master	13 Mb/s	0, 1, 2, 3	Half	SPIx-CLK; SPIx-IO; SPIx-I; SPIx_CS

For the 4-wire configuration, SPIx-I/O is used as output only, SPIx-I is used as input only.

4.4.1.3. SPI Waveforms

The following shows waveforms for SPI transfer with 4-wire configuration in master mode 0.

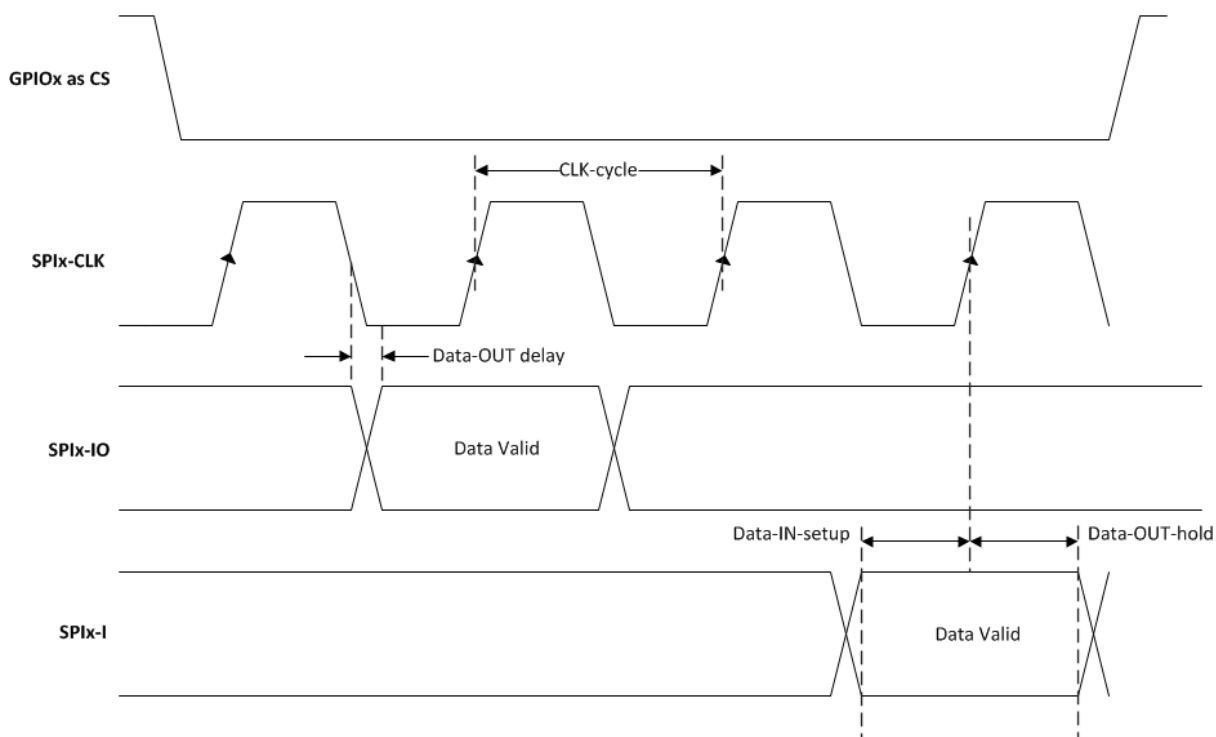


Figure 6. SPI Timing Diagrams; Mode 0, Master, 4 wires

Table 13. AC Characteristics of the SPI Bus

Signal	Description	Minimum	Typical	Minimum	Unit
CLK-cycle	SPI clock frequency	0.102		13	MHz
Data-OUT delay	Data out ready delay time			10	ns
Data-IN-setup	Data in setup time	2			ns
Data-OUT-hold	Data out hold time	2			ns

4.4.1.4. SPI1 Pin Description

Refer to the following table for the pin description of the SPI1 interface.

Table 14. SPI1 Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
SPI1-CLK	23	O	2V8	Z	SPI1 Serial Clock	GPIO28
SPI1-I	24	I	2V8	Z	SPI1 Serial input	GPIO30
SPI1-IO	25	I/O	2V8	Z	SPI1 Serial input/output	GPIO29
SPI1_CS	45	O	2V8	Z	SPI1 Chip Select	GPIO19

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

4.4.1.5. SPI2 Pin Description

Refer to the following table for the pin description of the SPI2 interface.

Table 15. SPI2 Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
SPI2-CLK	26	O	2V8	Z	SPI2 Serial Clock	GPIO32
SPI2-IO	27	I/O	2V8	Z	SPI2 Serial input/output	GPIO33
SPI2-I	29	I	2V8	Z	SPI2 Serial input	GPIO34
SPI2_CS	47	O	2V8	Z	SPI2 Chip Select	GPIO21

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

Caution: *SPI2 pins can only be used when UART2 pins are not in use. Refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information about switching between the two interfaces.*

4.4.1.6. Application

A 4-wire SPI configuration has the input and output data lines disassociated. The SPIx-IO signal is used only for output data whereas the SPIx-I signal is used only for input data.

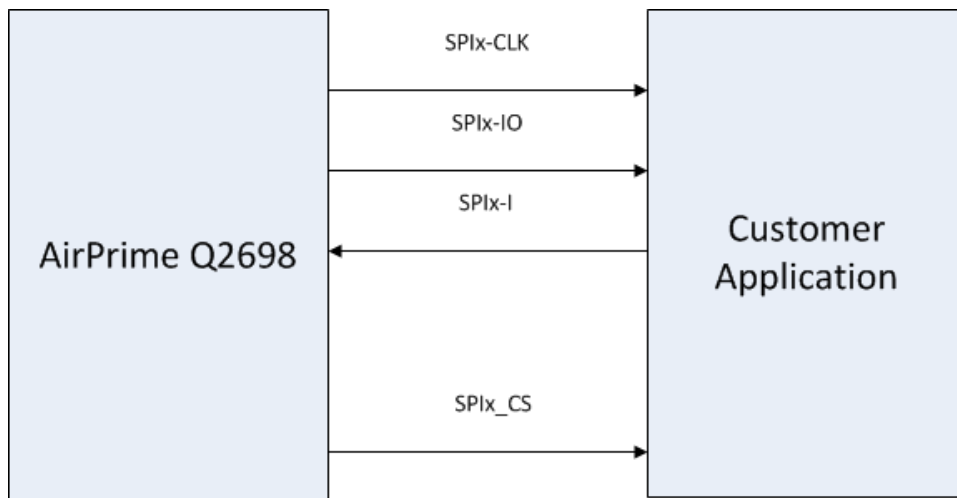


Figure 7. Example of 4-wire SPI Bus Application

4.4.2. I²C Bus

The I²C interface includes a clock signal (SCL1) and data signal (SDA1) complying with a 100kbit/s-standard interface (standard mode: s-mode). The maximum speed transfer range is 400kbit/s (fast mode: f-mode).

The I²C bus is always in master mode operation.

4.4.2.1. I²C Pin Description

Refer to the following table for the pin description of the I²C interface.

Table 16. I²C Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
SCL1	44	O	Open drain	Z	Serial Clock	GPIO26
SDA1	46	I/O	Open drain	Z	Serial Data	GPIO27

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

4.4.2.2. Application

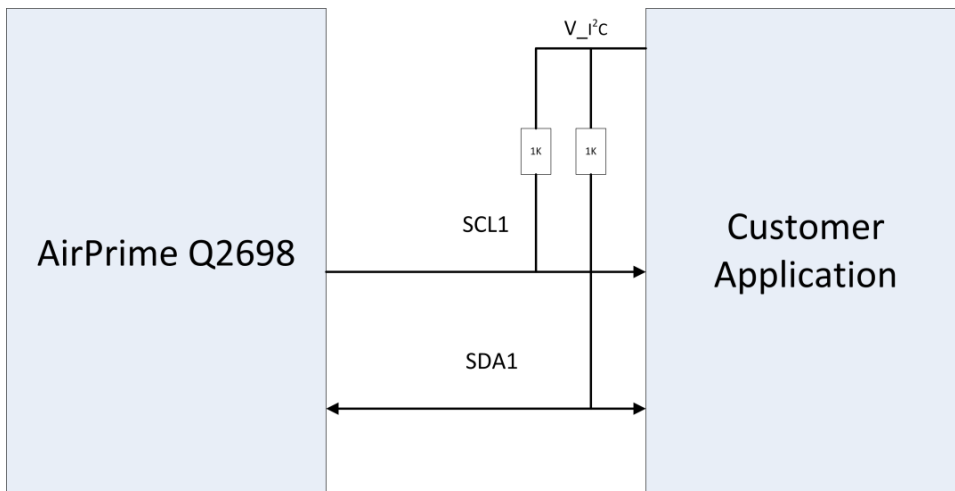


Figure 8. Example1 of an I²C Bus Application

The two lines, SCL1 and SDA1, both need to be pulled-up to the V_{I²C} voltage. The V_{I²C} voltage is dependent on the customer application component connected on the I²C bus, and should be higher than 1.8V. Nevertheless, the V_{I²C} must comply with the AirPrime Q2698 embedded module electrical specifications.

The VCC_2V8 (pin 10) of the AirPrime Q2698 embedded module may be used to connect the pull-up resistors, if the I²C bus voltage is 2.8V.

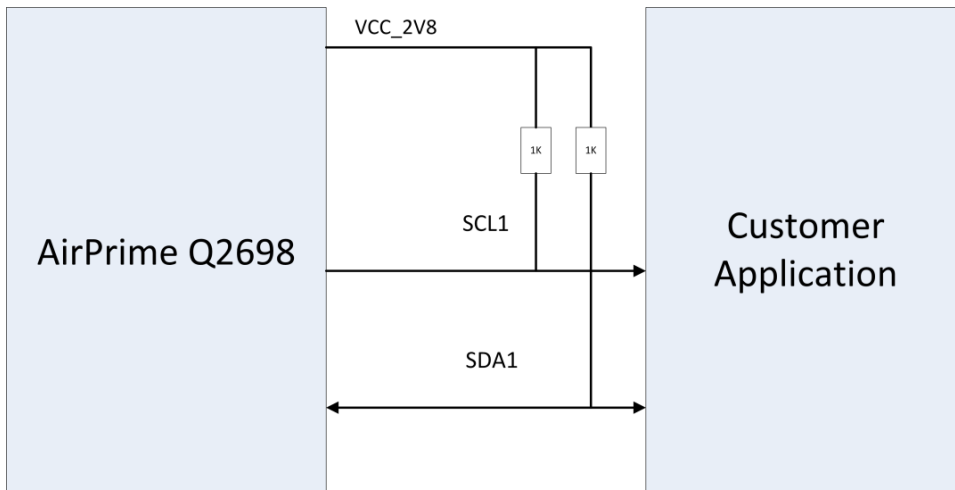


Figure 9. Example2 of an I²C Bus Application

The pull-up resistor values are selected depending on the mode used. For Fast mode, it is recommended to use 1kΩ resistors in order to ensure compliance with the I²C specification. For Standard mode, higher values of resistors may be used to save power consumption.

4.5. Main Serial Link (UART1)

The main serial link (UART1) is used for communication between the Q2698 embedded module and a PC or host processor. It consists of a flexible 8-wire serial interface that complies with V24 protocol signaling, but not with V28 (electrical interface) due to its 2.8 volts interface.

The UART1 interface is 2.8 volts type. However, it is 3.3 volts tolerant.

The signals used by UART1 are:

- TX data (CT103-TX)
- RX data (CT104-RX)
- Request To Send (~CT105-RTS)
- Clear To Send (~CT106-CTS)
- Data Terminal Ready (~CT108-2-DTR)
- Data Set Ready (~CT107-DSR)
- Data Carrier Detect (~CT109-DCD)
- Ring Indicator (CT125-RI)

4.5.1. Pin Description

Refer to the following table for the pin description of the UART1 interface.

Table 17. UART1 Pin Description

Signal*	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
CT103-TXD1	71	I	2V8	Z	Transmit serial data	GPIO36
CT104-RXD1	73	O	2V8	Z	Transmit serial data	GPIO37
~CT105-RTS1	72	I	2V8	Z	Request To Send	GPIO38
~CT106-CTS1	75	O	2V8	Z	Clear To Send	GPIO39
~CT108-2-DTR1	76	I	2V8	Z	Data Terminal Ready	GPIO41
~CT107-DSR1	74	O	2V8	Z	Data Set Ready	GPIO40
~CT109-DCD1	70	O	2V8	Z	Data Carrier Detect	GPIO43
~CT125-RI1	69	O	2V8	Z	Ring Indicator	GPIO42
CT102-GND	Shielding leads		GND		Ground	

* According to PC view

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

With the Open AT Application Framework, when the UART1 service is used, the whole multiplexed signals become unavailable for other purposes. In the same way, if one or more GPIOs (from the table above) are allocated elsewhere, the UART1 service becomes unavailable.

The **rise** and **fall time** of the reception signals (mainly ~CT103-TXD1) must be less than 300ns.

The maximum baud rate of UART1 is 921kbit/s for the Open AT Application Framework.

Note: UART1 of the AirPrime Q2698 embedded module is designed to operate using all serial interface signals. In particular, it is recommended to use ~CT105-RTS1 and ~CT106-CTS1 for hardware flow control in order to avoid data loss/corruption during transmission.

4.5.2. Level Shifter Implementation

The voltage level shifter must be 2.8V with V28 electrical signal compliance.

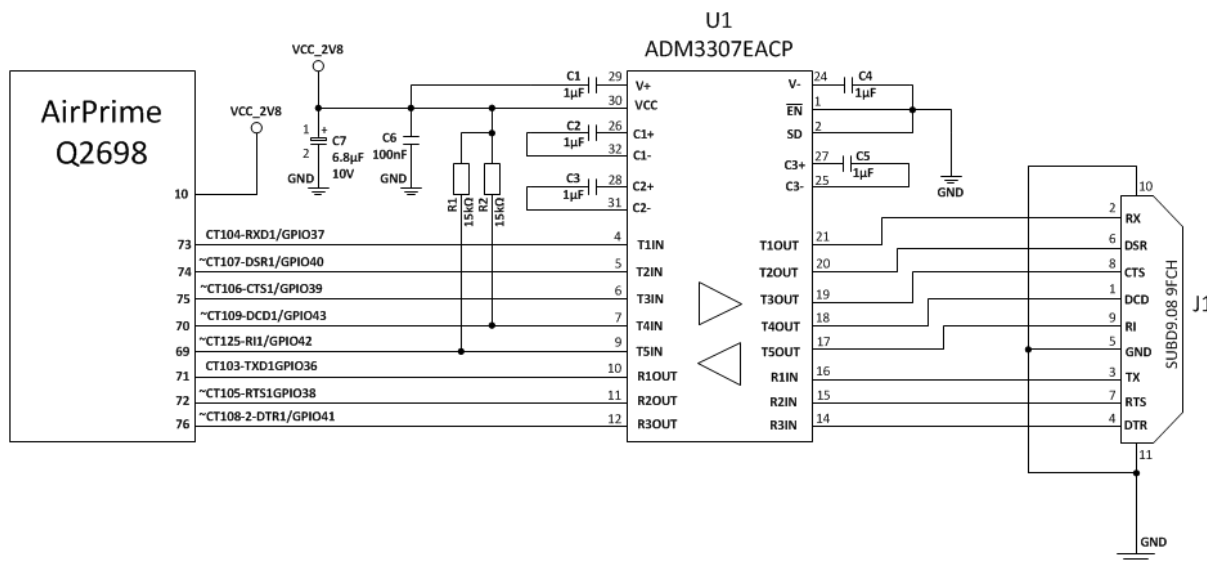


Figure 10. Example of RS-232 Level Shifter Implementation for UART1

Note: The U1 chip also protects the embedded module against ESD at 15kV (air discharge).

4.5.2.1. Recommended Components

- R1, R2: 15kΩ
- C1, C2, C3, C4, C5: 1µF
- C6: 100nF
- C7: 6.8µF TANTAL 10V CP32136 AVX
- U1: ADM3307AACP Analog devices
- J1: SUB-D9 female

R1 and R2 are only necessary during the Reset state, to force the ~CT1125-RI1 and ~CT109-DCD1 signals to high levels.

The ADM3307EACP chip has a maximum speed of 921kbits/s. If other level shifters are used, ensure that their speeds are compliant with the UART1 useful speed.

The ADM3307EACP can be powered either by VCC_2V8 (pin 10) of the AirPrime Q2698 embedded module or by an external regulator at 2.8 volts.

If the UART1 interface is connected directly to a host processor, it is not necessary to use level shifters. The interface can be connected as shown in the following sub-section.

4.5.3. V24/CMOS Possible Design

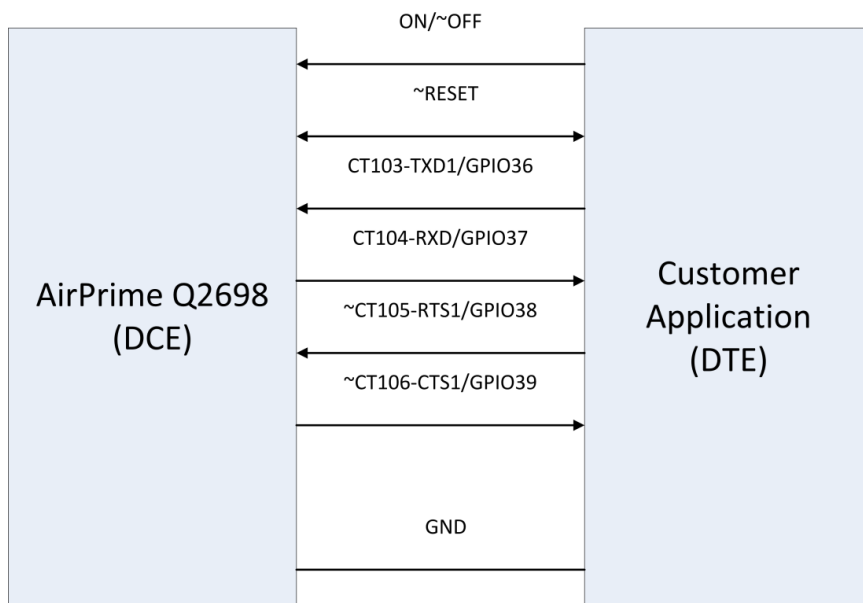


Figure 11. Example of V24/CMOS Serial Link Implementation for UART1

The design shown above is a basic design type. A more flexible design to access this serial link with all the modem signals is shown below.

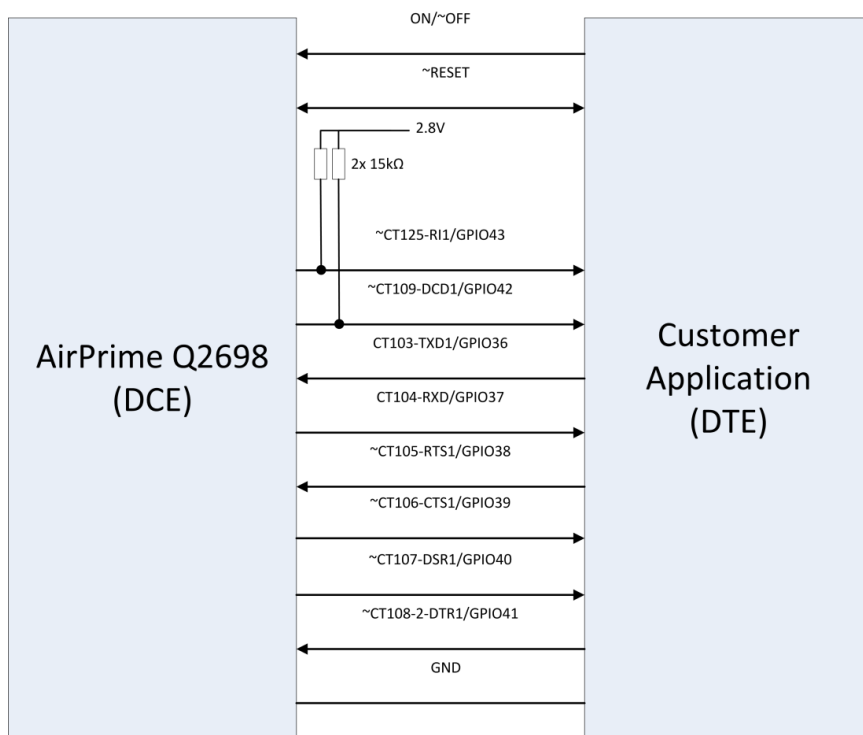


Figure 12. Example of a Full Modem V24/CMOS Serial Link Implementation for UART1

It is recommended to add 15kΩ pull-up resistors on ~CT125-RI1 and ~CT109-DCD1 signals to set them to high level during the reset state.

4.5.4. 5-wire Serial Interface

The signals used in this interface are:

- CT103-TXD1
- CT104-RXD1
- ~CT105-RTS1
- ~CT106-CTS1
- ~CT108-2/DTR1

The signal ~CT108-2-DTR1 must be managed by following the V24 protocol signaling, if sleep idle mode is to be used.

Other signals and their multiplexed GPIOs are not available.

Please refer to the technical appendixes of document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information.

4.5.5. 4-wire Serial Interface

The signals used in this interface are:

- CT103-TXD1
- CT104-RXD1
- ~CT105-RTS1
- ~CT106-CTS1

The signal ~CT108-2-DTR1 must be configured at low level.

Other signals and their multiplexed GPIOs are not available.

Please refer to the technical appendixes of document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information.

4.5.6. 2-wire Serial Interface

Caution: *This case is possible for a connected external chip, but not recommended (and forbidden for AT command or modem use).*

The flow control mechanism has to be managed from the customer side. The signals used in this interface are:

- CT103-TXD1
- CT104-RXD1

Signals ~CT108-2-DTR1 and ~CT105-RTS1 must be configured at low level.

Signals ~CT105-RTS1 and ~CT106-CTS1 are not used; default hardware flow control on UART1 should be de-activated using AT command **AT+IFC=0,0**. Refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information.

Other signals and their multiplexed GPIOs are not available.

Please refer to the technical appendixes of document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information.

4.6. Auxiliary Serial Link (UART2)

An auxiliary serial interface (UART2) is available on the AirPrime Q2698 embedded module. This interface may be used to connect a Bluetooth or a GPS chip controlled by a Library.

4.6.1. Pin Description

Refer to the following table for the pin description of the UART2 interface.

Table 18. UART2 Pin Description

Signal*	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
CT103-TXD2	31	I	1V8	Z	Transmit serial data	GPIO14
CT104-RXD2	30	O	1V8	Z	Receive serial data	GPIO15
~CT106-CTS2	32	O	1V8	Z	Clear To Send	GPIO16
~CT105-RTS2	33	I	1V8	Z	Request To Send	GPIO17

* According to PC view

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

Caution: *UART2 pins can only be used when SPI2 pins are not in use. Refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information about switching between the two interfaces.*

The maximum baud rate of UART2 is **921kbit/s** for the Open AT Application Framework.

Note: *UART2 of the AirPrime Q2698 embedded module is designed to operate using all serial interface signals. In particular, it is recommended to use ~CT105-RTS1 and ~CT106-CTS1 for hardware flow control in order to avoid data loss/corruption during transmission.*

4.6.2. Level Shifter Implementation

The voltage level shifter must be 1.8V with V28 electrical signal compliance.

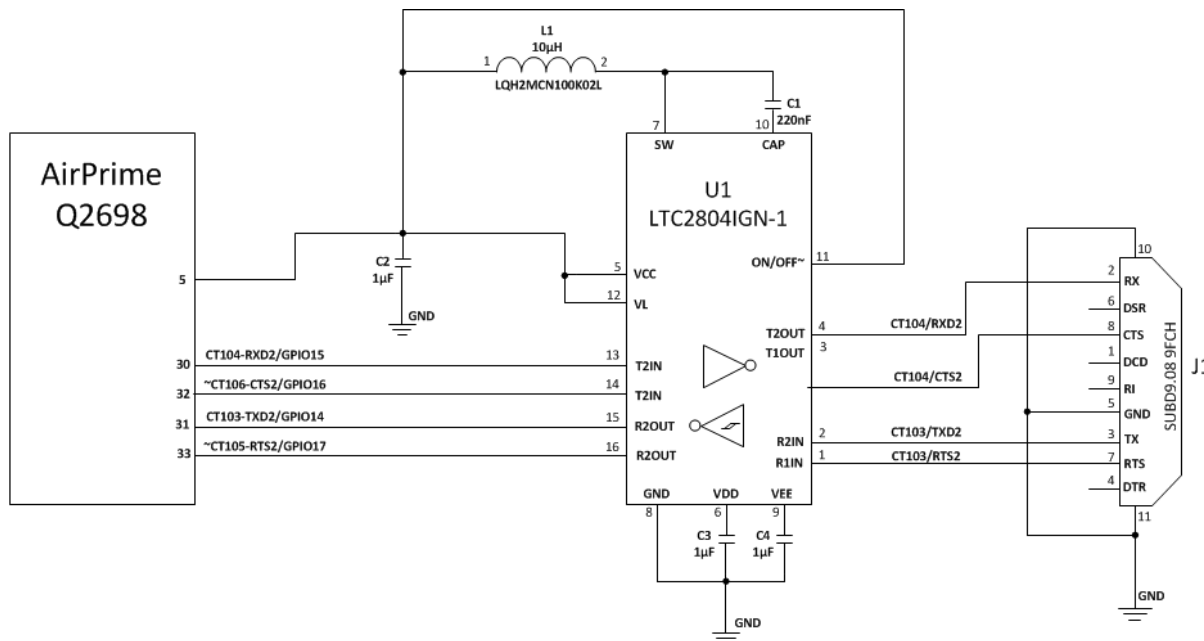


Figure 13. Example of RS-232 Level Shifter Implementation for UART2

4.6.2.1. Recommended Components

- Capacitors
 - C1: 220nF
 - C2, C3, C4: 1µF
- Inductor
 - L1: 10µH
- RS-232 Transceivers
 - U1: LINEAR TECHNOLOGY LTC[®]2804IGN
 - J1: SUB-D9 female

The LTC2804 may be powered either by VCC_1V8 (pin 5) of the AirPrime Q2698 embedded module or by an external regulator at 1.8 volts.

The UART2 interface may be connected directly to other components, if the voltage interface is 1.8V.

4.6.3. 4-wire Serial Interface

The signals used in this interface are:

- CT103-TXD2
- CT104-RXD2
- ~CT105-RTS2
- ~CT106-CTS2

Other signals and their multiplexed GPIOs are not available.

Please refer to the technical appendixes of document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information.

4.6.4. 2-wire Serial Interface

Caution: *This case is possible for a connected external chip, but not recommended (and forbidden for AT command or modem use).*

The flow control mechanism has to be managed at the customer side. The signals used in this interface are:

- CT103-TXD2
- CT104-RXD2

Signals \sim CT105-RTS2 and \sim CT106-CTS2 are not used; default hardware flow control on UART1 should be de-activated using AT command **AT+IFC=0,0**. Refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information.

The signal \sim CT105-RTS2 must be configured at low level.

Other signals and their multiplexed GPIOs are not available.

Please refer to the technical appendixes of document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information.

4.7. USIM/SIM Interface

The Universal Subscriber Identification Module (USIM) may be directly connected to the AirPrime Q2698 embedded module via this dedicated interface. Using the USIM is recommended over the SIM card. This interface controls either a 1V8 or 3V USIM.

The five signals used by this interface are:

- SIM-VCC: USIM power supply
- \sim SIM-RST: reset
- SIM-CLK: clock
- SIM-IO: I/O port
- SIMPRES: USIM card detect

4.7.1. Pin Description

Refer to the following table for the pin description of the USIM interface.

Table 19. USIM Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
SIM-CLK	14	O	2V9 / 1V8	0	USIM Clock	Not mux
\sim SIM-RST	13	O	2V9 / 1V8	0	USIM Reset	Not mux
SIM-IO	11	I/O	2V9 / 1V8	Pull-up*	USIM Data	Not mux
SIM-VCC	9	O	2V9 / 1V8		USIM Power Supply	Not mux
SIMPRES	12	I	1V8	Z	USIM Card Detect	GPIO18

* USIM-IO pull-up is about 10k Ω

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

4.7.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the USIM interface.

Table 20. Electrical Characteristics of the USIM Interface

Parameter	Condition	Minimum	Typical	Maximum	Unit
SIM-IO V _{IH}	I _{IH} = ± 20µA	0.7xSIMVCC			V
SIM-IO V _{IL}	I _{IL} = 1mA			0.4	V
~SIM-RST, SIM-CLK V _{OH}	Source current = 20µA	0.9xSIMVCC			V
SIM-IO V _{OH}	Source current = 20µA	0.8xSIMVCC			V
~SIM-RST, SIM-IO, SIM-CLK V _{OL}	Sink current = -200µA			0.4	V
SIM-VCC Output Voltage	SIMVCC = 2.9V IVCC= 1mA	2.84	2.9	2.96	V
	SIMVCC = 1.8V IVCC= 1mA	1.74	1.8	1.86	V
SIM-VCC current	VBATT = 3.8V			10	mA
SIM-CLK Rise/Fall Time	Loaded with 30pF		20		ns
~SIM-RST, Rise/Fall Time	Loaded with 30pF		20		ns
SIM-IO Rise/Fall Time	Loaded with 30pF		0.7	1	µs
SIM-CLK Frequency	Loaded with 30pF			3.9	MHz

Note: When **SIMPRES** is used, a **low to high** transition means that the USIM card is inserted and a **high to low** transition means that the USIM card is removed.

4.7.3. Application

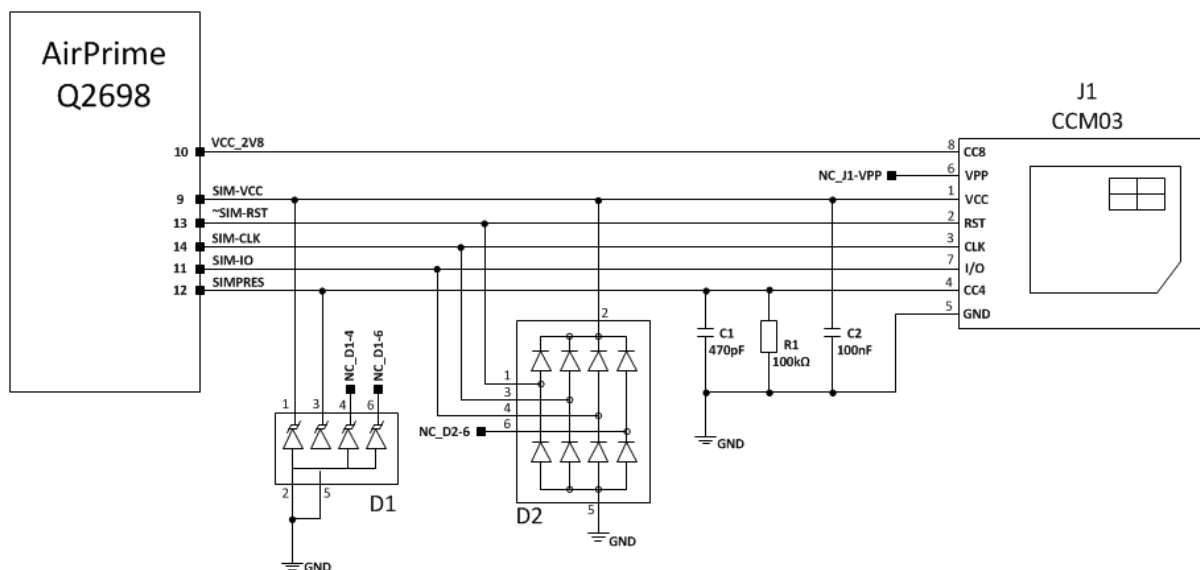


Figure 14. Example of a Typical SIM Socket Implementation

4.7.3.1. Recommended Components

- R1: 100 k Ω
- C1: 470 pF
- C2: 100 nF
- D1: ESDA6V1SC6 from ST
- D2: DALC208SC6 from SGS-THOMSON
- J1: ITT CANNON CCM03 series

The capacitor (C2) placed on the SIM-VCC line must not exceed 330nF.

4.7.3.2. SIM Socket Pin Description

The following table lists the SIM socket pin description.

Table 21. SIM Socket Pin Description

Signal	Pin Number	Description
VCC	1	SIM-VCC
RST	2	~SIM-RST
CLK	3	SIM-CLK
CC4	4	SIMPRES with 100 k Ω pull-down resistor
GND	5	GROUND
VPP	6	Not connected
I/O	7	SIM-IO
CC8	8	VCC_1V8 of the embedded module (pin 5)

4.8. USB 2.0 Interface

A 4-wire USB slave interface is available which complies with USB 2.0 protocol signaling and is 3.3V typ compatible.

Note: A 5V to 3.3V typ voltage regulator is needed between the external interface power-in line (+5V) and the embedded module line (VPAD-USB).

The signals used by the USB interface are:

- VPAD-USB
- USB-DP
- USB-DM
- GND

The USB interface features are:

- 480Mbit/s high-speed transfer rate
- USB Softconnect feature
- CDC 1.1 – ACM compliant

4.8.1. Pin Description

Refer to the following table for the pin description of the USB interface.

Table 22. USB Pin Description

Signal	Pin #	I/O	I/O Type	Description
VPAD-USB	52	I	VPAD_USB	USB Power Supply
USB-DP	54	I/O	VPAD_USB	Differential data interface positive
USB-DM	56	I/O	VPAD_USB	Differential data interface negative

4.8.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the USB interface.

Table 23. Electrical Characteristics of the USB Interface

Signal Name	Description	Input/Output	Voltage (V)		
			Minimum	Typical	Maximum
USB-DP	USB data positive (Low / Full speed)	Input High	2.00	3.30	3.60
		Input Low	0		0.80
		Output High	2.80	3.30	3.60
		Output Low			0.30
	USB data positive (High speed)	Input High	0.30		0.44
		Input Low	0		0.01
		Output High	0.36	0.38	0.44
		Output Low	0		0.01
USB-DM	USB data negative (Low / Full speed)	Input High	2.00	3.30	3.60
		Input Low	0		0.80
		Output High	2.80	3.30	3.60
		Output Low			0.30
	USB data negative (High speed)	Input High	0.30		0.44
		Input Low	0		0.01
		Output High	0.36	0.38	0.44
		Output Low	0		0.01

4.8.3. Application

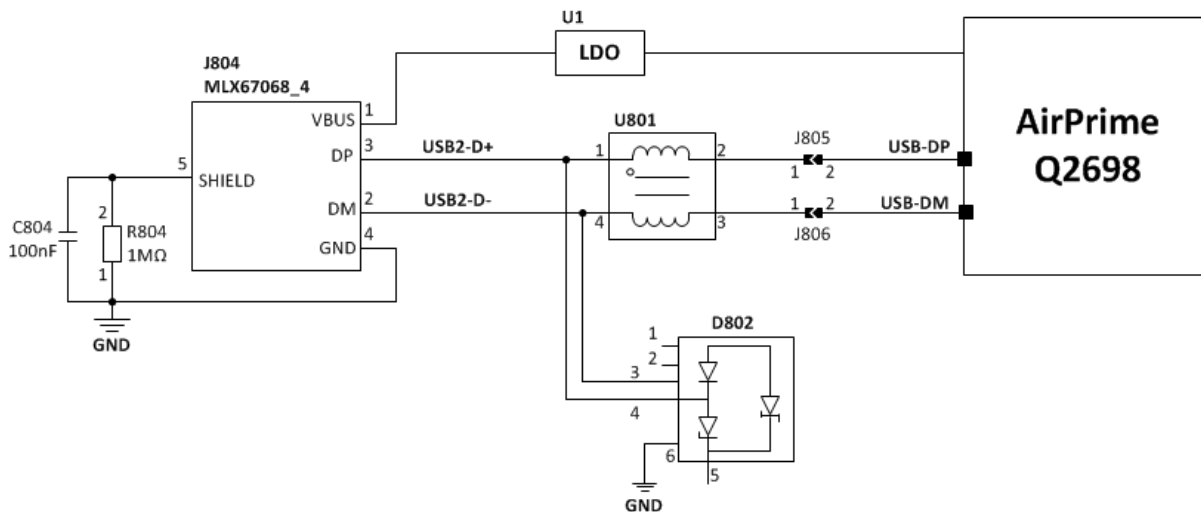


Figure 15. Example of a USB Implementation

The regulator used is a 3.3V regulator and it is supplied via J1 when the USB wire is plugged.

D1 is the EMI/RFI filter with ESD protection. The internal pull-up resistor of D1 which is used to detect the interface's full speed is not connected because the AirPrime Q2698 has a pull-up resistor embedded within, with the same function, which is to detect the speed.

Note that both R1 and C1 must be close to J1.

4.8.3.1. Recommended Components

- R1: 1MΩ
- C1, C3: 100nF
- C2, C4: 2.2μF
- U801: DLP0NSN900HL2L from MURATA
- D802: RCLAMP0503N from SEMTECH
- U1: LP2985AIM 3.3V from NATIONAL SEMICONDUCTOR

4.9. RF Interface

The AirPrime Q2698 embedded module supports three antennas (main, diversity and GPS). The RF interface has a 50 Ω nominal impedance and a high DC impedance.

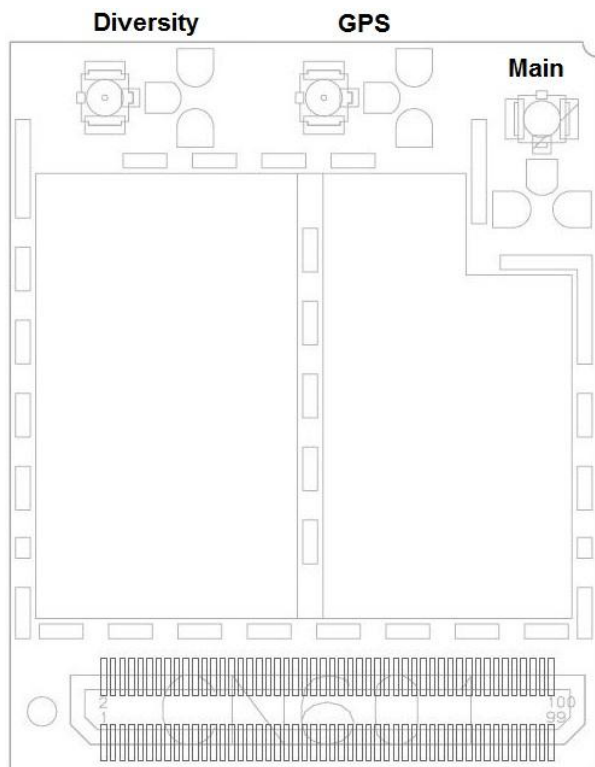


Figure 16. RF Interfaces on the AirPrime Q2698

4.9.1. RF Connections

The AirPrime Q2698 embedded module does not support an antenna switch for a car kit, but this function can be implemented externally and can be driven using a GPIO.

The antenna cable and connector should be selected in order to minimize loss in the frequency bands used for GSM 850/900MHz and 1800/1900MHz. The maximum value of loss considered between the embedded module and an external connector is 0.5dB.

4.9.1.1. U.FL Connector

The U.FL connector can be used for the main, diversity and GPS antennas.

A wide variety of cables fitted with U.FL connectors is offered by different suppliers. For more information, refer to section 10.6 RF Antenna.

4.9.1.2. Soldered Solution

The soldered solution can be used for the main, diversity and GPS antennas.

The soldered solution will preferably be based on an RG178 coaxial cable. For more information, refer to section 10.6 RF Antenna.

4.9.1.3. Precidip Solution

The precidip solution can be used for the main, diversity and GPS antennas.

For more information, refer to section 10.6 RF Antenna.

4.9.2. RF Performance

The RF performance is compliant with the ETSI GSM 05.05 recommendations.

The main receiver parameters are:

- GSM850 Reference Sensitivity = -109 dBm typical (Static & TUHigh)
- E-GSM900 Reference Sensitivity = -109 dBm typical (Static & TUHigh)
- DCS1800 Reference Sensitivity = -108 dBm typical (Static & TUHigh)
- PCS1900 Reference Sensitivity = -107 dBm typical (Static & TUHigh)
- 3G Band I 2100 Reference Sensitivity = -108 dBm typical (Static & TUHigh)
- 3G Band II 1900 Reference Sensitivity = -107 dBm typical (Static & TUHigh)
- 3G Band V 850 Reference Sensitivity = -110 dBm typical (Static & TUHigh)
- 3G Band VI 800 Reference Sensitivity = -110 dBm typical (Static & TUHigh)
- 3G Band VIII 900 Reference Sensitivity = -108 dBm typical (Static & TUHigh)
- Selectivity @ 200 kHz: > +9 dBc
- Selectivity @ 400 kHz: > +41 dBc
- Linear dynamic range: 63 dB
- Co-channel rejection: >= 9 dBc

The main transmitter parameters are:

- Maximum output power (EGSM900 & GSM850): 32.5 dBm +/- 2 dB at ambient temperature
- Maximum output power (GSM1800 & PCS1900): 29.5 dBm +/- 2 dB at ambient temperature
- Minimum output power (EGSM900 & GSM850): 5 dBm +/- 5 dB at ambient temperature
- Minimum output power (GSM1800 & PCS1900): 0 dBm +/- 5 dB at ambient temperature
- Maximum output power (3G all band): 23 dBm +1/-3 dB at ambient temperature

4.9.3. Antenna Specifications

The antenna must meet the requirements specified below.

The optimum operating frequency depends on the application. Either a dual-band or quad-band antenna will operate in these frequency bands and have the following characteristics.

Table 24. Antenna Specifications

Characteristics	GSM850 and WCDMA Band V	WCDMA Band VI	EGSM 900 and WCDMA Band VIII	DCS 1800	PCS 1900 and WCDMA Band II	WCDMA Band I
TX Frequency	824 to 849 MHz	830 to 840 MHz	880 to 915 MHz	1710 to 1785 MHz	1850 to 1910 MHz	1920 to 1980 MHz
RX Frequency	869 to 894 MHz	875 to 885 MHz	925 to 960 MHz	1805 to 1880 MHz	1930 to 1990 MHz	2110 to 2170 MHz
Impedance	50 Ω					
VSWR	Rx max	1.5:1				
	Tx max	1.5:1				
Typical radiated gain	0dBi in one direction at least					

4.9.4. GPS Specifications

Note: These specifications are preliminary targets that are subject to change without notice. Actual GPS functionality depends on the firmware version and module configuration.

The module provides the GPS features listed in the following sub-sections.

4.9.4.1. Standalone GPS

- Leading standalone/autonomous GPS performance
- -145 dBm cold start sensitivity
- -153 dBm hot start sensitivity
- -155 dBm tracking sensitivity
- < 45 second average cold start TTFF (Time To First Fix) in open air
- < 3 second average super hot TTFF in open sky
- < 10 m accuracy in open sky

Note: For optimum performance, the modem should be registered on the GSM/UMTS network, but does not need to be on an active data or voice call.

4.9.4.2. gpsOneXTRA™

- Enables enhanced standalone GPS operation by downloading < 40 kB file from a server on the Internet
- Performance closer to UE-based operation than traditional standalone GPS operation
- Best if downloaded once every 1–2 days, but valid for up to 7 days with some accuracy degradation

4.9.4.3. A-GPS Features

- Leading A-GPS performance
Exceeds 3GPP RAN 4 AGPS performance specification
- -153 dBm cold start sensitivity
- -155 dBm tracking sensitivity
- < 5 second average cold start TTFF in open sky (UE-based)
- < 3 second average super hot TTFF in open sky
- < 2 m accuracy in open sky 1 Hz tracking with CEP-50
- UMTS Control Plane (CP) – UE-assisted and UE-based
- GSM Control Plane (CP) – UE-assisted and UE-based

4.9.4.4. Enhanced Navigation 2.0 Feature

- Provides leading performance in car and walking navigation modes as well as accuracy while stationary
- Airline/Game/Offline mode
- GPS capability is available while phone is offline

4.9.4.5. NMEA

Supported sentences: GGA, GSA, GSV, RMC, VTG

4.10. Analog Audio Interface

The AirPrime Q2698 embedded module supports one microphone input and one speaker output. It also includes an echo cancellation feature and a noise reduction feature, which allows for an improved quality of hands-free functionality.

In some cases, ESD protection must be added on the audio interface lines.

4.10.1. Pin Description

Refer to the following table for the pin description of the Analog Audio interface.

Table 25. Analog Audio Pin Description

Signal	Pin #	I/O	I/O Type	Description
MIC1P	40	I	Analog	Microphone 1 positive input
MIC1N	38	I	Analog	Microphone 1 negative input
SPK1P	35	O	Analog	Speaker 1 positive output
SPK1N	37	O	Analog	Speaker 1 negative output

4.10.2. Microphone

The microphone can be connected in either differential or single-ended mode. However, it is strongly recommended to use a differential connection in order to reject common mode noise and TDMA noise. Using a single-ended connection requires a good ground plane, filtering as well as shielding in order to avoid any disturbance on the audio path.

The gain of both MIC inputs is internally adjusted and can be tuned using an AT command.

4.10.2.1. Microphone Inputs

By default, MIC1 are single-ended but can be configured in differential.

MIC1 input does not include an internal bias; it needs to have an external biasing if an electret microphone is used.

AC coupling is already embedded in the AirPrime Q2698 embedded module.

Table 26. Equivalent Circuits of MIC1

DC Equivalent Circuit	AC Equivalent Circuit

4.10.2.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of MIC1.

Table 27. Electrical Characteristics of MIC1

Parameters		Minimum	Typical	Maximum	Unit
DC Characteristics			N/A		V
AC Characteristics 200 Hz < F < 4 kHz	Z1	70	120	160	kΩ
Working voltage (MIC1P-MIC1N)	AT+VGT*=3500 ¹		13.8	18.6**	mVrms
	AT+VGT*=2000 ¹		77.5	104**	
	AT+VGT*=700 ¹		346	465**	
Maximum rating voltage (MIC1P or MIC1N)	Positive			+7.35	V
	Negative	-0.9			

* The input voltage depends of the input micro gain set by AT command. Please refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47.

** This value is obtained with digital gain = 0 and for frequency = 1kHz.

¹ This value is given in dB, but it's possible to toggle to index value. Please refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47.

Caution: *The voltage input value for MIC1 can't exceed the maximum working voltage, otherwise clipping will appear.*

4.10.2.3. Differential Connection Example

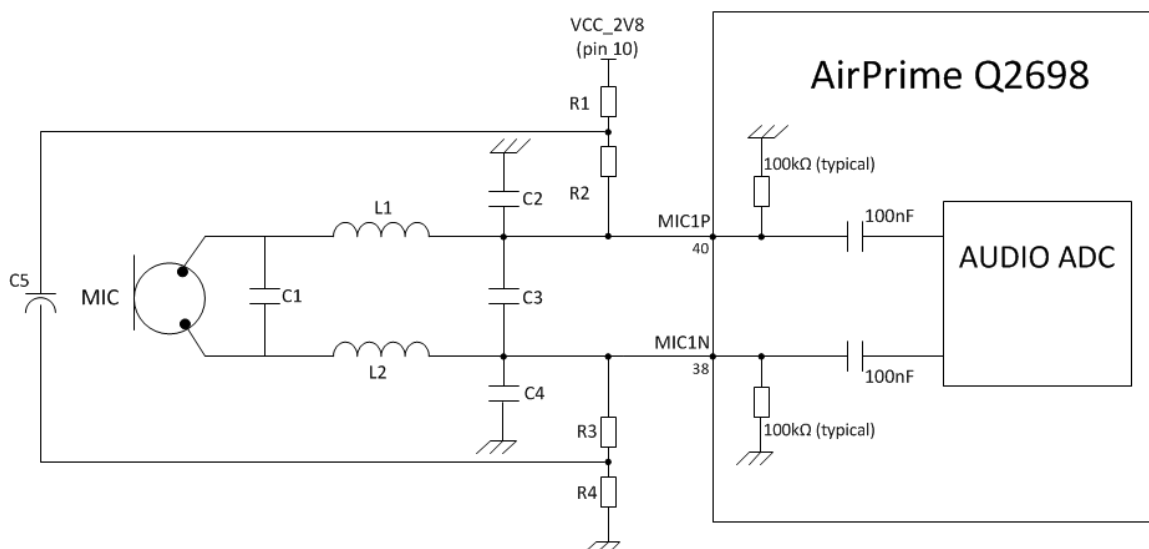


Figure 17. Example of MIC1 Input Differential Connection with LC Filter

The LC filter (L1, L2, C2, C3, and C4) is used to reduce EMI perturbation created by TDMA noise, but it is not mandatory. Good quality audio can be achieved without an LC filter depending on the design.

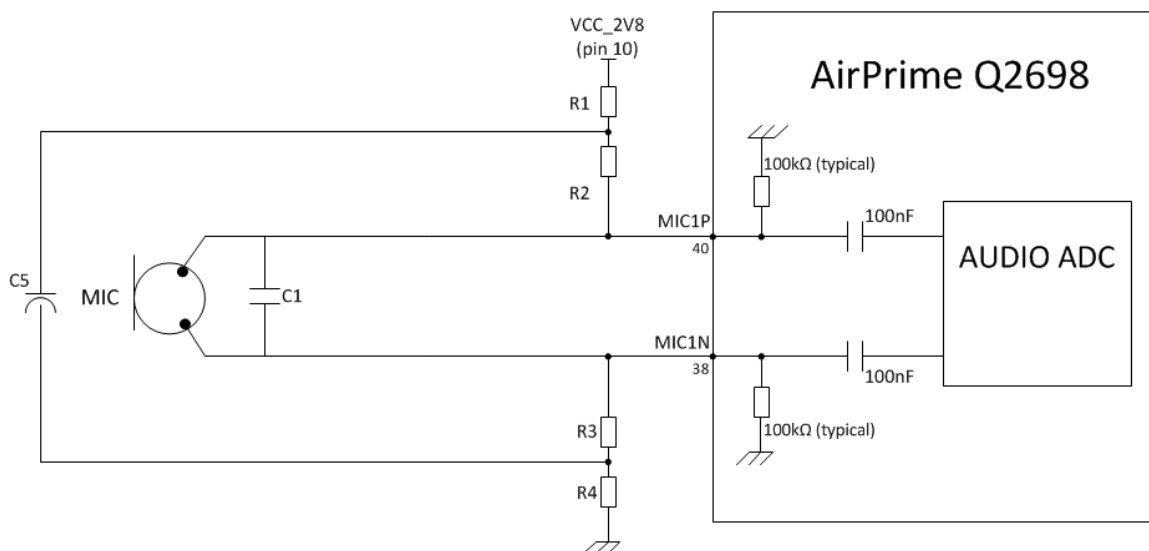


Figure 18. Example of MIC1 Input Differential Connection without LC Filter

Capacitor C1 is highly recommended to eliminate TDMA noise and it must be placed close to the microphone.

Vbias may be VCC_2V8 (pin 10) of the AirPrime Q2698 embedded module, but it is possible to use a different 2 volts to 3 volts supply voltage depending on the microphone characteristics.

Caution: If an external supply is used other than VCC_2V8 (pin 10), it is important to make sure that the voltage is clean and free from noise; otherwise, the audio quality will be degraded.

4.10.2.3.1. Recommended Components

- R1: 4.7kΩ (for Vbias equal to 2.8V)
- R2, R3: 820Ω
- R4: 1Ω
- C1: 12pF to 33pF (needs to be tuned depending on the design)
- C2, C3, C4: 47pF (needs to be tuned depending on the design)
- C5: 2.2μF +/- 10%
- L1, L2: 100nH (needs to be tuned depending on the design)

4.10.2.4. Single-Ended Connection Example

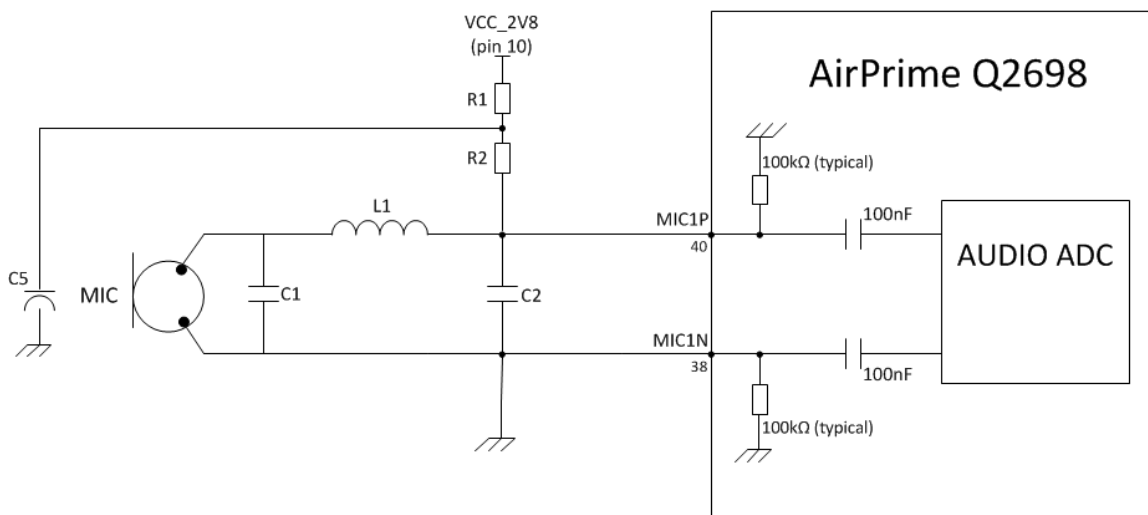


Figure 19. Example of MIC1 Input Single-Ended Connection with LC Filter

The single-ended design is not recommended for improving TDMA noise rejection as it is usually difficult to eliminate TDMA noise from a single-ended design.

The LC filter (L1 and C2) is used to reduce EMI perturbation created by TDMA noise, but it is not mandatory. Good quality audio can be achieved without an LC filter depending on the design.

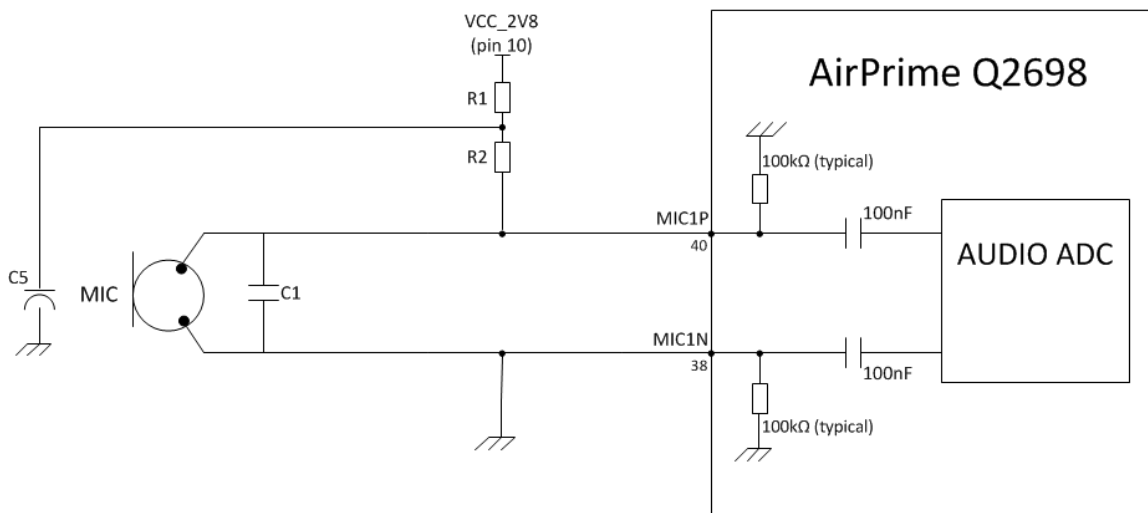


Figure 20. Example of MIC1 Input Single-Ended Connection without LC Filter

Capacitor C1 is highly recommended to eliminate TDMA noise, and must be placed close to the microphone.

Vbias must be very "clean" to avoid bad performance in case of a single-ended implementation. It is highly recommended to use the VCC_2V8 supply which is available on the system connector (pin 10), in order to avoid this problem.

4.10.2.4.1. Recommended Components

- R1: 4.7kΩ (for Vbias equal to 2.8V)
- R2: 820Ω
- C1: 12pF to 33pF (needs to be tuned depending on the design)
- C2: needs to be tuned depending on the design
- L1: needs to be tuned depending on the design

4.10.3. Speaker

One speaker channel, SPK1, connected in single-ended mode, is available on the AirPrime Q2698 embedded module.

Using a single-ended connection requires a good ground plane, filtering as well as shielding in order to avoid any disturbance on the audio path.

The following table lists the typical values for both SPK1.

Table 28. Speaker Information

Parameter	Typical	Unit	Connection
Z (SPK1P, SPK1N)	16 or 32	Ω	Single-ended mode

The maximal specifications given in the following sub-sections are available with the maximum power output configuration values set by an AT command; typical values are recommended.

4.10.3.1. Speaker Outputs

With the SPK1 interface, only a single-ended speaker connection is allowed.

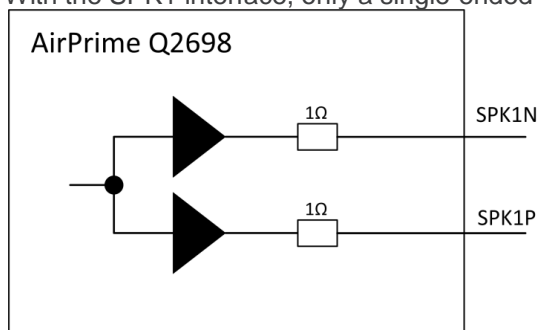


Figure 21. Equivalent Circuits of SPK1

4.10.3.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of SPK1.

Table 29. Electrical Characteristics of SPK1

Parameters		Minimum	Typical	Maximum	Unit	
Biasing voltage	-	-1.5		1.5	mV	
Output swing voltage	RL=16Ω; AT+VGR=-1600**; single-ended	-	1.7	-	Vpp	
	RL=32Ω; AT+VGR=-1600**; single-ended	-	1.9	2.75	Vpp	
RL	Load resistance	14.5	32	-	Ω	
IOUT	Output current; single-ended; peak value	RL=16Ω	-	40	85	mA
		RL=32Ω	-	22	-	mA
POUT	RL=16Ω; AT+VGR*=-1600**	-	25		mW	
	RL=32Ω; AT+VGR*=-1600**	-	16	27	mW	
RPD	Output pull-down resistance at power-down	28	40	52	kΩ	

* The output voltage depends of the output speaker gain set by AT command. Please refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47.

** This value is given in dB, but it's possible to toggle to index value. Please refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47.

4.10.3.3. Single-Ended Connection

A typical implementation of SPK1 is shown below:

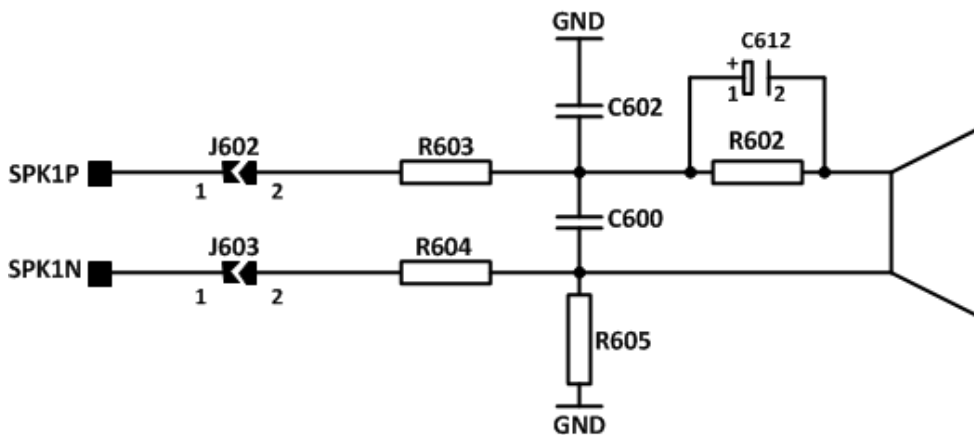


Figure 22. Example of Speaker Single-Ended Connection

Take note of the following when connecting the speaker in single-ended mode:

- J602 and J603 should be shorted
- Do not mount R602 and C602. R605 should also not be mounted; it is suggested to have this position reserved on the PCB
- 0Ω is recommended for R603 and R604
- 33 – 100pF is recommended for C600

When using a 32Ω speaker, a cheaper and smaller solution (where C612 = 4.7μF (ceramic)) should be used.

To reduce noise, SPK1N must be connected to the specific ground pin of the Q2698 embedded module. Also, both SPK1P and SPK1N signals must be connected using parallel lines to pins 35 and 37 (GND pins) of the Q2698 embedded module respectively.

4.10.3.4. Recommended Characteristics

- Type: 10mW, electro-magnetic
- Impedance
 - $Z = 32\Omega$ for headset kit
- Sensitivity: 110 dB SPL minimum (0 dB = 20μPa)
- Frequency response compatible with the GSM specifications

4.11. Digital Audio Interface (PCM)

The digital audio interface (PCM) interface allows connectivity with standard audio peripherals. It can be used, for example, to connect an external audio codec.

The programmability of this interface provides the ability to address a large range of audio peripherals.

The PCM interface consists of 4 wires:

- **PCM-SYNC** (output): The frame synchronization signal delivers an 8kHz frequency pulse that synchronizes the frame data in and the frame data out.
- **PCM-CLK** (output): The frame bit clock signal controls data transfer with the audio peripheral.
- **PCM-OUT** (output): The frame “data out” relies on the selected configuration mode.
- **PCM-IN** (input): The frame “data in” relies on the selected configuration mode.

The PCM interface features are:

- IOM-2 compatible device on physical level
- Master mode with 16 slots for Linear Law, 32 slots for compression Law
- Bit rate single clock mode at 2MHz (short sync mode)
- 16 bits data word MSB first only
- Linear Law and compression Law
- Short Frame Synchronization¹
- Push-pull configuration on PCM-OUT and PCM-IN

Note that the digital audio interface configuration cannot differ from those specified above.

¹ Optional Long Frame Synchronization (clock mode at 128KHz)

4.11.1. Pin Description

Refer to the following table for the pin description of the PCM interface.

Table 30. PCM Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description
PCM-SYNC	77	O	1V8	Z	Frame synchronization 8kHz
PCM-IN	78	I	1V8	Z	Data input
PCM-CLK	79	O	1V8	Z	Data clock
PCM-OUT	80	O	1V8	Z	Data output

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

4.11.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the PCM interface.

Table 31. AC Characteristics of the PCM Interface (refer to QCT datasheet)

Signal	Description	Minimum	Typical	Minimum	Unit
Tsync_low + Tsync_high	PCM-SYNC period		125		μs
Tsyncl	PCM-SYNC low time		124.5		μs
Tsynch	PCM-SYNC high time		0.5		μs
TCLK-cycle	PCM-CLK period		488		ns
Tsusync	PCM-SYNC setup time	60			ns
Thsync	PCM-SYNC hold time	60			ns
Tsudin	PCM-DIN setup time	50			ns
Thdin	PCM-DIN hold time	10			ns
Tpdout - delay	Delay from PCM_CLK rising to PCM_DOUT valid			350	ns
Tzdout -delay	Delay from PCM_CLK falling to PCM_DOUT high-Z		160		ns

4.11.3. PCM Waveforms

PCM_SYNC and the number of slots can be calculated as follows:

Number of slots = frame length/bit width; and

PCM_SYNC = PCM_CLK/frame length

For example:

If PCM_CLK = 2048 kHz and PCM_SYNC = 8 kHz,

Then,

$$\begin{aligned} \text{Frame length} &= \text{PCM_CLK} / \text{PCM_SYNC} \\ &= 2048 \text{ kHz} / 8 \text{ kHz} \\ &= 256 \end{aligned}$$

The number of slots can then be computed as:

- 256/16 = 16 slots for linear format; or
- 256/8 = 32 slots for A/μ law

The following figure shows the PCM timing frame.

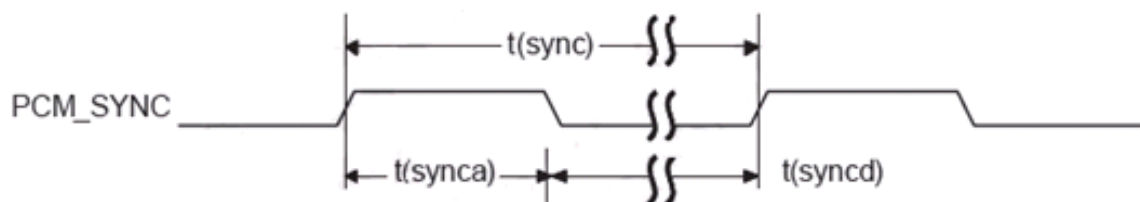


Figure 23. PCM-Sync Timing Frame Waveform

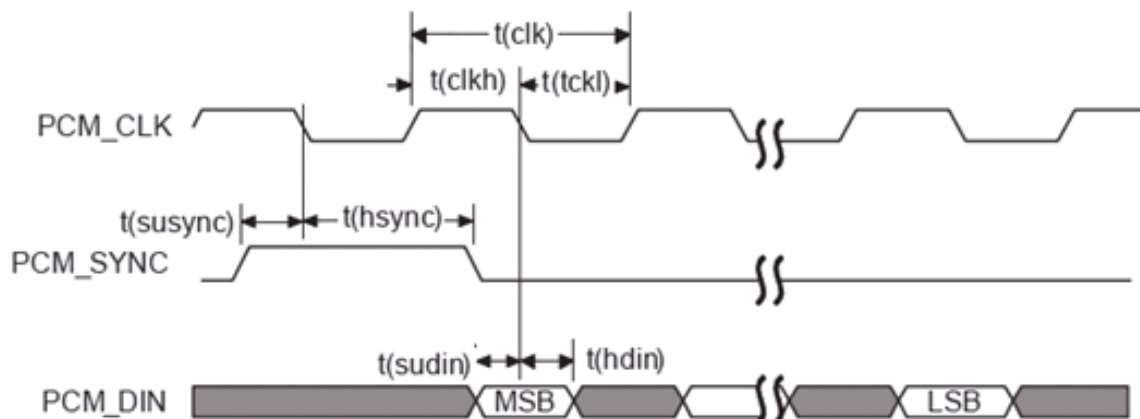


Figure 24. PCM_Codec to MDM Timing

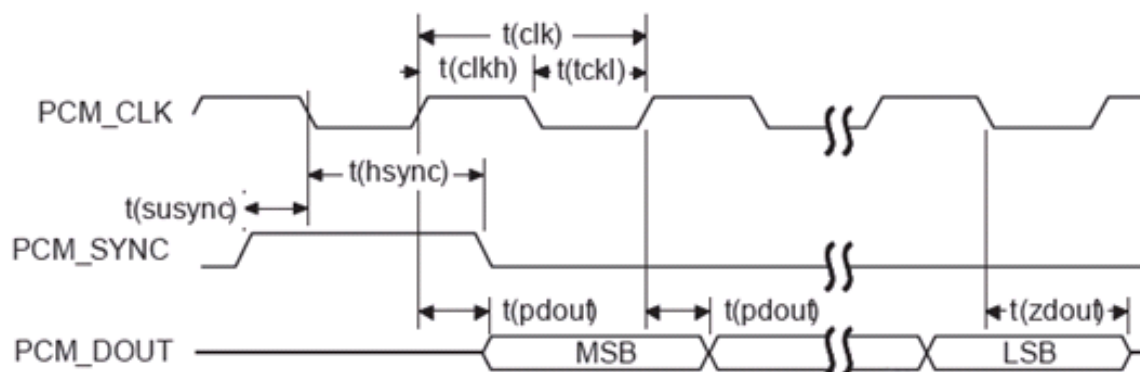


Figure 25. MDM to PCM_Codec Timing

4.12. Analog to Digital Converter

Three Analog to Digital Converter inputs are provided by the AirPrime Q2698 embedded module. The converters are 10-bit resolution ADCs ranging from 0 volt to 4 volts.

4.12.1. Pin Description

Refer to the following table for the pin description of the ADC.

Table 32. ADC Pin Description

Signal	Pin #	I/O	I/O Type	Description
ADC1	20	I	Analog	A/D converter
ADC2	21	I	Analog	A/D converter
ADC3	42	I	Analog	A/D converter

4.12.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the ADC.

Table 33. Electrical Characteristics of the ADC

Parameter	Minimum	Typical	Maximum	Unit
Maximum output code		TBC		LSB
Sampling period	0,5		3*	s
Input signal range	0		4	V
Input impedance	ADC1	1M		Ω
	ADC2	1M		
	ADC3	1M		

* Sampling rate only for ADC2 and the Open AT Application Framework application.



5. Signals and Indicators

5.1. ON/~OFF Signal

This input is used to switch the AirPrime Q2698 embedded module ON or OFF.

A high-level signal must be provided on the ON/~OFF pin to switch the embedded module ON. The voltage of this signal has to be maintained higher than $0.8 \times V_{BATT}$ for a minimum of 1500ms. This signal can be left at high level until switched off.

To switch the embedded module OFF, the ON/OFF pin must be released. The embedded module can be switched off via the operating system.

5.1.1. Pin Description

Refer to the following table for the pin description of the ON/~OFF signal.

Table 34. On/~OFF Signal Pin Description

Signal	Pin #	I/O	I/O Type	Description
ON/~OFF	19	I	CMOS	Embedded module Power-ON

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

5.1.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the ON/~OFF signal.

Table 35. Electrical Characteristics of the ON/~OFF Signal

Parameter	I/O Type	Minimum	Minimum	Unit
V_{IL}	CMOS		$V_{BATT} \times 0.2$	V
V_{IH}	CMOS	$V_{BATT} \times 0.8$	V_{BATT}	V

Caution: *All external signals must be inactive when the embedded module is OFF to avoid any damage when starting and to allow the embedded module to start and stop correctly.*

5.1.3. Power-ON

Once the embedded module is supplied with power via V_{BATT} , the application must set the ON/~OFF signal to high to start the embedded module power-ON sequence. The ON/~OFF signal must be held high for a minimum delay of $T_{on/off-hold}$ (minimum hold delay on the ON/~OFF signal) to power-ON. After this delay, an internal mechanism maintains the embedded module in power-ON condition.

During the power-ON sequence, an internal reset is automatically performed by the embedded module for 40ms (typical). Any external reset should be avoided during this phase.

Once initialization is completed (timing is USIM and network dependent), the AT interface answers "OK" to the application. For further details, please refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47.

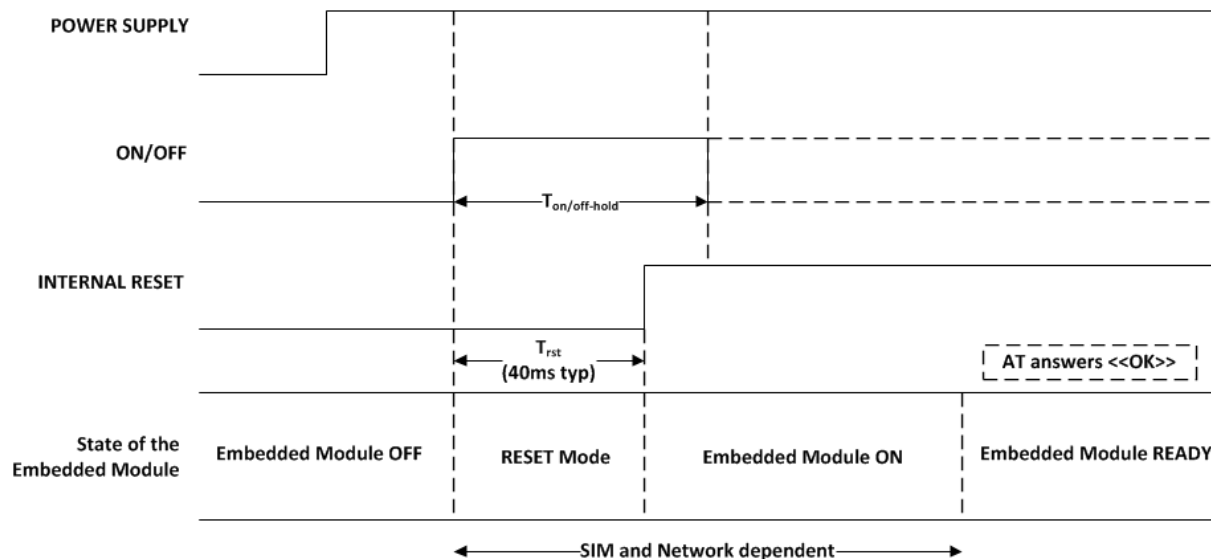


Figure 26. Power-ON Sequence (no PIN code activated)

The duration of the firmware power-ON sequence depends on the need to perform a recovery sequence if the power has been lost during a flash memory modification.

Listed below are other factors that have a minor influence on the power-ON sequence.

- the number of parameters stored in the flash memory by the AT commands received so far
- the ageing of the hardware components, especially the flash memory
- the temperature conditions

The *recommended* way to de-assert the ON/~OFF signal is to use either an AT command or WIND indicators: the application must detect the end of the power-up initialization and de-assert ON/~OFF afterwards.

To release the ON/~OFF signal, either:

- Send an "AT" command and wait for the "OK" answer: once the initialization is complete the AT interface answers « OK » to "AT" message².
- or
- Wait for the "+WIND: 3" message: after initialization, the embedded module, if configured to do so, will return an unsolicited "+WIND: 3" message. The generation of this message is enabled or disabled via an AT command.

Note: Refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information on these commands.

Proceeding thus, by software detection, will always prevent the application from de-asserting the ON/~OFF signal too early.

If WIND indicators are disabled or AT commands unavailable or not used, it is still possible to de-assert ON/~OFF after a delay long enough ($T_{on/off-hold}$) to ensure that the firmware has already completed its power-up initialization.

² If the application manages hardware flow control, the AT command can be sent during the initialization phase.

The table below gives the minimum values of $T_{on/off\text{-hold}}$:

Table 36. $T_{on/off\text{-hold}}$ Minimum Values

Open AT Application Framework	$T_{on/off\text{-hold}}$ Safe Evaluations of the Firmware Power-Up Time
Open AT Application Framework (version TBD)	8s

The figure above takes the worst cases into account: power-loss recovery operations, slow flash memory operations in high temperature conditions, and so on; but it's a safe figure, large enough to ensure that ON/~OFF is not de-asserted too early.

On the other hand, typical power-up initialization time figures for best case conditions (no power-loss recovery, fast and new flash memory) at approximately 3.5 seconds in every firmware version. Releasing ON/~OFF after this delay does not guarantee that the application will actually start-up if, for example, the power plug has been pulled off during a flash memory operation, like a phone book entry update or an AT&W command.

The ON/~OFF signal can be left at a high level until switched OFF. But this is not recommended as it will prevent the **AT+CPOF** command from performing a clean power-off. (Refer to the note in section 5.1.4 Power-OFF for an alternate usage.)

It not recommended letting this signal high when using a battery as a power source.

If the battery voltage is too low and the ON/~OFF signal is at low level, an internal mechanism switches the embedded module OFF. This automatic process prevents the battery from being over discharged and optimizes its life span.

During the power-ON sequence, an internal reset is automatically performed by the embedded module for 40 ms (typical). Any external reset should be avoided during this phase.

5.1.4. Power-OFF

To correctly power-OFF the embedded module, the application must reset the ON/~OFF signal and then send the **AT+CPOF** command to deregister from the network and switch the embedded module off.

Once the "OK" response is issued by the embedded module, the power supply can be switched off.

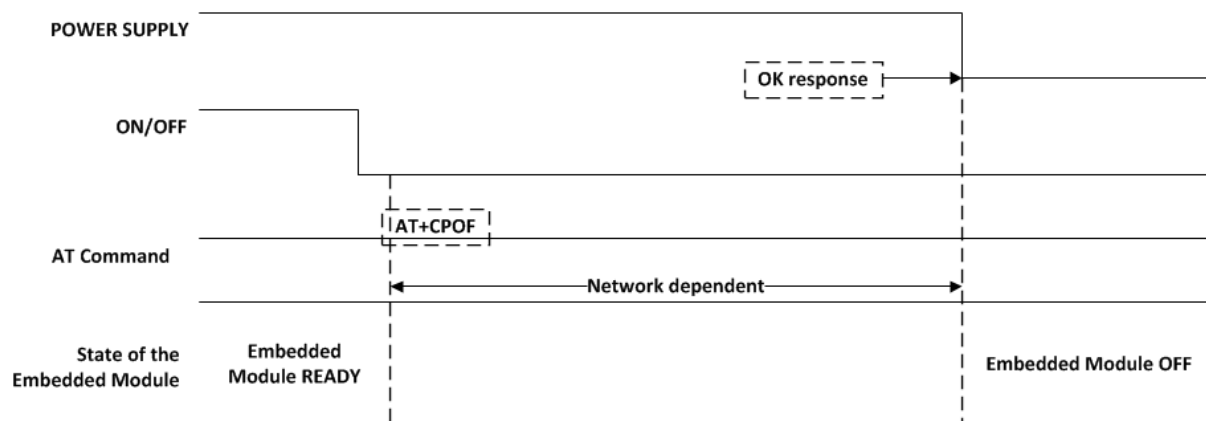


Figure 27. Power-OFF Sequence

Note: If the ON/~OFF pin is maintained at ON (High Level), then the embedded module can't be switched OFF. Connecting a charger on the embedded module has exactly the same effect as setting the ON/~OFF signal. Specifically, the embedded module will not POWER-OFF after the **AT+CPOF** command, unless the charger is disconnected.

5.2. VCC_2V8 and VCC_1V8 Output

These digital power supplies are mainly used to:

- Pull-up signals such as I/Os
- Supply the digital transistors driving the LEDs
- Supply the SIMPRES signal
- Act as a voltage reference for the ADC interface ADC1 (only for VCC_2V8)

Each power supply output has a maximum current of 15mA.

Both outputs are only available when the embedded module is ON.

5.2.1. Pin Description

Refer to the following table for the pin description of the VCC_2V8 and VCC_1V8 outputs.

Table 37. VCC_2V8 and VCC_1V8 Output Pin Description

Signal	Pin #	I/O	I/O Type	Description
VCC_2V8	10	O	Supply	Digital supply
VCC_1V8	5	O	Supply	Digital supply

5.2.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the VCC_2V8 and VCC_1V8 outputs.

Table 38. Electrical Characteristics of the VCC_2V8 and VCC_1V8 Output

Parameter		Minimum	Typical	Maximum	Unit
VCC_2V8	Output voltage	2.74	2.8	2.86	V
	Output Current			15	mA
VCC_1V8	Output voltage	1.76	1.8	1.94	V
	Output Current			15	mA

5.3. Reset Signal (~RESET)

This signal is used to force a reset procedure by providing low level for at least 200 μ s. This signal must be considered as an emergency reset only. A reset procedure is already driven by the internal hardware during the power-ON sequence.

This signal may also be used to provide a reset to an external device (at power-ON only). If no external reset is necessary, this input may be left open. If used (emergency reset), it must be driven by an open collector or an open drain.

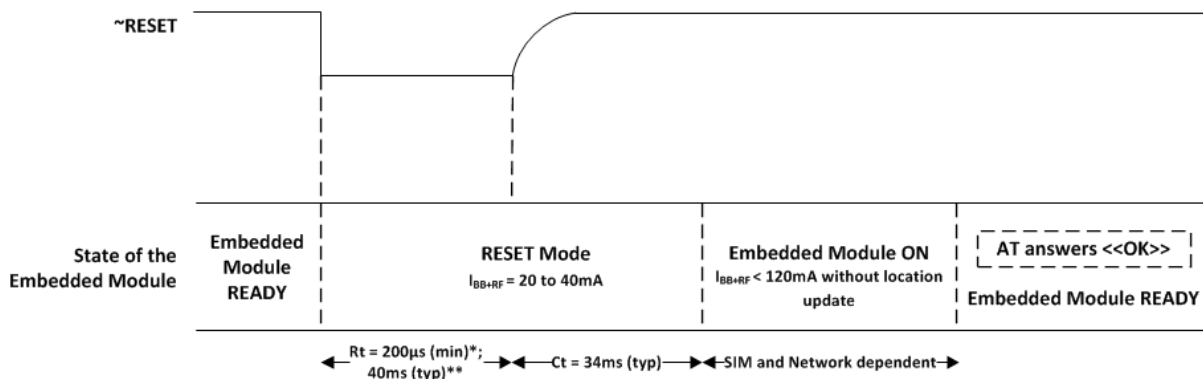
The embedded module remains in reset mode as long as the ~RESET signal is held low.

An operating system reset is to be preferred to a hardware reset.

Caution: *This signal should only be used for "emergency" resets.*

5.3.1. Reset Sequence

To activate the "emergency" reset sequence, the ~RESET signal must be set to low for a minimum of 200µs. As soon as the reset is completed, the AT interface answers "OK" to the application.



* This reset time is the minimum time to be carried out on the ~RESET signal when the power supply is already stabilized.
 ** This reset time is internally carried out by the embedded module power supply supervisor only when the embedded module power supplies are powered ON.

Figure 28. Reset Sequence Waveform

At power-up, the ~RESET time (Rt) is carried out after switching the embedded module ON. It is generated by the internal embedded module voltage supervisor.

The ~RESET time is provided by the internal RC component. To keep the same time, it is not recommended to connect another R or C component on the ~RESET signal. Only a switch or an open drain gate is recommended.

Ct is the cancellation time required for the AirPrime Q2698 embedded module initialization. Ct is automatically carried out by the embedded module after hardware reset.

5.3.2. Pin Description

Refer to the following table for the pin description of the reset signal.

Table 39. RESET Signal Pin Description

Signal	Pin #	I/O	I/O Type	Description
~RESET	18	I/O Open Drain	1V8	Embedded module Reset

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

5.3.3. Electrical Characteristics

Refer to the following table for the electrical characteristics of the reset signal.

Table 40. Electrical Characteristics of the ~RESET Signal

Parameter	Minimum	Typical	Maximum	Unit
Input Impedance (R)*		100		kΩ
Input Impedance (C)		10		nF

Parameter	Minimum	Typical	Maximum	Unit
~RESET time (Rt) ¹	200			μs
~RESET time (Rt) ² at power up only	20	40	100	ms
Cancellation time (Ct)		34		ms
V _H **	0.57			V
V _{IL}	0		0.57	V
V _{IH}	1.33			V

* Internal pull-up

** V_H: Hysteresis Voltage

1 This reset time is the minimum time to be carried out on the ~RESET signal when the power supply is already stabilized.

2 This reset time is internally carried out by the embedded module power supply supervisor only when the embedded module power supplies are powered ON.

5.3.4. Application

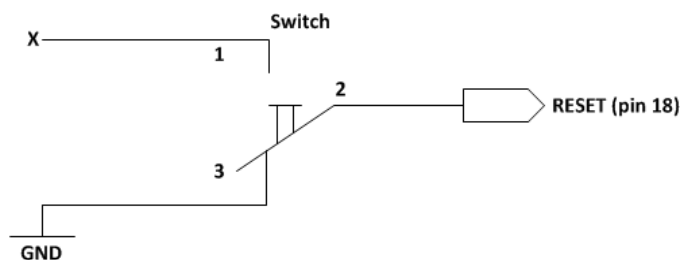


Figure 29. Example of ~RESET Pin Connection with Switch Configuration

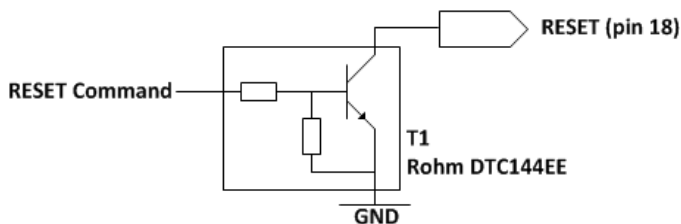


Figure 30. Example of ~RESET Pin Connection with Transistor Configuration

An open collector or open drain transistor may be used. If an open collector is selected, T1 may be a Rohm DTC144EE.

Refer to the following table for reset signal settings.

Table 41. Reset Command

Reset Command	~RESET (pin 18)	Operating Mode
1	0	Reset activated
0	1	Reset inactive

5.4. BAT-RTC (Backup Battery)

The AirPrime Q2698 embedded module provides an input/output to connect a Real Time Clock (RTC) power supply.

This pin is used as a back-up power supply for the internal Real Time Clock. The RTC is supported by the embedded module when VBATT is available, but a back-up power supply is needed to save date and time when VBATT is switched off (VBATT = 0V).

The back-up power supply can be provided by any of the following:

- A super capacitor
- A non-rechargeable battery
- A rechargeable battery

5.4.1. Pin Description

Refer to the following table for the pin description of BAT-RTC.

Table 42. BAT-RTC Pin Description

Signal	Pin #	I/O	I/O Type	Description
BAT-RTC	7	I/O	Supply	RTC Back-up supply

5.4.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of BAT-RTC.

Table 43. Electrical Characteristics of BAT-RTC

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	1.85		3.0	V
Input current consumption*		3.3		μA
Output voltage		2.45		V
Output current			2	mA

* Provided by an RTC back-up battery when the embedded module power supply is OFF (VBATT = 0V).

5.4.3. Application

5.4.3.1. Super Capacitor

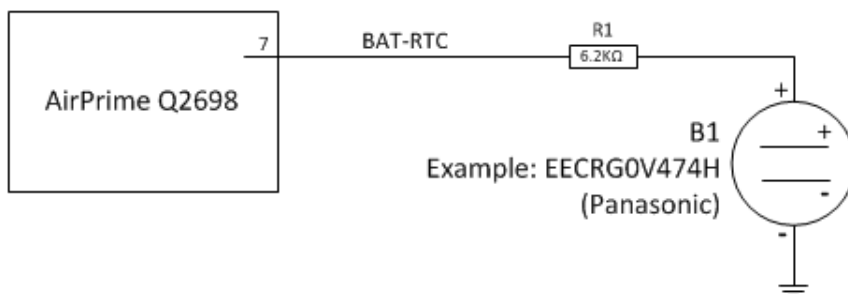


Figure 31. RTC Supplied by a Gold Capacitor

The typical discharge time with a 0.47 Farad gold capacitor is 25 hours for 3μA.

Note: The gold capacitor maximum voltage is 2.5 V.

5.4.3.2. Non-Rechargeable Battery

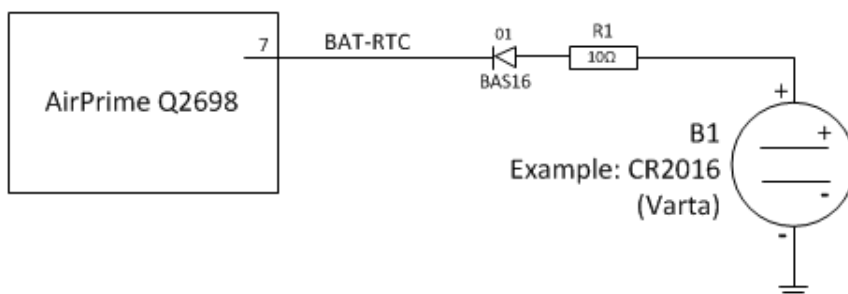


Figure 32. RTC Supplied by a Non-Rechargeable Battery

Diode D1 is mandatory in order to protect the non-rechargeable battery from becoming damaged.

The typical discharge time with an 85 mAh battery is 800 hours (minimum).

5.4.3.3. Rechargeable Battery

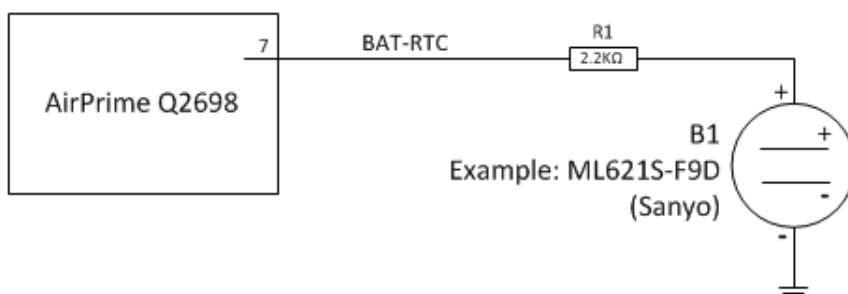


Figure 33. RTC Supplied by a Rechargeable Battery Cell

The typical discharge with a 2 mAh rechargeable battery is approximately 15 hours.

Caution: Before battery cell assembly, ensure that the cell voltage is lower than 2.75 V to avoid damaging the embedded module.

5.5. Buzzer Output

This output is controlled by a pulse width modulation controller and is an open drain output.

This signal may only be used in the implementation of a buzzer. The buzzer can be directly connected between this output and VBATT. The maximum current is 100mA (PEAK).

5.5.1. Pin Description

Refer to the following table for the pin description of the Buzzer output.

Table 44. Buzzer Output Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description
BUZZER0	15	O	Open drain	Z	Buzzer output

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

5.5.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the Buzzer output.

Table 45. Electrical Characteristics of the Buzzer Output

Parameter	Condition	Minimum	Minimum	Unit
$V_{OL\ on}$	$I_{ol} = 100mA$		0.4	V
I_{PEAK}	$VBATT = VBATT_{max}$		100	mA
Frequency		1	50000	Hz

5.5.3. Application

The maximum peak current of the Buzzer output is 100mA and the maximum average current is 40mA. A diode against transient peak voltage must be added as shown in the figure below.

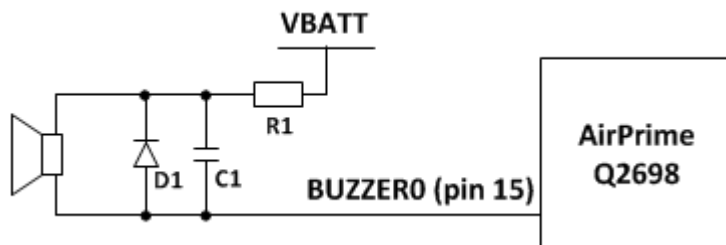


Figure 34. Example of a Buzzer Implementation

Where:

- R1 must be selected in order to limit the current at $I_{PEAK\ max}$
- C1 = 0 to 100nF (depends on the buzzer type)
- D1 = BAS16 (for example)

The BUZZ-OUT output may also be used to drive a LED as shown in the following figure.



Figure 35. Example of LED Driven by the Buzzer Output

The value of R1 depends on the LED (D1) characteristics.

5.5.3.1. Recommended Characteristics

- Electro-magnetic type
- Impedance: 7 to 30Ω
- Sensitivity: 90dB SPL min @ 10cm
- Current: 60 to 90mA

5.6. LED0 Signal

The GSM activity status indication signal, LED0 (pin 17), may be used to drive an LED. This signal is an open-drain digital transistor in accordance to the embedded module activity status. An LED and a resistor can be directly connected between this output and VBATT.

The LED0 state is high during RESET time and undefined during software initialization time. During software initialization time, for a maximum of 2 seconds after RESET cancellation, the LED0 signal is toggling and does not provide the embedded module status. After the 2s period, the LED0 provides the true status of the embedded module.

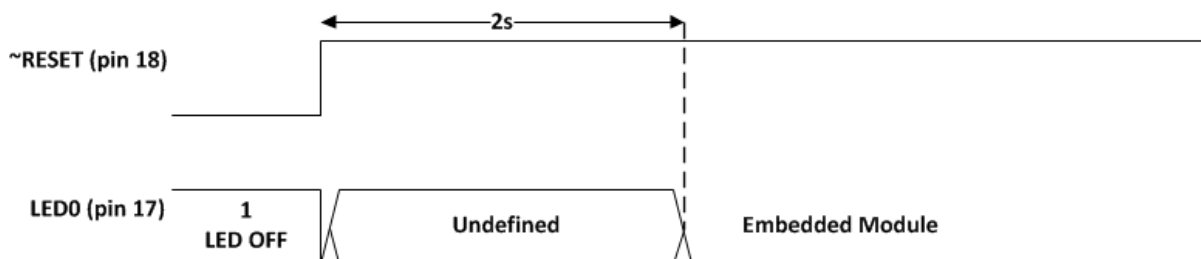


Figure 36. LED0 State During RESET and Initialization Time

When the AirPrime Q2698 embedded module is ON, this output is used to indicate network status.

Table 46. LED0 Status

Embedded Module State	VBATT Status	LED0 Status	Embedded Module Status
Embedded Module OFF	VBATT < 2.8V	OFF	Embedded Module is OFF

Embedded Module State	VBATT Status	LED0 Status	Embedded Module Status
Embedded Module ON	VBATT > 3.2V	Permanent	Embedded Module switched ON, not registered on the network
		Slow flash LED ON for 200ms, OFF for 2s	Embedded Module switched ON, registered on the network
		Quick flash LED ON for 200ms, OFF for 600ms	Embedded Module switched ON, registered on the network, communication in progress
		Very quick flash LED ON for 100ms, OFF for 200ms	Embedded Module switched on, software downloaded is either corrupted or non-compatible ("BAD SOFTWARE")

5.6.1. Pin Description

Refer to the following table for the pin description of LED0.

Table 47. LED0 Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description
LED0	17	O	Open Drain Output	1 and Undefined	LED driving

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

5.6.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of LED0.

Table 48. Electrical Characteristics of LED0

Parameter	Condition	Minimum	Typical	Maximum	Unit
V _{OL}				0.4	V
I _{OUT}				8	mA

5.6.3. Application

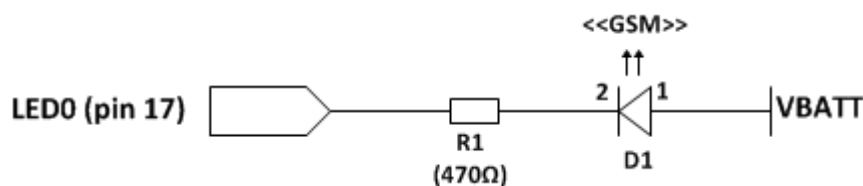


Figure 37. Example of LED0 Implementation

The value of R1 may be harmonized depending on the LED (D1) characteristics.

5.7. TX Burst Indication

The TX_Burst signal is a 1.8V indication signal for TX burst (for GSM only) available in the AirPrime Q2698 embedded module. This signal is available via GPIO_13 (pin 64) and enabled via a specific AT command, **AT+WTBI**.

Table 49. TX_Burst Status

AirPrime Q2698 State	TX_Burst Status
During TX burst	High
No TX	Low

During TX burst, there will be higher current drain from the VBATT power supply which causes a voltage drop. This voltage drop from VBATT is a good indication of a high current drain situation during TX burst.

The TX burst frequency is about 216Hz.

The output logic high duration, $T_{duration}$, depends on the number of TX slots and is computed as follows:

$$T_{duration} = T_{advance} + (0.577ms \times \text{number of TX slots}) + T_{delay}$$

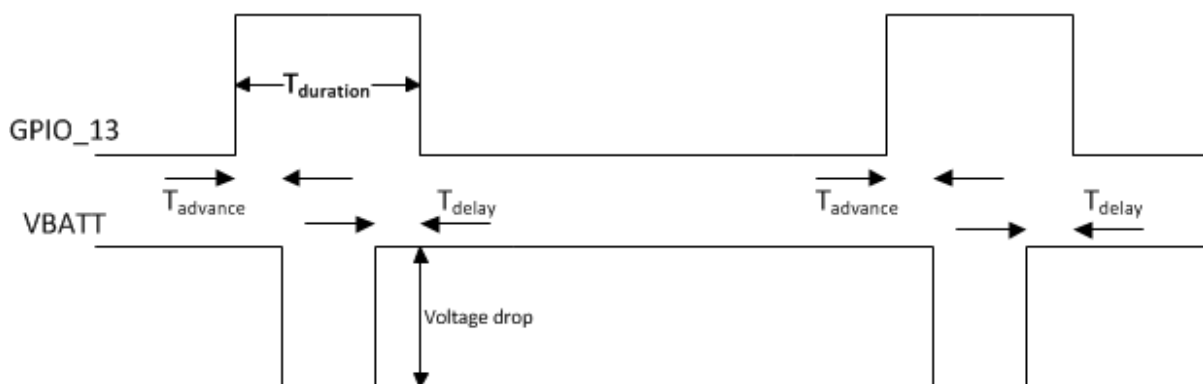


Figure 38. GPIO_13 State During TX Burst

Table 50. TX Burst Indication Signal Electrical Characteristics

Parameter	Minimum	Typ.	Maximum	Unit
V_{OH}	1.25	1.80	1.90	V
V_{OL}	0	-	0.45	V
$T_{advance}$	-	200	-	μ s
T_{delay}	-	40	-	μ s

5.7.1. Application

The TX burst indication signal available via GPIO_13, can be used to drive an LED through a transistor. It will then be a good visual indicator for any TX activity.

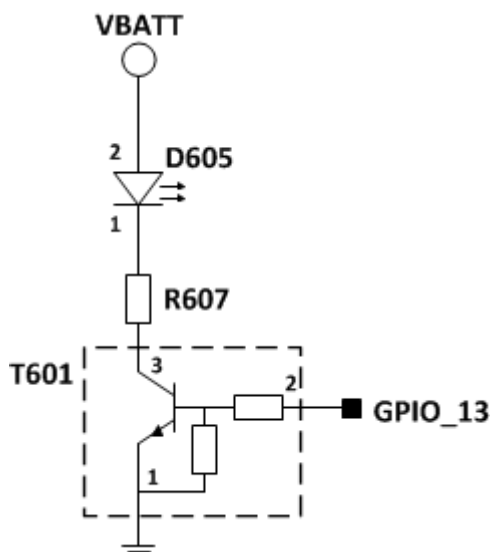


Figure 39. Example of TX Burst Implementation

The value of R607 can be harmonized depending on the LED (D605) characteristics.

5.8. External Interrupt

The AirPrime Q2698 embedded module provides three external interrupt inputs. These interrupt inputs can be activated on the:

- High to low edge
- Low to high edge
- Low to high and high to low edge

When used, the interrupt inputs must not be left open. When not used, they must be configured as GPIOs.

5.8.1. Pin Description

Refer to the following table for the pin description of the External Interrupt.

Table 51. External Interrupt Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
INT0	50	I	1V8	Z	External Interrupt 0	GPIO3
INT1	49	I	2V8	Z	External Interrupt 1	GPIO25
INT2	51	I	1V8	Pull-up	External Interrupt 2	~CS2 / GPIO1

Refer to section 4.2 Electrical Information for Digital I/O for 2V8, 1V8, open drain voltage characteristics; and reset state definition.

5.8.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the External Interrupt.

Table 52. Electrical Characteristics of the External Interrupt

Parameter		Minimum	Minimum	Unit
INT1	V _{IL}		0.84	V
	V _{IH}	1.96		V
INT0 , INT2	V _{IL}		0.54	V
	V _{IH}	1.33		V



6. Power Consumption

Power consumption is dependent on the configuration used. It is for this reason that the following consumption values are given for each mode, RF band and type of software used (AT or Open AT).

The following consumption values were obtained by performing measurements on embedded module samples at a temperature of 25°C; and assume a 50Ω RF output.

Three VBATT values are used to measure the consumption, VBATTmin (3.4V), VBATTmax (4.2V) and VBATTtyp (3.8V).

The average current is given for the three VBATT values and the peak current given is the maximum current peak measured with the three VBATT voltages.

For a more detailed description of the operating modes, see document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47.

6.1. Power Consumption without the Open AT Application Framework

The following measurement results are relevant when there is no Open AT Application Framework application.

For an explanation of the power consumption modes, please refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47.

Table 53. Power Consumption without the Open AT Application Framework

Operating Mode	Parameters	I _{AVERAGE} ; VBATT = 3.8V	I _{PEAK}	Unit
ALARM Mode		29.5		μA
SLEEP Mode		2.2		mA
ACTIVE Mode		45		mA
SLEEP mode with telecom stack in Idle Mode ¹	Case 2G (Paging 9/Rx burst occurrence ~2s)	1.975		mA
	Case 2G (Paging 2/Rx burst occurrence ~0.5s)	3.937		mA
	Case WCDMA (Paging 9)	1.767		mA
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5/gam.3 (TX power 33dBm)		2000	mA
	1800/1900 MHz - PCL0/gam.3 (TX power 30dBm)		1746	mA
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)	595		mA
	850/900 MHz - PCL19 (TX power 5dBm)	101		mA
	1800/1900 MHz - PCL0 (TX power 30dBm)	390		mA
	1800/1900 MHz - PCL15 (TX power 0dBm)	104		mA
GPRS Transfer Mode class 8 (4Rx/1Tx)	850/900 MHz - gam. 3(TX power 33dBm)	486		mA
	1800/1900 MHz - gam.3(TX power 30dBm)	371		mA

Operating Mode	Parameters	I _{AVERAGE} ; VBATT = 3.8V	I _{PEAK}	Unit
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 30dBm)	497		mA
	1800/1900 MHz - gam.3 (TX power 27dBm)	429		mA
GPRS Transfer Mode class 12 (1Rx/4Tx)	850/900 MHz - gam.3 (TX power 27dBm)	531		mA
	1800/1900 MHz - gam.3 (TX power 24dBm)	475		mA
EGPRS Transfer Mode class 8 (4Rx/1Tx)	850/900 MHz - gam.6 (TX power 27dBm)	229		mA
	1800/1900 MHz - gam.5 (TX power 26dBm)	285		mA
EGPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.6 (TX power 24dBm)	341		mA
	1800/1900 MHz - gam.5 (TX power 23dBm)	419		mA
EGPRS Transfer Mode class 12 (1Rx/4Tx)	850/900 MHz - gam.6 (TX power 21dBm)	376		mA
	1800/1900 MHz - gam.5 (TX power 20dBm)	476		mA
UMTS Connected Mode (Voice)	BAND I @ +22 dBm	544	613	mA
	BAND I @ +10 dBm	220		mA
	BAND II @ +22 dBm	485	521	mA
	BAND II @ +10 dBm	221		mA
	BAND V @ +22 dBm	483	516	mA
	BAND V @ +10 dBm	198		mA
	BAND VI @ +22 dBm	488	511	mA
	BAND VI @ +10 dBm	208		mA
	BAND VIII @ +22dBm	466	491	mA
	BAND VIII @ +10dBm	289		mA
UMTS Data Transfer2 384kbits/s	BAND I @ +22 dBm	558	579	mA
	BAND I @ +10 dBm	226	244	mA
	BAND II @ +22 dBm	605	626	mA
	BAND II @ +10 dBm	227	246	mA
	BAND V @ +22 dBm	485	509	mA
	BAND V @ +10 dBm	197	217	mA
	BAND VI @ +22 dBm	499	515	mA
	BAND VI @ +10 dBm	208	227	mA
	BAND VIII @ +22dBm	448	473	mA
	BAND VIII @ +10dBm	294	315	mA

Operating Mode	Parameters	I _{AVERAGE} ; VBATT = 3.8V	I _{PEAK}	Unit
HSDPA Data Transfer2 Cat. 8 7.2Mbits/s	BAND I @ +22 dBm	415	634	mA
	BAND I @ +10 dBm	302	322	mA
	BAND II @ +22 dBm	637	707	mA
	BAND II @ +10 dBm	409	437	mA
	BAND V @ +22 dBm	533	570	mA
	BAND V @ +10 dBm	251	275	mA
	BAND VI @ +22 dBm	552	590	mA
	BAND VI @ +10 dBm	262	287	mA
	BAND VIII @ +22dBm	523	562	mA
	BAND VIII @ +10dBm	357	381	mA
HSUPA Data Transfer2 Cat. 5 2Mbist/s	BAND I @ +22 dBm	517	581	mA
	BAND I @ +10 dBm	395	420	mA
	BAND II @ +22 dBm	548	642	mA
	BAND II @ +10 dBm	394	416	mA
	BAND V @ +22 dBm	439	483	mA
	BAND V @ +10 dBm	247	268	mA
	BAND VI @ +22 dBm	455	501	mA
	BAND VI @ +10 dBm	260	279	mA
	BAND VIII @ +22dBm	415	435	mA
	BAND VIII @ +10dBm	342	364	mA

TX means that the current peak is the RF transmission burst (Tx burst)

RX means that the current peak is the RF reception burst (Rx burst)

- 1 This mode consumption is dependent on the USIM card used. Some USIM cards respond faster than others; the longer the response time, the higher the consumption. The measurements were performed with a large number of 3V USIM cards.

Note: The USB port must be deactivated to enter Sleep Mode.

6.2. Power Consumption with the Open AT Application Framework

The activation of software could increase the power consumption up to 75mA in ACTIVE mode and CONNECTED mode when the full CPU load is used by the Open AT Application Framework application.

7. Reliability Compliance and Recommended Standards

7.1. Environmental Specifications

The AirPrime Q2698 embedded module is compliant with the operating classes listed in the following table. The temperature range supported by each operating class is also specified.

Table 54. Operating Class Temperature Range

Conditions	Temperature Range
Operating / Class A	-30°C to +70°C
Operating / Storage / Class B	-40°C to +85°C

7.1.1. Functions Status Classification

7.1.1.1. Class A

The embedded module remains fully functional, meeting GSM performance criteria in accordance with ETSI requirements, across the specified temperature range.

7.1.1.2. Class B

Operating Class B restrictions depends on the AirPrime Q2698 implementation; refer to section 9 Design Guidelines for optimized implementation.

The embedded module remains functional, across the specified temperature range. Some GSM parameters may occasionally deviate from the ETSI specified requirements. Auto shut down is implemented for protection against extreme temperature (deactivated for emergency calls).



8. Certification Compliance and Recommended Standards

8.1. Certification Compliance

The AirPrime Q2698 embedded module connected on a development kit board application is compliant with the following requirements:

Table 55. Standards Conformity for the Q2698 Embedded Module

Domain	Applicable Standard
Safety & Health	IEC 60950:2005+A1:2009 EN 60950:2006+A11:2009+A1:2010 EN 62311: 2008
Efficient use of the radio frequency spectrum	EN 301 440-1, v1.6.1 EN 301 440-2 v1.4.1 EN 301 511, v9.0.2 EN 301 908-1, v4.2.1 EN 301 908-2, v5.2.1
EMC	EN 301 489-1, v1.9.2 EN 301 489-3, v1.4.1 EN 301 489-7, v1.3.1 EN 301 489-24, v1.5.1
FCC	FCC Part 22, 24

8.2. Applicable Standards Listing

The table hereafter gives the basic list of standards applicable for the AirPrime Q2698 Embedded Module (2G (R99/Rel. 4)).

Note: References to any features can be found from these standards.

Table 56. Applicable Standards and Requirements for the Q2698 Embedded Module

Document	Current Version	Title
GCF-CC	3.46.0	GSM Certification Forum - Certification Criteria
NAPRD.03	5.11	Overview of PCS Type certification review board (PTCRB) Mobile Equipment Type Certification and IMEI control
TS 51.010-1	10.1.0	3rd Generation Partnership Project; Technical Specification Group GSM/EDGE Radio Access Network; Digital cellular telecommunications system (Phase 2+); Mobile Station (MS) conformance specification; Part 1: Conformance specification
TS 51.010-2	10.1.0	3rd Generation Partnership Project; Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station (MS) conformance specification; Part 2: Protocol Implementation Conformance Statement (PICS) proforma specification

Document	Current Version	Title
TS 51.010-4	4.23.0	3rd Generation Partnership Project; Technical Specification Group GSM/EDGE Radio Access Network; Digital cellular telecommunications system (Phase 2+); Mobile Station (MS) conformance specification; Part 4: SIM Application Toolkit Conformance specification
EN 301 511	9.0.2	Global System for Mobile Communications (GSM); Harmonised standard for mobile stations in the GSM 900 and DCS 1800 bands covering essential requirements under article 3.2 of the R&TTE directive (1999/5/EC)
EN 301 908-2	5.2.1	Global System for Mobile Communications (GSM); Harmonised standard for mobile stations in the GSM 900 and DCS 1800 bands covering essential requirements under article 3.2 of the R&TTE directive (1999/5/EC)

Federal Communications Commission (FCC) rules and Regulations: Power listed on the Grant is conducted for Part 22 and conducted for Part 24.

This device is to be used only for mobile and fixed applications. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter within a host device, except in accordance with FCC multi-transmitter product procedures.

Antennas used for this OEM module must not exceed a gain of 7.5dBi (850MHz) and 3.5dBi (1900MHz) respectively. This device is approved as a module to be installed in other devices.

Installed in other portable devices, the exposure conditions require a separate equipment authorization.

The licensed module has an FCC ID label on the module itself. The FCC ID label must be visible through a window or it must be visible when an access panel, door or cover is easily removed.

If not, a second label must be placed on the outside of the device that contains the following text:

Contains FCC ID: N7NQ2698

Manufacturers of mobile or fixed devices incorporating AirPrime Q2698 embedded module are advised to:

- clarify any regulatory questions,
- have their completed product tested,
- have product approved for FCC compliance, and
- include instructions according to above mentioned RF exposure statements in end product user manual.

Please note that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

9. Design Guidelines

This section provides general design guidelines for the AirPrime Q2698 embedded module.

9.1. Power Supply

The power supply is one of the key issues in the design of a terminal.

A weak power supply design could, in particular, affect:

- EMC performance
- The emission spectrum
- Phase error and frequency error

When designing the power supply, careful attention should be paid to the following:

- Quality of the power supply
 - Low ripple, PFM (Power Frequency Modulation) or PSM (Phase Shift Modulation) systems should be avoided
 - Linear regulation or PWM converters are preferred for low noise.
- Capacity to deliver high current peaks in a short time (pulsed radio emission).
- That the VBATT line supports peak currents with an acceptable voltage drop which guarantees a VBATT minimal value of 3.4V.

9.2. Antenna

Sierra Wireless strongly recommends working with an antenna manufacturer either to develop an antenna adapted to the application or to adapt an existing solution to the application.

Both the mechanical and electrical antenna adaptation is one of the key issues in the design of the GSM/UMTS terminal.

9.3. Thermal Recommendations

In order to improve thermal dissipation in the customer board, it is recommended to add foam on the bottom side of the AirPrime Q2698 and to add a copper area (without solder mask) on both sides of the customer PCB. Both sides shall be connected with thermal via.

9.4. EMC Recommendations

EMC tests must be performed on the application as soon as possible to detect any potential problems.

When designing, special attention should be paid to:

- Possible spurious emission radiated by the application to the RF receiver in the receiver band
- ESD protection is **mandatory** on all signals which have external accessibility (typically human accessibility). Typically, ESD protection is mandatory for the:
 - USIM (if accessible from outside)
 - Serial link
- EMC protection on audio input/output (filters against 900MHz emissions)
- Biasing of the microphone inputs
- Length of the USIM interface lines (preferably < 10cm)
- Ground plane: Sierra Wireless recommends a common ground plane for analog/digital/RF grounds.
- A metallic case or plastic casing with conductive paint are recommended

Note: The embedded module does not include any protection against over-voltage.

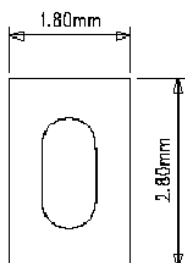
9.5. Layout Requirements

CHIPS & BORING DIAMETER

of the WISMO QUIK mechanical insertion pins

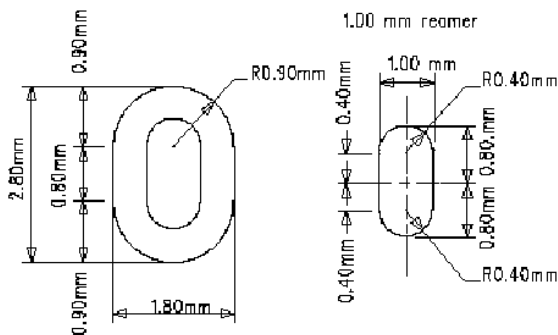
CASE N 1

To be used in priority



CASE N 2

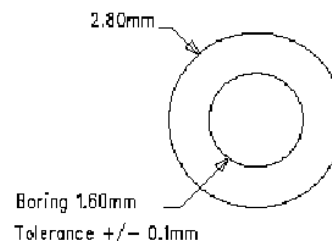
on specific request



Tolerance $\pm 0.1\text{mm}$
1.00 mm reamer

CASE N 3

Other



THERMAL BRAKES DEFINITION

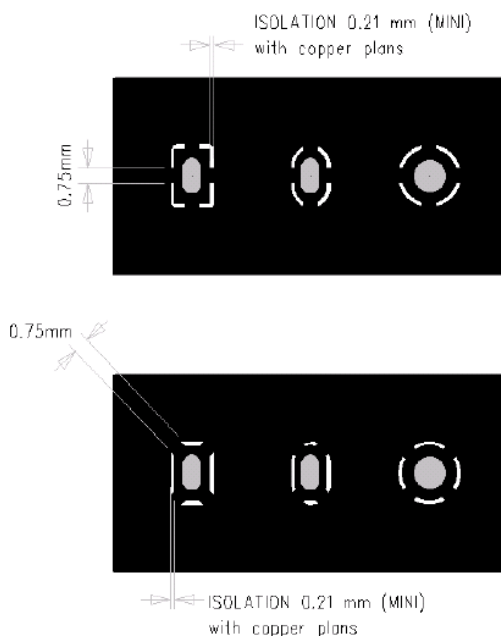


Figure 40. Layout Requirement

9.6. Mechanical Integration

Attention should be paid to:

- Antenna cable integration (bending, length, position, etc)
- Leads of the embedded module to be soldered to the Ground plane

9.7. Operating System Upgrade

The AirPrime Q2698 embedded module operating system is stored in flash memory and can be easily upgraded.

Caution: *In order to follow regular changes in the 3GPP standard and to offer a state-of-the-art Operating System, Sierra Wireless recommends that the application designed around an embedded module (or embedded module-based product) allow easy Operating System upgrades on the embedded module via the standard X-modem protocol. Therefore, the application shall either allow a direct access to the embedded module serial link through an external connector or implement any mechanism allowing the embedded module Operating System to be downloaded via X-modem.*

The Operating System file can be downloaded to the modem using the X-modem protocol. The AT+WDWL command allows the download process to be launched (refer to document [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47 for more information).

The serial signals required to proceed with X-modem downloading are:

- Rx
- Tx
- RTS
- CTS
- GND

The Operating System file can also be downloaded to the modem using the DOTA (download over the air) feature. This feature is available with the Open AT Application Framework interface. For more details, please refer to the documents listed in section 11.2 Reference Documents.



10. Connector and Peripheral Device References

This section contains a list of recommended manufacturers or suppliers for the peripheral devices to be used with the AirPrime Q2698 embedded module.

10.1. General Purpose Connector

The GPC is a 100-pin connector with 0.5mm pitch from the from PANASONIC Group's P5K series, with the following reference:

- AXK600347BN1

The mating connector has the following reference:

- AXK500147BN1J

The stacking height is 3.0 mm.

Sierra Wireless recommends that the **AXK500147BN1J** connector be used for applications to benefit from Sierra Wireless prices. For more information, contact Panasonic and quote the Sierra Wireless connector reference: **1710741**.

For more information about the recommended GPC, refer to the GPC data sheets available from Panasonic (see <http://www.panasonic.com/host/industrl.html>).

10.2. USIM Card Reader

- AMPHENOL C707 series (see <http://www.amphenol.com>)
- JAE (see <http://www.jae.co.jp>)
- MOLEX 99228-0002 (connector)/MOLEX 91236-0002 (holder) (see <http://www.molex.com>)

10.3. Microphone

- HOSIDEN
- PANASONIC
- PEIKER

10.4. Speaker

- SANYO
- HOSIDEN
- PRIMO
- PHILIPS

10.5. Antenna Cable

A wide variety of cables fitted with UF-L connectors is offered by HIROSE:

- UF-L pigtails, Ex: Ref = **U.FL-2LP(V)-04-A-(100)**
- UF-L, Ex: Ref = **U.FL-R-SMT**
- UF-L cable assemblies
- Between series cable assemblies

More information is also available from <http://www.hirose-connectors.com/>.

For the coaxial cable soldered on the RF pad the following references have been certified for mounting on the AirPrime Q2698 embedded module:

- RG178
- RG316

10.6. RF Antenna

RF antennas and support for antenna adaptation can be obtained from manufacturers such as:

- TAOGLAS (<http://www.taoglas.com>)
- HIRSCHMANN (<http://www.hirschmann.com/>)

>> 11. References

11.1. Web Site Support

Table 57. Web Site Support Links

Content	Web Site
General information about Sierra Wireless and its range of products	http://www.sierrawireless.com/
Open AT Application Framework Introduction	http://www.sierrawireless.com/openAT
Sierra Wireless Developer Zone	http://developer.sierrawireless.com/
Sierra Wireless Developer Forum	http://forum.sierrawireless.com/

11.2. Reference Documents

For more details, several reference documents can be consulted. The Sierra Wireless documents referenced herein are provided in the Sierra Wireless documentation package; however, the general reference documents which are not Sierra Wireless owned are not provided in the documentation package.

Please check the web site for the latest documentation available.

11.2.1. Sierra Wireless Documents

- [1] ADL User Guide for Open AT Application Framework OS 6.37
Reference: 4111704
- [2] Open AT Application Framework AT Commands Interface Guide for Firmware 7.47
Reference: 4111703
- [3] AirPrime Q26 Series Development Kit User Guide
Reference: 4112192

11.2.2. General Reference Documents

- [4] "I²C Bus Specification and user guide", Version 3.0, NXP 2007
- [5] ISO 7816-3 Standard

11.3. List of Abbreviations

Table 58. Abbreviations

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CB	Cell Broadcast
CEP	Circular Error Probable
CLK	CLock
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital to Analog Converter
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EFR	Enhanced Full Rate
EGPRS	Enhanced General Packet Radio Service
E-GSM	Extended GSM
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service
EN	ENable
ESD	ElectroStatic Discharges
FIFO	First In First Out
FR	Full Rate
FTA	Full Type Approval
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output

Abbreviation	Definition
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HSxPA	High Speed x(downlink/uplink) Packet Access
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MT	Mobile Terminated
na	Not Applicable
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal
NTC	Negative Temperature Coefficient
PA	Power Amplifier
Pa	Pascal (for speaker sound pressure measurements)
PBCCH	Packet Broadcast Control CHannel
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation (audio) or Protection Circuit Module (battery)
PDA	Personal Digital Assistant
PFM	Power Frequency Modulation
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RST	ReSeT
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime services
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial DAta

Abbreviation	Definition
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
SPK	SPEaKer
SRAM	Static Random Access Memory
TBC	To Be Confirmed
TDMA	Time Division Multiple Access
TP	Test Point
TVS	Transient Voltage Suppressor
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
USIM	Universal Subscriber Identification Module
USSD	Unstructured Supplementary Services Data
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access



12. Safety Recommendations (for Information Only)

For the efficient and safe operation of your GSM device, please read the following information carefully.

12.1. RF Safety

12.1.1. General

Your GSM terminal is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out as well as receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

12.1.2. Exposure to RF Energy

There has been some public concern on possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the guidelines below.

12.1.3. Efficient Terminal Operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

If your terminal has an extendable antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However your GSM terminal operates more efficiently with the antenna when it is fully extended.

Do not hold the antenna when the terminal is "IN USE". Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

12.1.4. Antenna Care and Replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace a damaged antenna immediately. You may repair antenna to yourself by following the instructions provided to you. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Buy or replace the antenna only from the approved suppliers list. Using of unauthorized antennas, modifications or attachments could damage the terminal and may violate local RF emission regulations or invalidate type approval.

12.2. General Safety

12.2.1. Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please:

- give full attention to driving,
- pull-off from the road and park before making or answering a call if driving conditions so require.

12.2.2. Electronic Devices

Most electronic equipment, for example in hospitals and motor vehicles is shielded from RF energy. However, RF energy may affect some improperly shielded electronic equipment.

12.2.3. Vehicle Electronic Equipment

Check your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

12.2.4. Medical Electronic Equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

12.2.5. Aircraft

Turn your terminal OFF before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you should have prior permission from a crew member to use your terminal while the aircraft is on the ground. In order to prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

12.2.6. Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

12.2.7. Blasting Areas

To avoid interfering with blasting operations, turn your unit OFF when you are in a "blasting area" or in areas posted: "turn off two-way radio". Construction crew often uses remote control RF devices to set off explosives.

12.2.8. Potentially Explosive Atmospheres

Turn your terminal **OFF** when in any area with a potentially explosive atmosphere. Though it is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fuelling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is used.



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