Radiocrafts
Embedded Wireless Solutions

RC2000

2.45 GHz FSK Multi-Channel RF Transceiver Module

Product Description

The RC2000 RF Transceiver Module is a compact surface-mounted module for multi-channel FSK operation in the 2.45 GHz ISM band. The module is completely shielded and pre-certified for operation under the European radio regulations for license-free use, and complies with FCC (US) and ARIB (Japan) regulations.

Applications

- OEM equipment
- Home and building automation
- Radio modems
- Point-of-sales terminals
- Bar code scanners
- Telemetry stations
- Fleet management
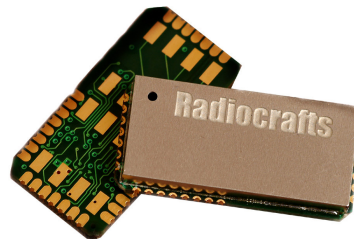
Features

- Multi-channel FSK
- Compact shielded module for SMD mounting
- Embedded RF protocol (RC232™)
- 83 channels at 2.400 – 2.483 GHz
- Buffered mode: 0.6 – 19.2 kBd UART Baud rate, max 31 byte buffer
                                  10 kbit/s, 250 kbit/s and 1 Mbit/s on air RF data rate
- Un-buffered transparent mode: 10 kbit/s, 250 kbit/s and 1 Mbit/s streaming data rate
- 2.8 – 5.5 V supply voltage, 3/5 V compliant I/O
- Conforms with EN 300 440 (Europe), FCC CFR 47 part 15 (US), ARIB STD-T66 (Japan)

Quick Reference Data (3.0V, 25°C)

Parameter	Min	Typ	Max	Unit
Frequency band	2400		2483	MHz
Number of channels		83		
RF data rate (programmable)	10		1000	kbit/s
UART data rate	0.6		19.2	kBaud
Output power (programmable)	-25		-3	dBm
Adjacent Channel Power (2 MHz)		-33		dBc
Sensitivity (10 kbit/s)		-101		dBm
Adjacent Channel Rejection (250 kbit/s)		12		dB
Image Channel Rejection (250 kbit/s)		39		
Blocking, out-of-band		49		dB
Supply voltage	2.8		5.5	Volt
Current consumption, RX		25		mA
Current consumption, TX 0dBm		21		mA
Current consumption, SLEEP		85		µA
Current consumption, OFF		0.003		µA
Temperature range	-30		+85	°C

Typical Application Circuit
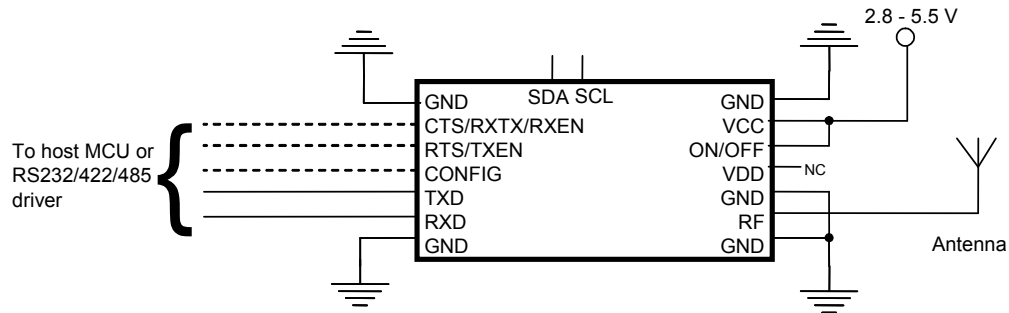
Quick Product Introduction

How do I transmit data?
Send your data to the RXD pin on the module. Use the UART format with settings (19200, 8, 1, N, no flow control), use 2 stop-bits if CTS is enabled. Up to 31 bytes are buffered in the module. The module will transmit the data when

- the max packet length is reached
- the unique end character is sent to the module
- the modem timeout limit is reached

The packet length, end character and timeout limit are configurable in-circuit.

How do I receive data?
Any received data packet with correct address and check sum will be sent on the TXD pin using the same UART format as for transmit.
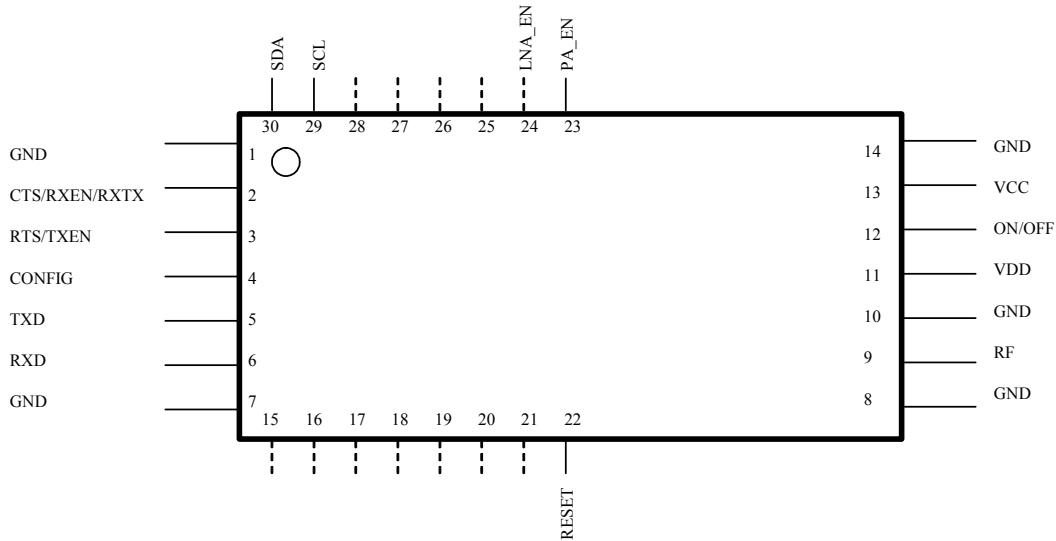
What about the antenna?
In most cases a simple quarter wavelength wire or a PCB track will do. Connect a piece of wire to the RF pin with length corresponding to the quarter of a wavelength. For space limited products, contact Radiocrafts and we will recommend the best antenna solution for your application.

How do I change the RF channel or any other parameter?
To change configurable parameters, assert the CONFIG pin, and send the command string using the same serial interface as for transmitting data. Parameters can be changed permanently and stored in non-volatile memory in the module.

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Pin Assignment

Pin Description

Pin no	Pin name	Description	Equivalent circuit
1	GND	System ground	GND (ground symbol)
2	CTS/RXEN/RXTX	UART Clear to Send, UART RXTX (for RS485), Receive Mode Enable, or SLEEP mode activation. Connect to VDD if not used. Internal 100 kΩ series resistor, 2.7 V output.	Input: VDD (2.7V) 100k (circuit)
3	RTS/TXEN	UART Request to Send, Transmit Mode Enable, or SLEEP mode activation. Connect to VDD if not used. Internal 100 kΩ series resistor.	
4	CONFIG	Configuration Enable. Active low. Should normally be set high. Connect to VDD if not used. Internal 100 kΩ series resistor.	Output: VDD (2.7V)
5	TXD	UART TX Data. Internal 100 kΩ series resistor, 2.7 V output.	100k (circuit)
6	RXD	UART RX Data. Internal 100 kΩ series resistor.	
7	GND	System ground	GND (ground symbol)
8	GND	System ground	

9	RF	RF I/O connection to antenna	 RF○───┬──┤├── ──── 220p 10k
10	GND	System ground	GND ○───
11	VDD	Supply voltage output, regulated 2.7 V. Should normally be left open if not used for pull-ups.	──── 2.7 V VREG ──○ VDD 2u2
12	ON/OFF	Module on/off (shutdown). ON when high, OFF when low. See also important note under Power Management page 14.	ON/OFF ○───
13	VCC	Supply voltage input. Internally regulated. Maximum rise-time requirement apply, see Electrical Specification.	VCC ○───┬─── 2.7 V VREG ──── 2u2
14	GND	System ground	GND ○───
15-21	RESERVED	Test pins, or pins reserved for internal/future use. *Do not connect!*	
22	RESET	Main reset (active low). Should normally be left open. Internal 100 kΩ pull-up resistor, no series resistor.	VDD (2.7V) 100k RESET ○───
23	PA_EN	External PA Enable output (active low). No internal series resistor or pull-up, 2.7 V output.	VDD (2.7V)
24	LNA_EN	External LNA Enable output (active low). No internal series resistor or pull-up, 2.7 V output.	

25-28	RESERVED	Test pins, or pins reserved for internal/future use. *Do not connect!*	
29	SCL	Transparent synchronous serial data clock. No internal series resistor or pull-up, 2.7 V output.	VDD (2.7V)
30	SDA	Transparent synchronous serial data I/O. No internal series resistor or pull-up, 2.7 V input/output.	

Note 1: In buffered mode the TXD and RXD are used for serial data, and CTS/RXTX and RTS for flow control (optional). If flow control is not used, and RXEN and TXEN are both asserted (active low) the module is set in SLEEP mode. RXEN and TXEN should be connected to VDD if not to be used for SLEEP mode activation. A pull-up resistor is not necessary due to an internal series resistor.
Note 2: In synchronous mode the SCL (data clock output) and SDA (Data input and output) are used for serial data. The RXEN and TXEN pins are then used to select the operation mode of the device. Signals are active low.
Note 3: The CONFIG pin is used to enter configuration mode (change of default settings). Active low.
Note 4: Do not use VDD for supply to external circuits. Should only be used for pull-ups, if required.
Note 5: RXEN, TXEN, CONFIG, TXD and RXD have internal 100 kΩ series resistors. Driving capability when used as outputs is therefore limited and they should be connected to CMOS inputs only.

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Block Diagram
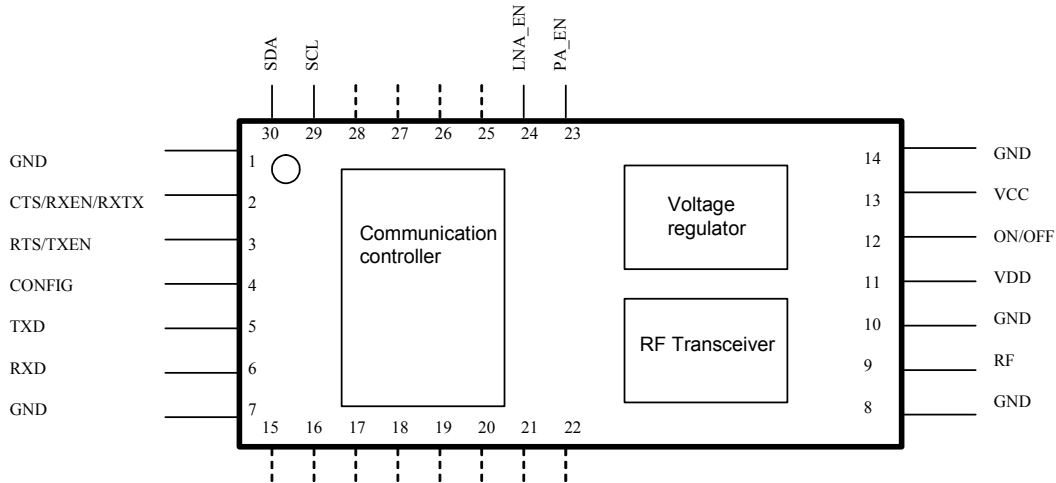
Circuit Description

The module contains a communication controller with embedded RC232™ protocol software, a Frequency Shift Keying (FSK) high performance RF transceiver and an internal voltage regulator.

The communication controller handles the radio packet protocol, the UART interface, the synchronous interface, and controls the RF transceiver. Data to be sent by the host is received at the RXD pin and buffered in the communication controller. The data packet is then assembled with preamble, start-of-frame delimited (SOF), packet control and address information, and Cyclic Redundancy Check sum (CRC) before it is transmitted on RF. The preamble and SOF are always used. The address and CRC are optional.

The RF transceiver modulates the data to be transmitted on RF frequency, and demodulates data that are received. FSK modulation is used for optimum performance.

Received data are checked for correct address and CRC by the communication controller. If the address matches the modules own address, and no CRC errors were detected, the data packet is sent to the host on the TXD line after removing the header.

The asynchronous UART interface consists of RXD and TXD. Optionally CTS/RXTX and RTS can be used for hardware handshake flow control. CTS/RXTX can be used to control the direction of an RS485 driver circuit.

The module can also be used in an un-buffered transparent mode for data streaming. In this case the data interface is synchronous using SCL and SDA for data transfer to/from the host. The RXEN and TXEN are then used to set the operational mode.

When the CONFIG pin is asserted the communication controller enters configuration mode and interprets data received on the RXD pin as configuration commands. There are commands to change the radio channel, the output power, the destination address etc. Permanent changes of the configuration is also possible and are then stored in internal non-volatile memory (EEPROM).

The RC232™ RF protocol and the configuration commands and parameters are described in general in the RC232™ User Manual. The complete list of configurable parameters stored in non-volatile memory that apply for RC2000 is given in the table "Configuration Memory" page

11. For configurable parameters not stored in non-volatile memory and other configuration commands, please refer to "Module configuration" page 10.

The supply voltage is connected to the VCC pin. The module contains an internal voltage regulator and can therefore operate over a wide supply voltage range. The regulated voltage is available at the VDD pin, but should not be used to supply external circuits.

The ON/OFF pin can be used to turn the module completely off, and hence reduce the power consumption to a minimum. For normal operation the ON/OFF pin must be connected to VCC. To turn the module completely off, connect the ON/OFF pin to ground (logic low level). See also Power Management page 14.

RC232™ Embedded Protocol

The module offers a buffered packet radio as well as un-buffered transparent modes in the RC232™ embedded protocol.

Using the buffered packet radio mode (MAC_MODE = 1), all data to be sent is stored in the module before they are transmitted by the RF circuitry. Likewise, when data is received they are stored in the module before they are sent to the host. This allows the communication controller to add address information and to do error check of the data. In buffered mode the UART interface is used to communicate with the host.

If the application requires a transparent data link, the module can be configured to operate in one of three un-buffered modes (MAC_MODE = 0, 2 or 3). In mode 0 the module adds only a preamble and start-of-frame bytes to synchronize the receiver, while in mode 2 and 3 this is left to the user. No addressing or checksum is provided in the transparent modes. A synchronous interface is used to transfer data to/from the host. However, note that the configuration of the module is done using the UART even if the un-buffered transparent mode is used for data transfer. See the Un-buffered transparent mode section page 9 for further information on how to configure and use the transparent modes.

The embedded protocol, configuration commands and configuration memory is described in general in the RC232™ User Manual. This protocol is used in a wide range of RF modules available from Radiocrafts. Please refer to the latest revision available on Radiocrafts web-site. Exceptions and additions that apply for RC2000 only are found throughout in this data sheet.

Maximum Packet Length

In buffered mode the max number of user data bytes in one packet frame on the air is 31 bytes (30 for 10 kbps) in addition to the preamble, start-of-frame delimiter, and a length byte. The 31 (30) bytes includes any address or CRC bytes if enabled. The maximum number of payload bytes is therefore 26 - 31 bytes depending on the configuration. The table below shows the maximum number of payload bytes in each case.

The PACKET_LENGTH must be set accordingly to prevent buffer overflow. This is very important when using UART hardware handshake transferring data using the maximum packet length. The factory setting is 26 in order to prevent accidental overflow when addressing and CRC is used.

ADDRESS_MODE (= # bytes)	CRC_MODE (= # bytes)	PACKET_LENGTH must be set to (1 Mbps and 250 kbps)	PACKET_LENGTH must be set to (10 kbps)
0	0	31 or less	30 or less
0	2	29 or less	28 or less
2	0	29 or less	28 or less
2	2	27 or less	26 or less

Addressing

The module provides addressing enabled by setting ADDRESS_MODE in the configuration memory.

ADDRESS_MODE = 2 is the standard RC232 addressing, using the SYSTEM_ID and the UNIQUE_ID. The SYSTEM_ID must be equal if two modules shall communicate. See the RC232 User Manual for further details.

The UNIQUE_DESTINATION_ID default value is set in the configuration memory (non-volatile memory). It may also be changed in volatile memory using the 'T' command.

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CRC error detection
The module provides error detection enabled by setting CRC_MODE in the configuration memory.

CRC_MODE = 2 is the standard RC232 error detection using a 16-bit CRC check sum. See the RC232 User Manual for further details.

Un-buffered transparent modes
Three different un-buffered transparent modes are provided. The difference between these modes is how the preamble and start-of-frame (SOF) sequence is used to set up the radio link. The different modes are selected by setting MAC_MODE.

MAC_MODE = 0. On the receiver side the SCL and SDA is muted until a valid preamble and SOF is detected. When transmit mode is activated, the module will insert a preamble and SOF that will open the receiver, after which the SCL will start running. After TXEN is activated until the SOF is detected on the receiver and the receivers SCL start to run, there is a period of approximately 4.8 ms. After the receivers SCL start to run there is another 440 us where the data is not valid. The user should include a synchronization code in the data stream in order to recognize valid data. From RXEN de-asserted until SDA and SCL stops it is 120-140 us.

MAC_MODE = 2. On the receiver side the SCL and SDA starts running as soon as RXEN is activated. There is no preamble or SOF detection. When transmit mode is activated the transmitters SCL will start running after approximately 650 us. The module does not insert a preamble or SOF. After approximately 12 us the receiver's data is valid. The user should include a synchronization code in the data stream in order to recognize valid data. From RXEN de-asserted until SDA and SCL stops is 110-130 us.

MAC_MODE = 3 is a combination of the two above where the user must send a valid preamble and SOF in order to open the receiver. On the receiver side the SCL and SDA is muted until a valid preamble and SOF is detected. When transmit mode is activated the transmitters SCL will start running after approximately 650 us. The user should send a preamble and SOF as describe below in order to open the receiver. From RXEN de-asserted until SDA and SCL stops is 120-140 us. This is the recommended transparent mode since the data at the receiver will be immediately available after the SOF is detected.

The preamble and SOF to be sent in MAC_MODE 3 should consist of 4 preamble bytes and 4 SOF bytes. The preamble should be a 1010101…10 pattern. The SOF should be in hexadecimal notation 0xD391DA26. The complete preamble and SOF should therefore be 0xAAAAAAAAD391DA26. The next byte following this pattern will be the first one to appear on the receivers SDA when the SCL starts running.

To enable un-buffered transparent mode the following settings must be done in the configuration memory:
- MAC_MODE (address 0x13) = 0, 2 or 3
- DATA_INTERFACE (address 0x36) = 1
- CRC_MODE (address 0x15) = 0
- ADDRESS_MODE (address 0x14) =0

Module Configuration

The table below shows the complete list of configuration commands provided in the RC2000 module. A general description is found in the RC232 User Manual.

Commands must be sent as ASCII characters or their corresponding binary value. All arguments must be sent as binary values to the module (not as ASCII representation for hex or decimal).

Parameter	Command	Argument in hex (decimal)	Note
Channel	'C' – 0x43	RC2000: 0x01-0x53 (1-83)	Data is stored in volatile memory only.
Output power	'P' – 0x50	0x01-0x05 (1-5)	Data is stored in volatile memory only.
Signal strength (RSSI)	'S' – 0x53	RC2000: Return one byte indicating the signal strength	
Destination address	'T' – 0x54	0x00 – 0xFF (0-255)	Data is stored in volatile memory only.
Memory configuration	'M' – 0x4D	(Address, Data): see list of parameters below. 0xFF exits memory configuration.	Used to enter memory configuration menu. Parameters changed are stored in non-volatile memory.
Exit command	'X' – 0x58	(none)	Exit to normal operation mode. All changes of parameters take effect.
Sleep mode	'Z' – 0x5A	(none)	CONFIG pin must be asserted while in SLEEP mode. Exit sleep mode by releasing CONFIG pin.
Test mode 0	'0' – 0x30	(none)	List all configuration memory parameters, product ID and revisions
Test mode 1	'1' – 0x31	(none)	TX carrier. Go to test mode 4 (IDLE) before exiting configuration mode
Test mode 2	'2' – 0x32	(none)	TX modulated signal with PN9 sequence at 1 Mbit/s. Go to test mode 4 (IDLE) before exiting configuration mode
Test mode 3	'3' – 0x33	(none)	Un-buffered RX mode at 1 Mbit/s. Go to test mode 4 (IDLE) before exiting configuration mode
Test mode 4	'4' – 0x34	(none)	IDLE mode. Turns off RX or TX.
Test mode 5	'5' – 0x35	(none)	Power Down mode. Use test mode 6 to power up the module.
Test mode 6	'6' – 0x36	(none)	Power Up mode. Must be used before test mode 1, 2 and 3 if power down mode was used.

For details on using the commands, refer to the RC232 User Manual (Test mode 3-6 is unique for RC2000 and not described in the RC232 manual).

Configuration Memory

The table below shows the complete list of configurable parameters stored in non-volatile memory for RC2000. These values can be changed using the 'M' command. All addresses and arguments must be sent as binary values to the module (not as ASCII representation for hex or decimal).

Parameter	Description	Address hex	Argument dec	Factory setting hex (dec)	Comment
Radio configuration					
RF_CHANNEL	Default RF channel	0x00	1-83	0x32 (50)	See page 22 for channel frequencies.
RF_POWER	Default RF output power	0x01	1-5	0x05 (5)	See page 22 for output power levels.
RF_DATA_RATE	Default RF data rate	0x02	1-3 0x01 (1): 1Mbit/s 0x02 (2): 250kbit/s 0x03 (3): 10 kbit/s	0x01 (1)	
Reserved		0x03		0x00 (0)	
Reserved		0x04		0x02 (2)	
Reserved		0x05		0x01 (1)	
Reserved		0x06		0x00 (0)	
Reserved		0x07		0x00 (0)	
Reserved		0x08		0x00 (0)	
Reserved		0x09		0x00 (0)	
Radio packet configuration					
Reserved		0x0A		0x00 (0)	
Reserved		0x0B-0x0D		0xD391DA	
ABSOLUTE_MAX_PACKET_LENGTH		0x0E		0x20 (32)	Limited by hardware. Do not change.
PACKET_LENGTH	Max packet length. When buffer is full, modem will transmit data	0x0F	0x01-0x1F (1-31)	0x1A (26)	See page 8 for details on maximum value
PACKET_TIMEOUT	Time before modem time-out and transmit buffered data	0x10	0x00-0xFE (0-254) 0x00 (0): None 0x01 (1): 32 ms 0x02 (2): 48 ms 0x03 (3): 64 ms 0x7C (124): 2 s 0xF9 (249): 4 s	0x7C (124)	None means packet timeout is disabled (not 0 s). Use packet length or end character instead. Timeout value is (PACKET_TIMOEOUT x 16 ms) + 0/16 ms min/max 0xFE (254) is max, giving 4.080 sec. Default is 2 s = 0x7C (124)
PACKET_END_CHARACTER		0x11	0x00-0xFF (0-255) 0: None 0x0D (13): CR 0x0A (10): LF 0x5A (90): 'Z'	0x00 (0)	ASCII character (any character can be chosen, CR, LF and 'Z' are examples only)
Medium access, addressing and network management					
Reserved		0x12		0x02 (2)	
MAC_MODE		0x13	0:Transparent 1: Buffered 2: Transparent 3: Transparent	0x01 (1)	Transparent means using RXEN and TXEN. See page 9 for details.
ADDRESS_MODE		0x14	0: No addressing	0x02 (2)	Set to 0 in transparent

			1: Reserved 2: Addressing		mode. For description of the addressing mode see page 8.
CRC_MODE		0x15	0: No CRC 1: Reserved 2: CRC16	0x02 (2)	Set to 0 in transparent mode. See page 9 for details.
Reserved		0x16		0x00 (0)	
Reserved		0x17		0x00 (0)	
Reserved		0x18		0x00 (0)	
UNIQUE_ID	Unique ID (UID)	0x19	0-255	0x01 (1)	
SYSTEM_ID	System (net or family) ID (SID)	0x1A	0x00-0xFF (0-255)	0x01 (1)	
Reserved		0x1B		0x0A (10)	
Reserved		0x1C		0x0A (10)	
Reserved		0x1D		0x0A (10)	
Reserved		0x1E		0x0A (10)	
Reserved		0x1F		0x01 (1)	
Reserved		0x20		0x01 (1)	
UNIQUE_ DESTINATION_ID	Default destination address	0x21		0x01 (1)	Set to same as BROADCAST_ADDRESS when broadcasting using address mode 2.
Reserved		0x22		0x01 (1)	
Reserved		0x23		0x00 (0)	
Reserved		0x24		0x00 (0)	
Reserved		0x24		0x00 (0)	
Reserved		0x26		0x00 (0)	
Reserved		0x27		0x04 (4)	
BROADCAST_ ADDRESS	Broadcast address	0x28	0x00-0xFF (0-255)	0xFF (255)	All nodes accept messages to this address in address mode 2.
Reserved		0x29		0x08 (8)	
Reserved		0x2A		0x00 (0)	
Reserved		0x2B		0x00 (0)	
Reserved		0x2C		0x00 (0)	
Reserved		0x2D		0x00 (0)	
Reserved		0x2E		0x00 (0)	
Reserved		0x2F		0x00 (0)	
Data and configuration interface, UART Serial Port					
UART_BAUD_RATE	Baud rate	0x30	0x00: Not used 0x01: 600 0x02: 1200 0x03: 2400 0x04. 4800 0x05: 9600 0x06: 19200	0x06 (6)	BE CAREFUL IFCHANGING AS HOST MAY LOOSE CONTACT WITH MODULE! Does not take effect until module is re-booted / reset.
Reserved		0x31		0x08 (8)	
Reserved		0x32		0x00 (0)	
Reserved		0x33		0x01 (1)	
Reserved		0x34		0x05 (5)	
UART_FLOW_CTRL	UART flow control	0x35	0: None 1:CTS only 3:CTS/RTS 4:RXTX(RS485)	0x00 (0)	Set to 0 in transparent mode. When handshake is used, the terminal must be configured for 2 stop bits.
DATA_INTERFACE	Data interface	0x36	0x00: UART using RXD and TXD 0x01: Synchronous interface (SDA, SCL) using RXEN and TXEN for direction control	0x00 (0)	When buffered mode is selected for MAC_MODE use UART. For flow control, see above. When transparent mode is selected for MAC_MODE use Synchronous interface.
Reserved		0x37		0x01 (1)	
Reserved		0x38		0x2B (43)	

Reserved		0x39		0x00 (0)	
Reserved		0x3A		0x01 (1)	
Exit from memory configuration		0xFF	No argument should be sent		To exit from configuration mode the 'X' command must be sent after '>' is received.

Power Management

The module can be set in SLEEP mode or OFF mode in order to reduce the power consumption.

The low power SLEEP mode is entered by using the SLEEP command, see RC232™ User Manual, or by pulling both RXEN and TXEN low. In sleep mode the module will not receive or detect incoming data, neither from the host (UART port) nor from the RF transceiver. The module is awakened from the SLEEP mode by a positive edge on the CONFIG, RXEN or TXEN pins if the module was set in SLEEP mode using the 'Z' command. The module is awakened by a positive edge on the RXEN or TXEN pin if these two pins were used to enter SLEEP mode. CONFIG must be high when awakening the module to avoid setting the module directly in configuration mode.

Note: If UART handshake is used, the RXEN and TXEN pins can not be used to enter SLEEP mode. In this case, use the SLEEP command.

The ultra-low power OFF mode is entered by pulling the ON/OFF pin low. The module will then shut down completely. The module is turned on by setting the ON/OFF pin high (to VCC). After the module has been in OFF mode all operational parameters are set to the default values stored in configuration memory.

The VDD output should not be used to supply external circuits, other than for pull-ups for RXEN, TXEN and CONFIG.

Power on Reset

In order to ensure that the internal Power on Reset (POR) operates correctly, the maximum rise-time specification for VCC must be met (see Electrical Specifications). Longer VCC rise-time or short supply voltage interrupts may cause improper operation that is not handled by the internal POR. For proper operation it is crucial to use an external control of the RESET pin as described below (see also Application Note AN001).

When turning the module OFF by setting ON/OFF low, or switching VCC off, great care should be taken to ensure proper power-on-reset (POR). I/O pins driving the module when the module is off can give a low residual voltage in the module that prevents trigging of the internal POR. Also in this case an external RESET signal is required to ensure proper start-up.

The figures below shows suggested circuits for RESET control. The MCU can operate over the whole VCC operation range. But do note that the module TXD output operates at 2.7 V, and hence the host MCU must accept this lower voltage swing. If not, a voltage translator must be used, see section 'I/O pin Interfaces' page 18).The suggested solutions are:

- Control the RESET pin by a separate I/O pin from the MCU using a 10 kOhm series resistor (RESET does not have any internal serial resistor, but a 100k pull-up to VDD). Set RESET low before ON/OFF is turned low, and keep low until ON/OFF is high again (VCC – 10%). This will ensure proper power-on reset (POR). See Figure 1 below.
- Control the RESET pin by the same I/O in used to control ON/FF. A 10 kOhm series resistor is used for the RESET pin to limit the input current from the 3 / 5V signal from the MCU. See Figure 2 below.
- Use an external POR and brown-out supervisory circuit. The circuit should be connected between VDD and GND, controlling RESET. This solution will force RESET low as long as VDD is below the threshold voltage. The RESET has an internal pull-up resistor to VDD, thus an open-drain output supervisory circuit can be used. A threshold voltage between 2.3 and 2.6 V is recommended. See Figure 3. Supervisory circuits are suggested below.
- If the host system already has an external POR and brown-out supervisory circuit, this can also be used to control the module RESET. The supervisory circuit should be connected between VCC (or the MCU supply voltage if different) and GND, controlling RESET through a 10k resistor. This solution will force RESET low as long as VCC is below the threshold voltage. The RESET has an internal pull-up resistor to VDD, thus an open-drain output supervisory circuit can be used. A threshold voltage of 2.8 V or higher is recommended. See Figure 4. Supervisory circuits are suggested below.
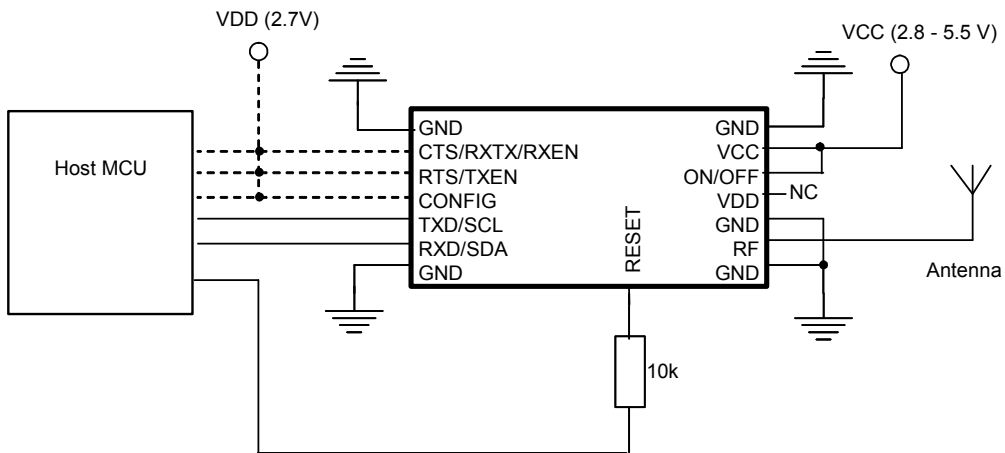
VDD (2.7V)

VCC (2.8 - 5.5 V)

Host MCU

GND
CTS/RXTX/RXEN
RTS/TXEN
CONFIG
TXD/SCL
RXD/SDA
GND

RESET

GND
VCC
ON/OFF
VDD — NC
GND
RF
GND

Antenna

10k

Figure 1. Reset circuit using host MCU

VDD (2.7V)

VCC (2.8 - 5.5 V)

Host MCU

GND
CTS/RXTX/RXEN
RTS/TXEN
CONFIG
TXD/SCL
RXD/SDA
GND

RESET

GND
VCC
ON/OFF
VDD — NC
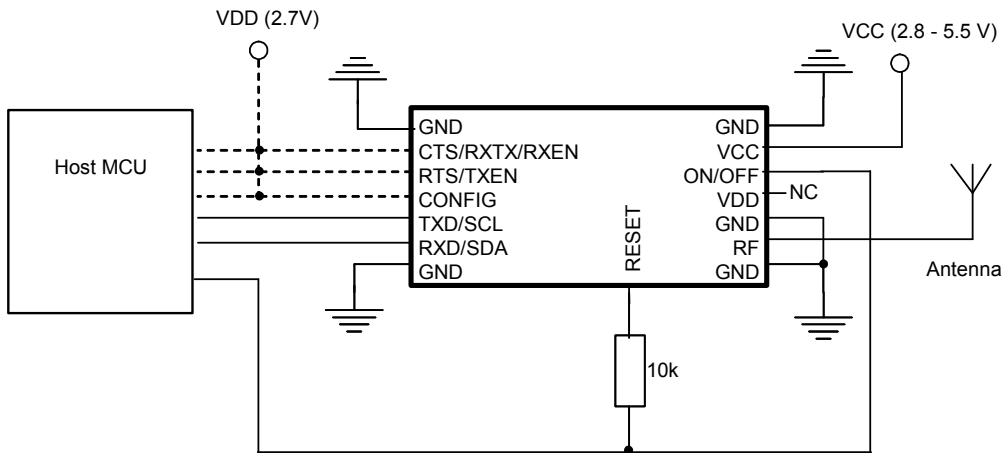GND
RF
GND

Antenna

10k

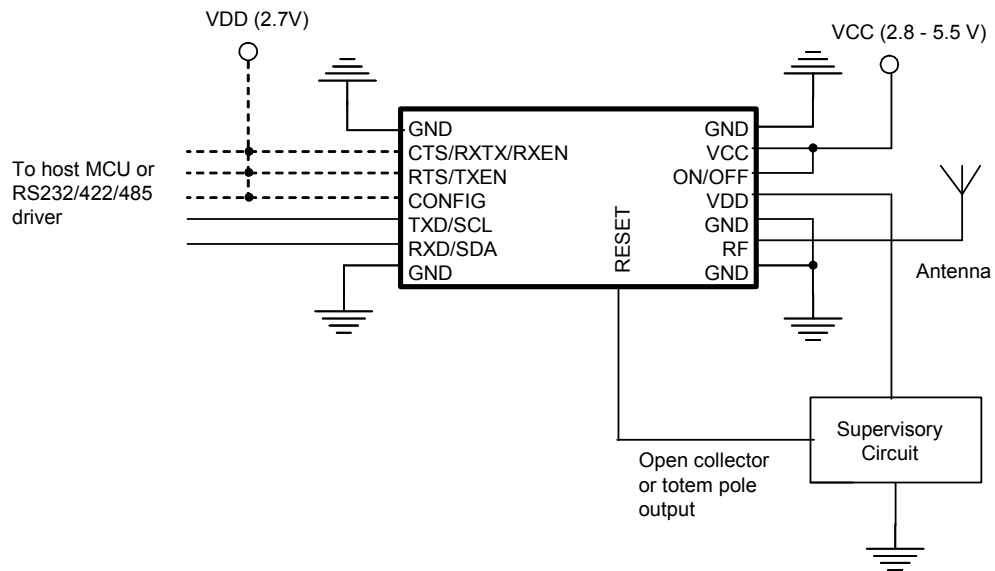**Figure 2. Reset circuit controlling ON/OFF**

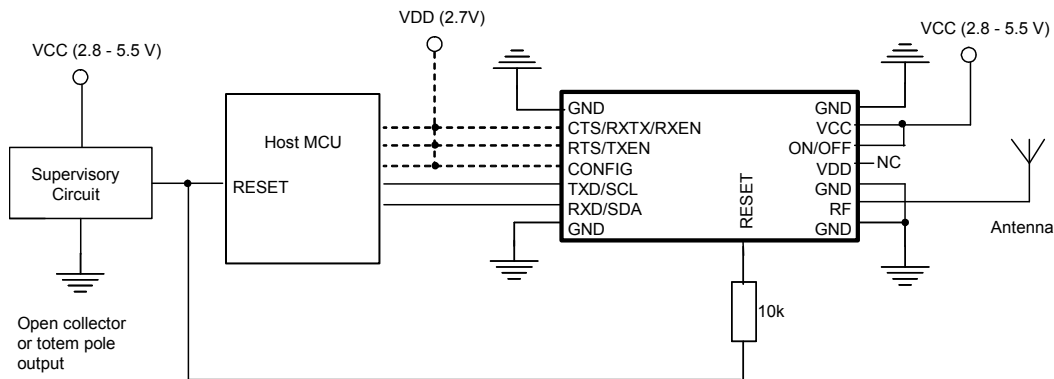**Figure 3. Reset circuit using supervisory circuit on VDD**

Figure 4. Reset circuit using supervisory circuit on VCC

As a reference, potential suppliers of supervisory circuits are provided below. Radiocrafts does not endorse any specific vendor. In most cases, similar components from other suppliers will provide satisfactory performance. A threshold voltage of 2.3 – 2.6 V is recommended if the supervisory circuit is connected to VDD.

Manufacturer	Model number	Delay [ms]	Nominal trigger volt.	Max trigger volt.	Output	Package	Distributor
Microchip	MCP100-270	150-700	2.62	2.70	Push-pull	SOT-23/3 & TO92	Future, Digi-Key
Microchip	TC1275-20ENB	100-300	2.55	2.64	Complementary 100k pull down for RST=0V	SOT-23B/3	Future, Digi-Key
Maxim	MAX803R/	140-	2.63	2.70	Open-drain/	SOT-23/3	Maxim direct

	MAX809R	460			push-pull	SC-70/3	
Maxim	MAX6328_R25-T	100-280	2.50	2.562	Open drain, external pull-up resistor	SOT-23/3 SC-70/3	Maxim direct
Analog Devices	ADM809_Z	140-460	2.32	2.38	Push-pull	SOT-23/3 SC-70/3	Arrow
Texas Instruments	TPS3800G27	60-140	2.5	2.55	Push-pull	SC-70/5	Avnet, Digi-Key
Texas Instruments	TPS3809J25	120-280	2.25	2.30	Push-pull	SOT-23/3	Avnet, Digi-Key
Texas Instruments	TPS3836J25	5-15	2.25	2.29	Push-pull	SOT-23/5	Avnet, Digi-Key
Sipex	SP810EK-2-3	100-1030	2.3	2.346	Push-pull	SOT-23/3	Future, Newark
National Semiconductor	LM3722EM5-2.32	100-560	2.32	2.37	Push-pull	SOT-23/5	Future

I/O pin Interfaces

As noted in the Pin Description, RXEN (CTS/RXTX), TXEN (RTS) and CONFIG pins should have their pull-ups connected to VDD, not VCC. If RXEN is used as CTS (hardware handshake) or as RXTX (RS485) output, no pull-up is required and should be avoided as this reduces the voltage swing due to the internal resistor.
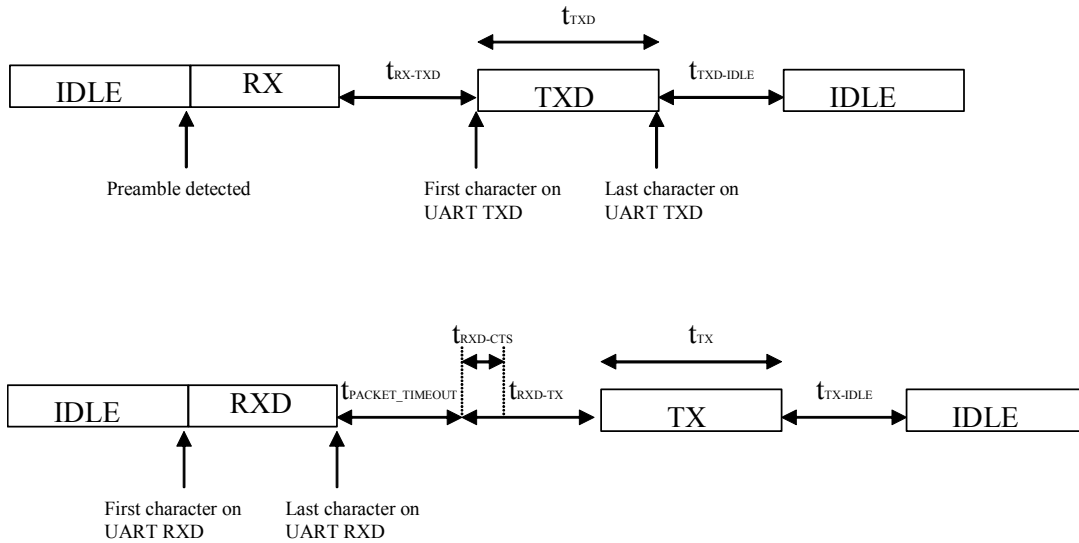
Important note: The RXEN (CTS/RXTX) and TXD (SCL) and SDA pins are logic signals with 0 – VDD voltage swing, where VDD is 2.7 V. When connecting these signals to external circuitry operating on supply voltage above 2.7 V, a level translator may be required. Single transistor buffers or integrated level translators can be used for this purpose. An example of such a level translator is SN74LVC1t45.
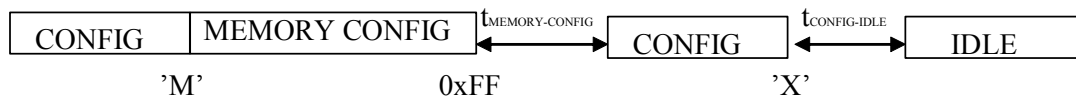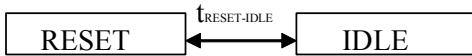
Timing Information

The figure and table below shows the timing information for the module when changing between different operating states.

The IDLE state is the normal state where the module search for preamble on the air and wait for a character to be received on the UART. RXD is the state when receiving characters from the host filling up the internal buffer. TX state is when the data is transmitted on the air. RX state is when data is received from the air after a preamble detection. TXD is the state where the received data is sent to the host on the UART.

CONFIG is the state entered by asserting the CONFIG pin and used during parameter configuration, while MEMORY CONFIG is the sub-state entered by the 'M' command where the configuration memory is being programmed.

```
           t OFF-IDLE
┌─────────┐ ◄──────► ┌─────────┐
│   OFF   │          │  IDLE   │
└─────────┘          └─────────┘


           t RESET-IDLE
┌─────────┐ ◄──────► ┌─────────┐
│  RESET  │          │  IDLE   │
└─────────┘          └─────────┘


           t SLEEP-IDLE
┌─────────┐ ◄──────► ┌─────────┐
│  SLEEP  │          │  IDLE   │
└─────────┘          └─────────┘


             t C-CONFIG              t CONFIG-IDLE
┌─────────┐ ◄──────► ┌─────────┐ ◄──────► ┌─────────┐
│ CONFIG  │          │ CONFIG  │          │  IDLE   │
└─────────┘          └─────────┘          └─────────┘
    'C'                   'X'


┌─────────┬──────────────────┐ t MEMORY-CONFIG           t CONFIG-IDLE
│ CONFIG  │  MEMORY CONFIG    │ ◄──────► ┌─────────┐ ◄──────► ┌─────────┐
└─────────┴──────────────────┘          │ CONFIG  │          │  IDLE   │
    'M'            0xFF                  └─────────┘          └─────────┘
                                            'X'
```

Symbol	Value	Description / Note
t_{RX-TXD}	1.68 ms	Time from last byte is received from the air until first character is sent on the UART
t_{TXD}	Min 620 us	t_{TXD} = # bytes received x 620 us/char (10 bits at 19.2 kBd + 100 us delay per character)
$t_{TXD-IDLE}$	1.4 ms	Time from last character is sent on the UART until module is in IDLE mode (ready for RXD and RX)
$t_{PACKET-TIMEOUT}$	Programmable	If enabled, the packet timeout can be configured from 16/32 ms to 4.08 s. If end character or fixed packet length is used, the timeout is 0.
$T_{RXD-CTS}$	10-30 us	Time from last character is received by the UART (including any timeout) until CTS is activated
t_{RXD-TX}	860 us (1 char) 2.36 ms (16 chars)	Time from last character is received by the UART (including any timeout) until the module sends the first byte on the air. Depends on the number of characters to be sent.
$T_{TX-IDLE}$	1.4 ms	Time from last character is sent on the air until module is in IDLE mode (ready for RXD and RX)
$t_{OFF-IDLE}$	42 ms	
$t_{RESET-IDLE}$	42 ms	
$t_{SLEEP-IDLE}$	Approx. 10 ms	
$t_{CONFIG-PROMPT}$	1 ms	From CONFIG is asserted until prompt '>' (including the prompt)
$t_{C-CONFIG}$	0.6 ms	After setting new channel until prompt '>' (including the prompt) (For other commands like 'M', 'T' there is no delay but immediate prompt)
$t_{CONFIG-M}$	1.0 ms	After sending the 'M' command until prompt '>' (including the prompt)
$t_{MEMORY-CONFIG}$	26 ms	In this period the internal flash is programmed. *Do not reset, turn the module off, or allow any power supply dips in this period as it may cause permanent error in the Flash configuration memory. After 0xFF the host should wait for the '>' prompt before any*

		further action is done to ensure correct re-configuration.
$t_{CONFIG\text{-}IDLE}$	1.7 ms	
t_{TX}	110 us (1 char) 240 us (16 chars)	t_{TX} = # bytes to send x 8 us/byte (at 1 Mbit/s) approximatelly. Add 8 overhead bytes if addressing and CRC is not used. Add additionally 2 extra bytes for addressing and 2 extra bytes for CRC if enabled. At 10 kbps one byte is 800 us, and at 250 kbps one byte is 32 us and t_{TX} is increased accordingly.

Example: To send one character (no CRC or addressing) takes totally 2.5-2.7 ms from the character is received on the UART until the transceiver is back in IDLE mode.

Note also that in IDLE mode every 16 seconds the module recalibrates its internal UART clock reference in order to compensate for temperature drift. The recalibration takes approximately 750 us. There is no recalibration in CONFIG mode, therefore the module should not be left in CONFIG mode for an extended time if the temperature is likely to change by more than +/- 5 degrees.

RF Frequency, Output Power Levels and Data Rates

The following table shows the available RF channels and their corresponding frequencies, nominal output power levels and available data rates.

RF channel	Output power	Data rate
1-83: f_{RF}=2400+N MHz where N is the channel number Factory setting: 50: **2450 MHz**	1: -25 dBm 2: -15 dBm 3: -10 dBm 4: -5 dBm 5: **-3 dBm**	1: **1 Mbit/s** 2: 250 kbit/s 3: 10 kbit/s

RF channel and output power level can be set using the configuration commands 'C' and 'P' respectively. The data rate and *default* RF channel and output power level can be set in the configuration memory by using the 'M' command setting RF_CHANNEL and RF_POWER. The default values are used after power ON and RESET. The default factory settings are shown in **bold** in the table above.

For more details on changing the RF channel, output power or data rate, refer to the RC232™ User Manual describing the configuration commands.

The use of RF frequencies and maximum allowed RF power is limited by national regulations. The RC2000 is complying with the applicable directives within the European Union and meeting FCC and ARIB standards for US/Canada and Japan. The module complies also with most other regulations for license-free use world-wide.

External PA and LNA control

Pin 23 and 24 can be used to control an external Power Amplifier (PA), external Low Noise Amplifier (LNA) and Transmit/Receive (T/R) switch. The control signals are active low logic level (0-VDD) digital outputs. The PA_EN signal is active (low) while the internal PA is on. The PA is on during transmitting mode. The LNA_EN signal is active (low) while the internal LNA is on.

RSSI

The module provide a digital Received Signal Strength Indicator (RSSI) through the 'S' command. The module returns an 8 bit character indicating the signal strength read as an instantaneous value (followed immediately by a second character which is the prompt ('>')). The signal strength can be used as an indication of fading margin, or as a carrier sense signal to avoid collisions.

Do note that if the signal strength for an incoming packet is to be measured, the 'S' command must be performed while the packet is being received. To simplify the test of a link, and avoid timing problems, the transmitter can be set to continuous transmission using the '2' test command, while the receiver use the 'S' command to read the signal strength.

The RSSI value is a 2's complement value and is a measure of the input power. To refer the measurement to actual input power, in dBm, use the following equation giving an approximate value:

$$P = RSSI - 45 \text{ [dBm]}$$

The offset (approximately -45 dB) may be found empirically in an actual application taking into account any loss in the antenna input.

Antenna Connection

The antenna shall be connected to the RF pin. The RF pin is matched to 50 Ohm. If the antenna connector is placed away from the module at the motherboard, the track between the RF pin and the connector should be a 50 Ohm transmission line.

Note: Although the RF output is designed for 50 Ohm load, it has been found that a 1.8 pF capacitor should be added at the RF output for improved spectrum shape, and thus improved link quality, for some antenna loads. The capacitor should be placed as close as possible to the RF output terminal from RF to ground. This capacitor could improve the spectrum quality as seen by deeper notch at the first null in the FSK spectrum. Since the antenna load varies significantly depending on surroundings and close objects, it is recommended to always include the shunt capacitor.

On a two layer board made of FR4 the width of a microstrip transmission line should be 1.8 times the thickness of the board, assuming a dielectric constant of 4.8. The line should be run at the top of the board, and the bottom side should be a ground plane.

Example: For a 1.6 mm thick FR4 board, the width of the trace on the top side should be 1.8 x 1.6 mm = 2.88 mm.

The simplest antenna to use is the quarter wave whip antenna. A quarter wave whip antenna above a ground plane yields 37 Ohm impedance and a matching circuit for 50 Ohm are usually not required. A quarter wave antenna, like a piece of wire normal to ground plane should have a length equivalent to 95% of the free space wavelength.

A PCB antenna can be made as a copper track where the ground plane is removed on the back side. The rest of the PCB board should have a ground plane as large as possible, preferably as large (in one dimension) as the antenna itself, to make it act as a counterweight to the antenna. A quarter wavelength antenna on a PCB must be shorter than the wire antenna due to the influence of the dielectric material of the PCB. The length reduction depends on the PCB thickness and material, as well as how close to the edge of the board the antenna is placed. Typical reduction is to 75-90 % but must be found empirically.

If, for space reasons, the track is made even shorter than the resonating quarter of a wavelength, the antenna should be matched to 50 ohms using a series inductor and a shunt capacitor.

The length of a quarter-wave antenna is given in the table below.

Frequency [MHz]	Length of whip antenna [cm]	Length of PCB track [cm]
2450	2.9	2.25 – 2.7

PCB Layout Recommendations

The recommended layout pads for the module are shown in the figure below. All dimensions are in thousands of an inch (mil). The circle in upper left corner is an orientation mark only, and should not be a part of the copper pattern.
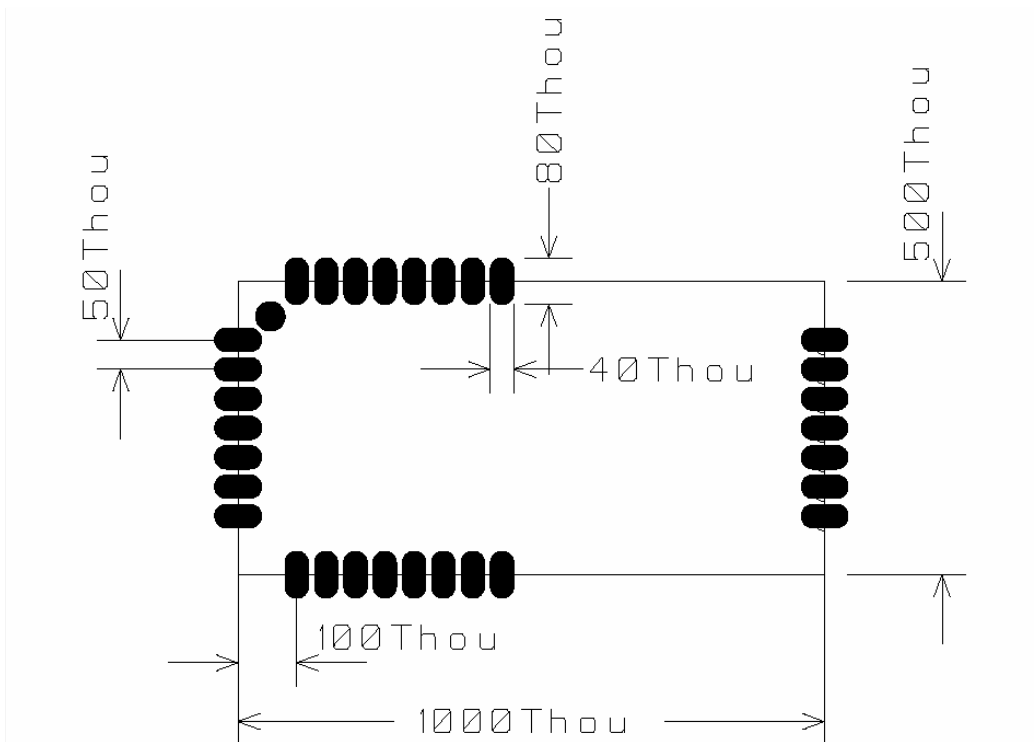

A PCB with two or more layers and with a solid ground plane in one of the inner- or bottom layer(s) is recommended. All GND-pins of the module shall be connected to this ground plane with vias with shortest possible routing, one via per GND-pin.

On the back side of the module there are several test pads. These test pads shall not be connected, and the area underneath the module should be covered with solder resist. If any routing or vias is required under the module, the routing and vias must be covered with solder resist to prevent short circuiting of the test pads. It is recommended that vias are tented.

Reserved pins should be soldered to the pads but the pads must be left floating.

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Mechanical Dimensions
The module size is 12.7 x 25.4 x 3.5 mm.
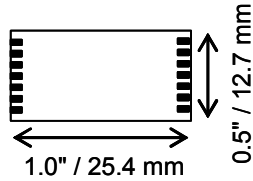
Carrier Tape and Reel Specification
Carrier tape and reel is in accordance with EIA Specification 481.

| Tape width	Component pitch	Hole pitch	Reel diameter	Units per reel
44 mm	16 mm	4 mm	13"	Max 1000

Soldering Profile Recommendation
JEDEC standard IEC/JEDEC J-STD-020B (page 11 and 12), Pb-Free Assembly is recommended.

The standard requires that the heat dissipated in the "surroundings" on the PCB is taken into account. The peak temperature should be adjusted so that it is within the window specified in the standard for the actual motherboard.

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RC2000

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply voltage, VCC	-0.3	5.5	V
Voltage on any pin	-0.3	5.5	V
Input RF level		10	dBm
Storage temperature	-50	150	°C
Operating temperature	-30	85	°C
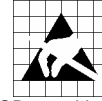
Caution ! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

Under no circumstances the absolute maximum ratings given above should be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Electrical Specifications

T=25°C, VCC = 3.0V if nothing else stated.

Parameter	Min	Typ.	Max	Unit	Condition / Note
Operating frequency	2400		2483	MHz	
Number of channels		83			
Input/output impedance		50		Ohm	
Data rate (programmable)	10	250	1000	kbit/s	
Frequency stability			+/-40	ppm	Over operating temperature range
Transmit power Power level 1: 2: 3: 4: 5:		-25 -15 -10 -5 -3		dBm	
Harmonics, 2nd and 3rd		< -55		dBm	
Spurious emission, TX 30-1000 MHz 1 – 12.75 GHz 1.8 – 1.9 GHz 5.15 – 5.33 GHz			-36 -30 -47 -47	dBm	Complies with EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T66
Sensitivity 10 kbit/s 250 kbit/s 1 Mbit/s		-101 -91 -87		dBm	BER = 0.1%
Adjacent channel rejection, 250 kbit/s 1 Mbit/s		12 0		dB	1 MHz spacing. BER = 0.1%
Image channel rejection, 250 kbit/s 1 Mbit/s		39 21		dB	2 MHz offset. BER = 0.1%, wanted signal 10 dB above sensitivity level
Blocking / Interferer rejection / desensitization +/- 5 MHz +/- 10 MHz +/- 20 MHz +/- 50 MHz	-50 -45 -40 -30	-52 -55 -56 -59		dBm	Wanted signal 3 dB above sensitivity level, modulated interferer. BER=0.1% Minimum numbers corresponds to class 2 receiver requirements in EN 300 440 class 2 .
Saturation		3		dBm	BER = 0.1%

Spurious emission, RX 30 – 1000 MHz 1 – 12.75 GHz			-57 -47	dBm	Complies with EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T66
Supply voltage	2.8		5.5	V	
Supply voltage rise time			150	us	If appropriate rise time can not be guaranteed, the RESET pin should be activated after supply voltage is stable.
Current consumption, CONFIG RX		2.1 25.2		mA	Apply over entire supply voltage range
Current consumption, TX Power level 1: -27 dBm 2: -17 dBm 3: -12 dBm 4: -7 dBm 5: -3 dBm		10.7 11.8 12.9 15.1 18.5		mA	Apply over entire supply voltage range
Current consumption, SLEEP		85	**150**	µA	Max value in bold apply over the entire temperature and supply voltage range
Current consumption, OFF		0.003	**1.5**	µA	Max value in bold apply over the entire temperature and supply voltage range
Digital I/O Input logic level, low Input logic level, high Output logic level, low (1µA) Output logic level, high(-1µA)	1.7 0 2.6		0.7 5.5 0.1 2.7	V	RXEN, TXEN, CONFIG, TXD and RXD have internal 100 kΩ series resistors. No internal pull-ups. Outputs should not be loaded resistively.
RESET pin Input logic level, low Input logic level, high	1.7		0.7 2.7	V	Internal 100 kΩ pull-up resistor to VDD
ON/OFF pin Input logic level, low Input logic level, high	1.4		0.4 VCC	V	No internal pull-up resistor
UART Baud Rate tolerance		+/- 2		%	UART receiver and transmitter
Configuration memory write cycles	10 000	100 000			The guaranteed number of write cycles using the 'M' command is limited

Regulatory Compliance Information

The use of RF frequencies and maximum allowed RF power is limited by national regulations. The RC2000 have been designed to comply with the R&TTE directive 1999/5/EC.

According to R&TTE directives, it is the responsibility of Radiocrafts' customers to check that the host product (i.e. final product) is compliant with R&TTE essential requirements. The use of a CE marked radio module can avoid re-certification of the final product, provided that the end user respects the recommendations established by Radiocrafts. A Declaration of Conformity is available from Radiocrafts on request.

The RC2000 has been tested towards FCC regulations for license free operation under part 15. However, a final approval is required by FCC for the end product.

The RC2000 has been designed to comply with the requirements given by the Japanese ARIB STD-T66 for low power (short range) devices in the 2.4GHz range. However, it has not been assessed for conformity with the appropriate regulations. Users must assess and verify that their final product meets the appropriate specifications and to perform the required procedures for regulatory compliance.

The relevant regulations are subject to change. Radiocrafts AS do not take responsibility for the validity and accuracy of the understanding of the regulations referred above. Radiocrafts only guarantee that this product meets the specifications in this document. Radiocrafts is exempt from any responsibilities related to regulatory compliance.

Document Revision History

Document Revision	Changes
1.0	First release
1.1	Added pin description equivalent circuits Added new section and more information on Power on Reset and reset circuits Added soldering profile recommendation Added note on 2 stop-bits if CTS is used Corrected IDLE to CONFIG in current consumption in electrical characteristics Added UART baud rate tolerance specification Added configuration memory write cycle specification, and note in the text Added note on RSSI measurement is followed by a new prompt Added note on delay after channel-byte in timing information Added new section and more information on I/O pin interfaces Added more info on ON/OFF in pin description Added note on digital signal output level and level translators Added new section on regulatory compliance information Clarified awakening from SLEEP mode using RXEN and TXEN Clarified Product Status and Definition Clarified PCB Layout Recommendations Note on load capacitance at antenna output added
1.11	Updated figure for application circuit
1.12	Corrected pin 23 Pin Name from CCA/PA_EN to PA_EN

Product Status and Definitions

Current Status	Data Sheet Identification	Product Status	Definition
	Advance Information	Planned or under development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
	Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. Radiocrafts reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
X	**No Identification Noted**	**Full Production**	**This data sheet contains final specifications. Radiocrafts reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.**
	Obsolete	Not in Production	This data sheet contains specifications on a product that has been discontinued by Radiocrafts. The data sheet is printed for reference information only.

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Radiocrafts AS believes the information contained herein is correct and accurate at the time of this printing. However, Radiocrafts AS reserves the right to make changes to this product without notice. Radiocrafts AS does not assume any responsibility for the use of the described product; neither does it convey any license under its patent rights, or the rights of others. The latest updates are available at the Radiocrafts website or by contacting Radiocrafts directly.

As far as possible, major changes of product specifications and functionality, will be stated in product specific Errata Notes published at the Radiocrafts website. Customers are encouraged to check regularly for the most recent updates on products and support tools.

Trademarks

RC232™ is a trademark of Radiocrafts AS. The RC232™ Embedded RF Protocol is used in a range of products from Radiocrafts. The protocol handles host communication, data buffering, error check, addressing and broadcasting. It supports point-to-point, point-to-multipoint and peer-to-peer network topologies.

All other trademarks, registered trademarks and product names are the sole property of their respective owners.

Life Support Policy

This Radiocrafts product is not designed for use in life support appliances, devices, or other systems where malfunction can reasonably be expected to result in significant personal injury to the user, or as a critical component in any life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness. Radiocrafts AS customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Radiocrafts AS for any damages resulting from any improper use or sale.

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