DALC208

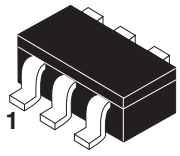
ASD™

LOW CAPACITANCE DIODE ARRAY

MAIN APPLICATIONS

Where ESD and/or over and undershoot protection for datalines is required :

- Sensitive logic input protection
- Microprocessor based equipment
- Audio / Video inputs
- Portable electronics
- Networks
- ISDN equipment
- USB interface



SOT23-6L
(Plastic)

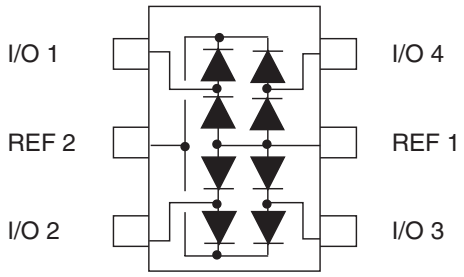
FEATURES

- Protection of 4 lines
- Peak reverse voltage: V_{RRM} = 9 V per diode
- Very low capacitance per diode: C < 5 pF
- Very low leakage current: I_R < 1 µA

Table 1: Order Code

Part Number	Marking
DALC208SC6	DALC

Figure 1: Functional Diagram



DESCRIPTION

The DALC208SC6 diode array is designed to protect components which are connected to data and transmission lines from overvoltages caused by electrostatic discharge (ESD) or other transients. It is a rail-to-rail protection device also suited for overshoot and undershoot suppression on sensitive logic inputs.

The low capacitance of the DALC208SC6 prevents from significant signal distortion.

BENEFITS

- Cost-effectiveness compared to discrete solution
- High efficiency in ESD suppression
- No significant signal distortion thanks to very low capacitance
- High reliability offered by monolithic integration
- Lower PCB area consumption versus discrete solution

COMPLIES WITH THE FOLLOWING STANDARDS:

- IEC61000-4-2 level 4
- MIL STD 883C-Method 3015-6: class3 (Human Body Model)

TM: ASD is a trademark of STMicroelectronics.

Table 2: Absolute Maximum Ratings (T_{amb} = 25°C)

Symbol	Parameter	Value	Unit
V_{PP}	IEC61000-4-2, air discharge IEC61000-4-2, contact discharge	15 8	kV
V_{RRM}	Peak reverse voltage per diode	9	V
ΔV_{REF}	Reference voltage gap between V_{REF2} and V_{REF1}	9	V
V_{In} max.	Maximum operating signal input voltage	V_{REF2}	V
V_{In} min.	Minimum operating signal input voltage	V_{REF1}	V
I_F	Continuous forward current (single diode loaded)	200	mA
I_{FRM}	Repetitive peak forward current (t_p = 5 ms, F = 50 kHz)	700	mA
I_{FSM}	Surge non repetitive forward current - rectangular waveform (see curve on figure 3) t_p = 2.5 µs t_p = 1 µs t_p = 100 µs	 6 2 1	A
T_{stg} T_j	Storage temperature range Maximum junction temperature	-55 to + 150 150	°C °C

Table 3: Thermal resistances

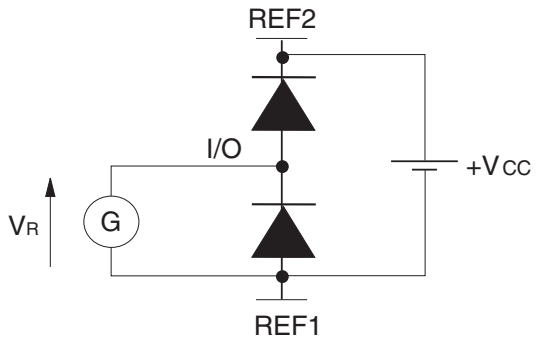
Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient (note 1)	500	**°C/W**

Note 1: device mounted on FR4 PCB with recommended footprint dimensions.

Table 4: Electrical Characteristics (T_{amb} = 25°C)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_F	Forward voltage	I_F = 50 mA		1.2	V
I_R	Reverse leakage current per diode	V_R = 5 V		1	µA
C	Input capacitance between Line and GND	see figure 2	7	10	pF

Figure 2: Input capacitance measurement



- REF1 connected to GND
- REF2 connected to +Vcc
- Input applied :
  Vcc = 5V, Vsign = 30 mV, F = 1 MHz

Figure 3: Maximum non-repetitive peak forward current versus rectangular pulse duration (T_j initial = 25°C)

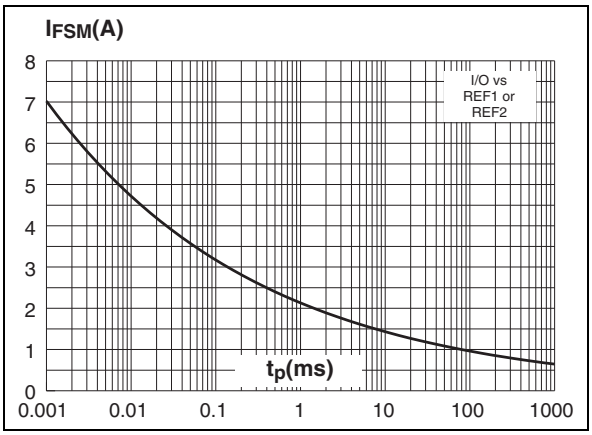


Figure 4: Reverse clamping voltage versus peak pulse current (T_j initial = 25°C), typical values. Rectangular waveform t_p = 2.5 ms

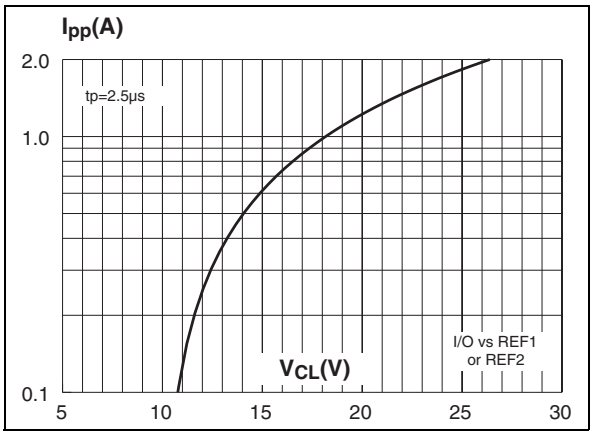


Figure 5: Variation of leakage current versus junction temperature (typical values)

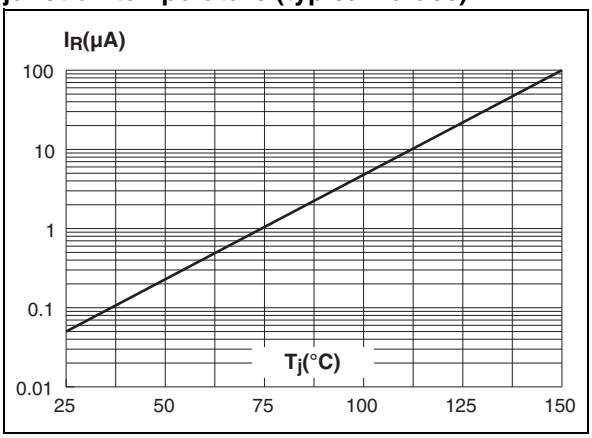


Figure 6: Input capacitance versus reverse applied voltage (typical values)

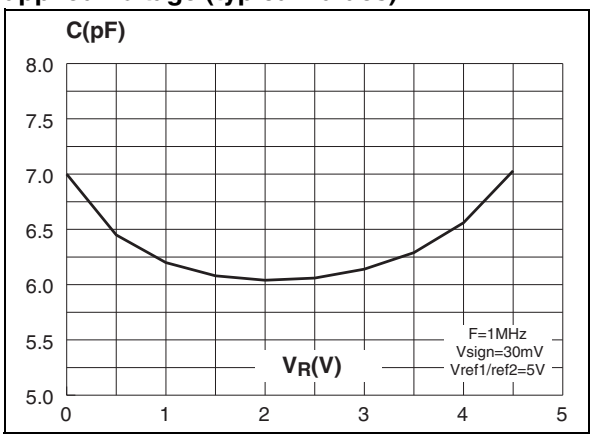
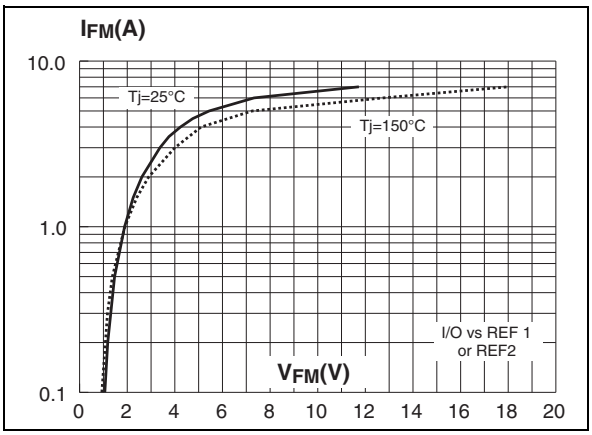


Figure 7: Peak forward voltage drop versus peak forward current (typical values). Rectangular waveform t_p = 2.5 ms



TECHNICAL INFORMATION

1. SURGE PROTECTION

The DALC208SC6 is particularly optimized to perform surge protection based on the rail to rail topology. The clamping voltage V_{CL} can be calculated as follow :

$$V_{CL}+ = V_{REF2} + V_F \text{ for positive surges}$$
$$V_{CL}- = V_{REF1} - V_F \text{ for negative surges}$$

with: $V_F = V_T + R_d.I_p$
(V_F forward drop voltage) / (V_T forward drop threshold voltage)

According to the curve figure 7 on page 3, we assume that the value of the dynamic resistance of the clamping diode is typically $R_d = 0.7\Omega$ and $V_T = 1.2V$.
For an IEC61000-4-2 surge Level 4 (Contact Discharge: V_g=8kV, R_g=330Ω), V_{REF2} = +5V, V_{REF1} = 0V, and if in first approximation, we assume that : $I_p = V_g / R_g$ ′ 24A.
So, we find:

$V_{CL}+$ ′ +23V
$V_{CL}-$ ′ -18V

Note: the calculations do not take into account phenomena due to parasitic inductances.

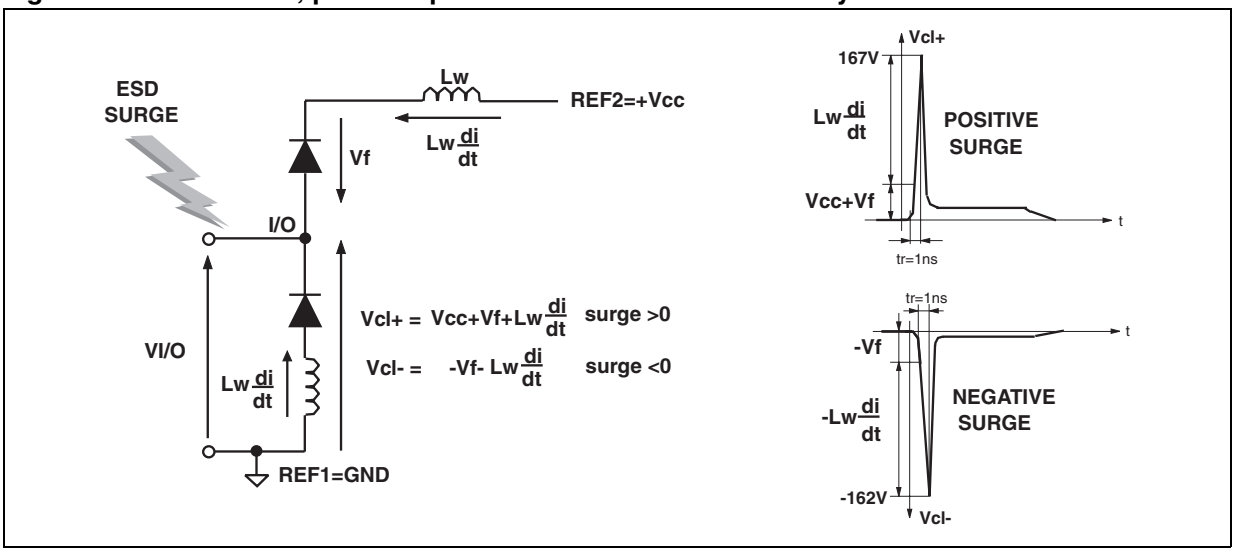
2. SURGE PROTECTION APPLICATION EXAMPLE

If we consider that the connections from the pin REF_2 to V_{CC} and from REF_1 to GND are done by two tracks of 10mm long and 0.5mm large; we assume that the parasitic inductances of these tracks are about 6nH. So when an IEC61000-4-2 surge occurs, due to the rise time of this spike (tr=1ns), the voltage V_{CL} has an extra value equal to Lw.dI/dt.
The dI/dt is calculated as: dI/dt = Ip/tr ′ 24 A/ns
The overvoltage due to the parasitic inductances is: Lw.dI/dt = 6 x 24 ′ 144V
By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be :

$V_{CL}+ = +23 + 144$ ′ 167V
$V_{CL}- = -18 - 144$ ′ -162V

We can reduce as much as possible these phenomena with simple layout optimization.
It's the reason why some recommendations have to be followed (see paragraph "How to ensure a good ESD protection").

Figure 8: ESD behavior; parasitic phenomena due to unsuitable layout



3. HOW TO ENSURE A GOOD ESD PROTECTION

While the DALC208SC6 provides a high immunity to ESD surge, an efficient protection depends on the layout of the board. In the same way, with the rail to rail topology, the track from the V_{REF2} pin to the power supply $+V_{CC}$ and from the V_{REF1} pin to GND must be as short as possible to avoid overvoltages due to parasitic phenomena (see figure 8).
It's often harder to connect the power supply near to the DALC208SC6 unlike the ground thanks to the ground plane that allows a short connection.

To ensure the same efficiency for positive surges when the connections can't be short enough, we recommend to put close to the DALC208SC6, between V_{REF2} and ground, a capacitance of 100nF to prevent from these kinds of overvoltage disturbances (see figure 9).
The add of this capacitance will allow a better protection by providing during surge a constant voltage.
The figures 10, 11 and 12 show the improvement of the ESD protection according to the recommendations described above.

Figure 9: ESD behavior: optimized layout and add of a capacitance of 100nF

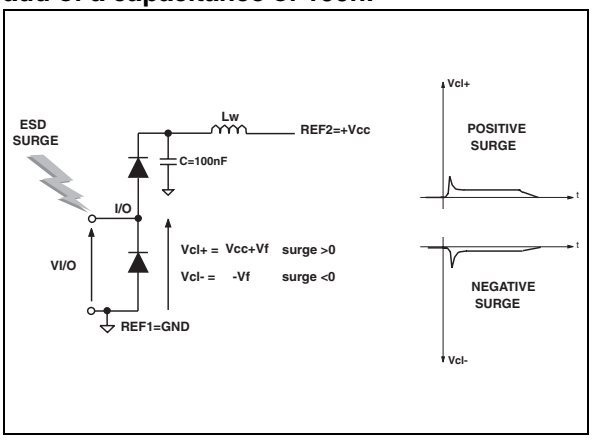


Figure 10: ESD behavior: measurements conditions (with coupling capacitance)

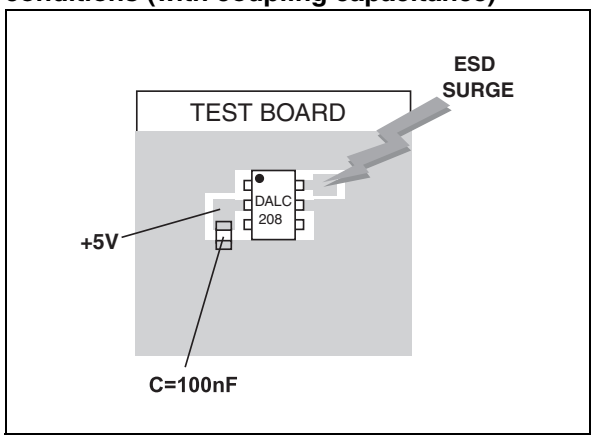


Figure 11: Remaining voltage after the DALC208SC6 during positive ESD surge

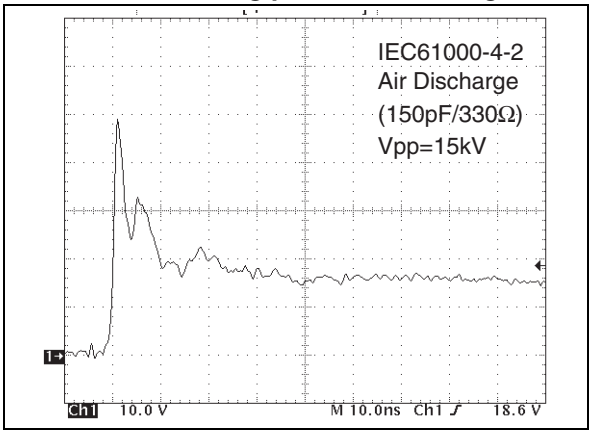
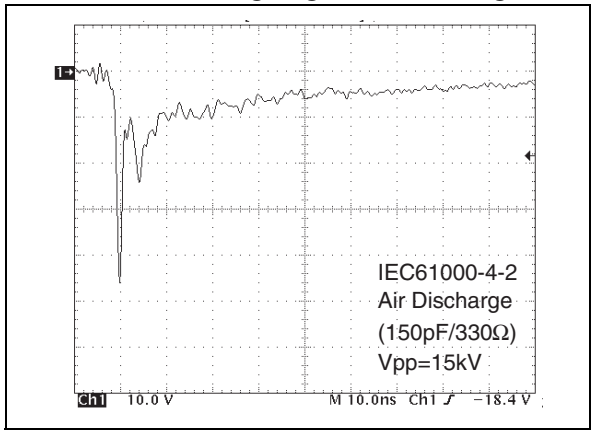


Figure 12: Remaining voltage after the DALC208SC6 during negative ESD surge



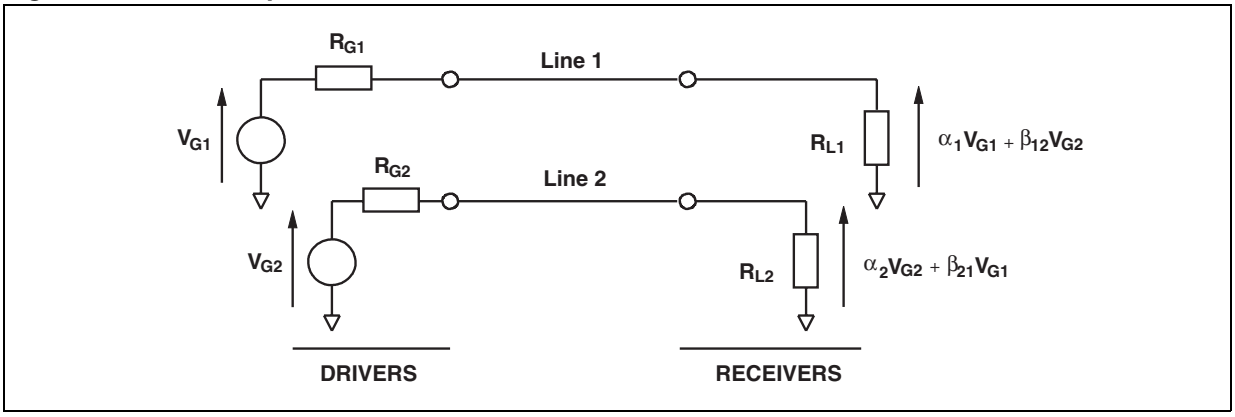
IMPORTANT:
A main precaution to take is to put the protection device closer to the disturbance source (generally the connector).

Note: The measurements have been done with the DALC208SC6 in open circuit.

4. CROSSTALK BEHAVIOR

4.1. Crosstalk phenomena

Figure 13: Crosstalk phenomena



The crosstalk phenomena are due to the coupling between 2 lines. The coupling factor (β12 or β21) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ). The following chapters give the value of both digital and analog crosstalk.

4.2. Digital crosstalk

Figure 14: Digital crosstalk measurements

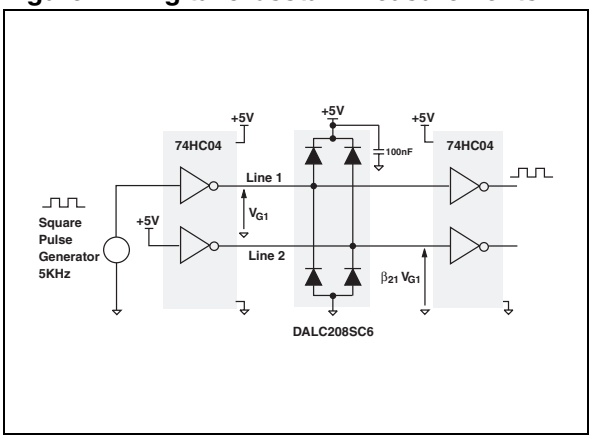


Figure 15: Digital crosstalk results

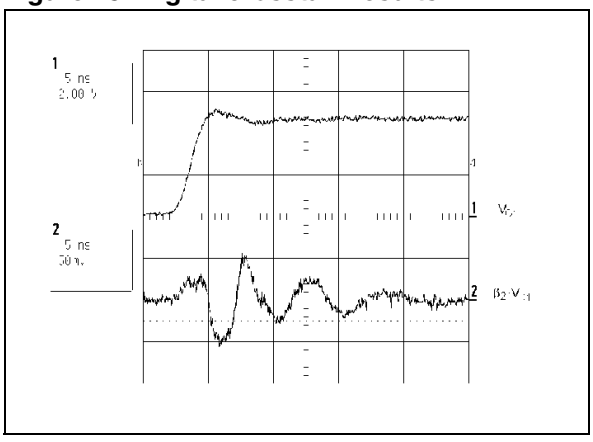


Figure 14 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure 15 shows that in such a condition: signal from 0V to 5V and a rise time of 5 ns, the impact on the disturbed line is less than 100mV peak to peak. No data disturbance was noted on the concerned line. The same results were obtained with falling edges.

Note: The measurements have been done in the worst case i.e. on two adjacent cells (I/O1 & I/O4).

4.3 Analog crosstalk

Figure 16: Analog crosstalk measurements

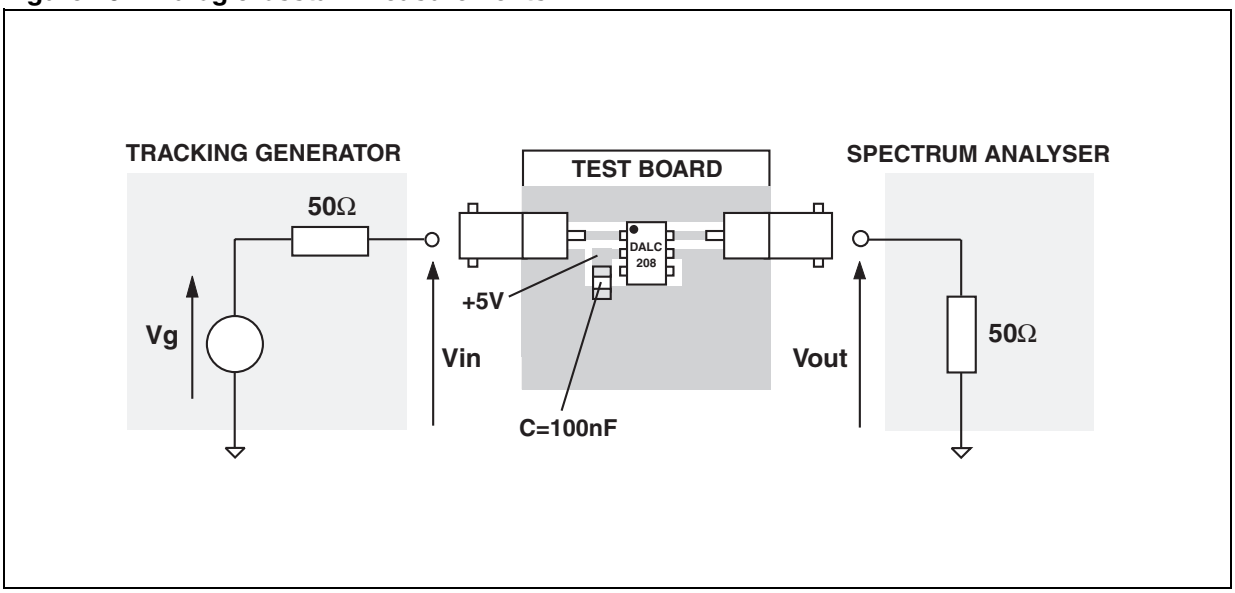


Figure 16 gives the measurement circuit for the analog application. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -45 dBm (please see figure 17).

Figure 17: Analog crosstalk results

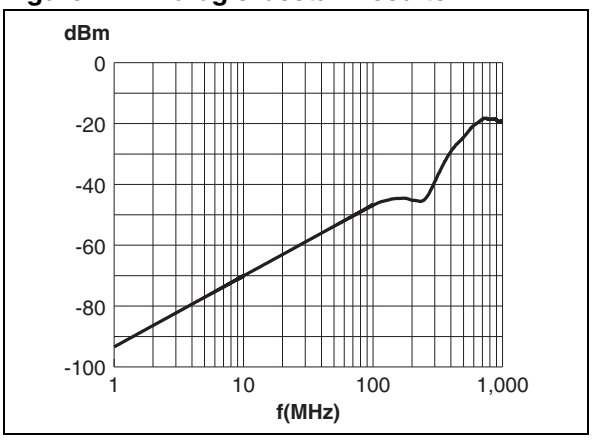
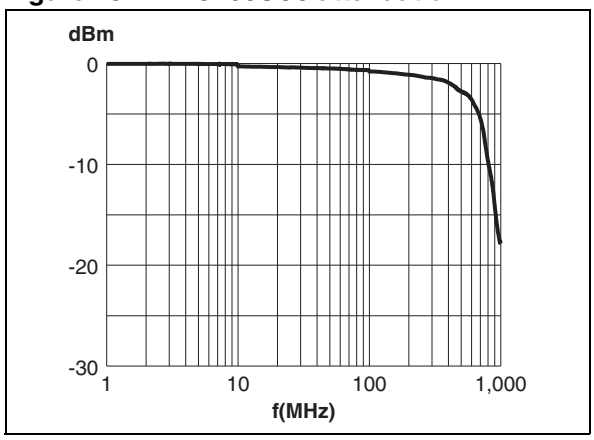


Figure 18: DALC208SC6 attenuation

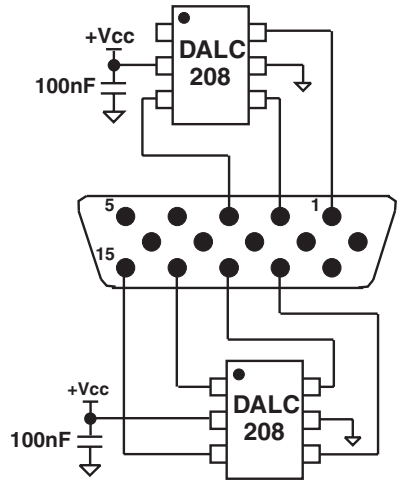


As the DALC208SC6 is designed to protect high speed data lines, it must ensure a good transmission of operating signals. The attenuation curve give such an information.

Figure 18 shows that the DALC208SC6 is well suitable for data line transmission up to 100 Mbit/s while it works as a filter for undesirable signals as GSM (900MHz).

5. APPLICATION EXAMPLES

Figure 19: Video line protection



Pin N°	Signal
1	RED VIDEO
2	GREEN VIDEO or COMPOSITE SYNC with GREEN VIDEO
3	BLUE VIDEO
4	GROUND
5	DDC (Display Data Channel) GROUND
6	RED GROUND
7	GREEN GROUND
8	BLUE GROUND
9	NC
10	SYNC GROUND
11	GROUND
12	SDA (Sérial Data)
13	HORIZONTAL SYNC or COMPOSITE SYNC
14	VERTICAL SYNC (VCLK)
15	SCL (Serial Clock)

Figure 20: T1/E1 protection

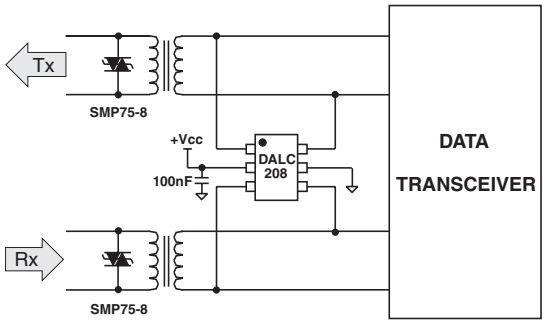


Figure 21: USB port protection

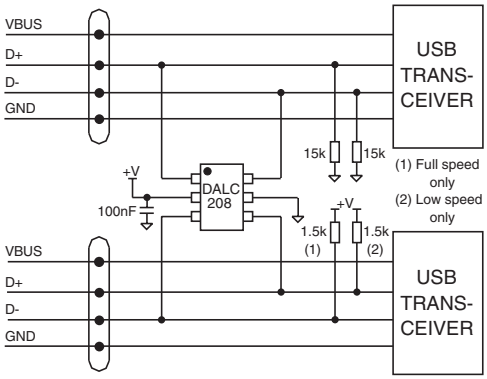
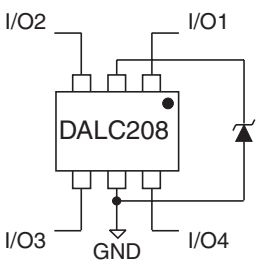


Figure 22: Another way to connect the DALC208SC6



Note It's absolutely necessary to connect the pin 5 (REF1) to GND !

6. PSPICE MODEL

Figure 23 shows the PSpice model of one DALC208SC6 cell. In this model, the diodes are defined by the PSpice parameters given in table 5.

Figure 23: PSpice model of one DALC208SC6 cell

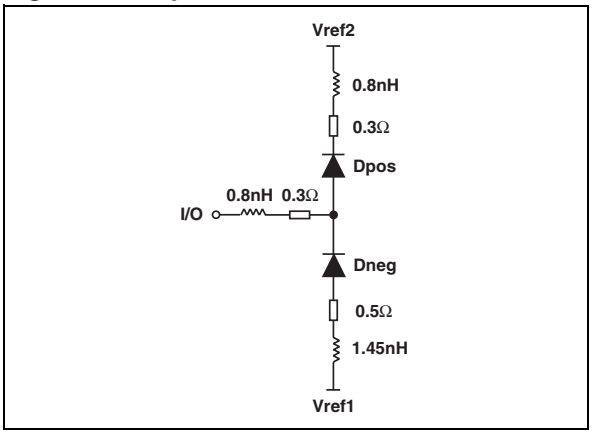


Table 5: PSpice parameters

	DPOS	DNEG
BV	9	9
CJO	7p	7p
IBV	1u	1u
IKF	28.357E-3	1000
IS	118.78E-15	5.6524E-9
ISR	100E-12	472.3E-9
M	0.3333	0.3333
N	1.3334	2.413
NR	2	2
RS	0.68377	0.71677
VJ	0.6	0.6

Note: This simulation model is available only for an ambient temperature of 27°C.
The simulations done (figures 24, 25 and 26) show that the PSpice model is close to the product behavior.

Figure 24: PSpice model simulation: surge > 0 IEC61000-4-2 contact discharge response

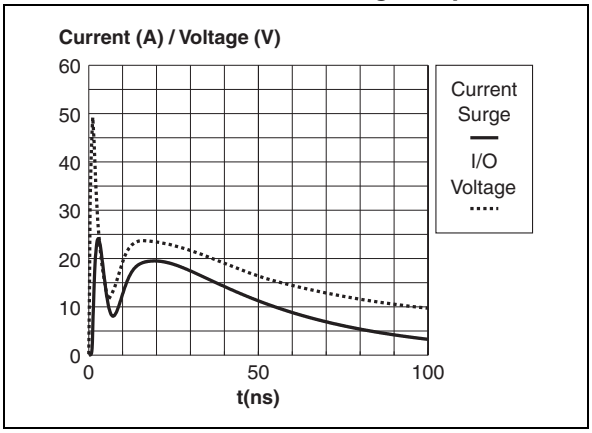


Figure 25: PSpice model simulation: surge < 0 IEC61000-4-2 contact discharge response

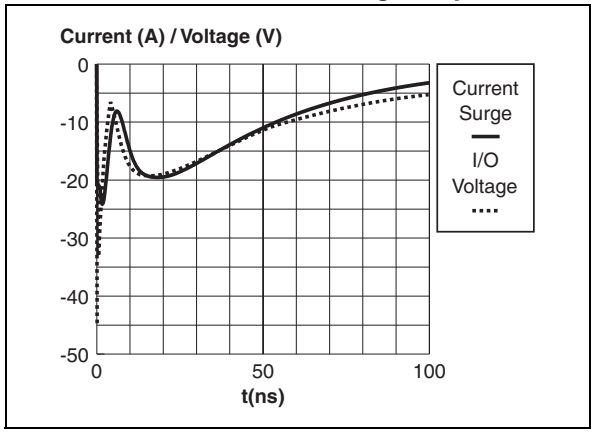


Figure 26: Attenuation comparison

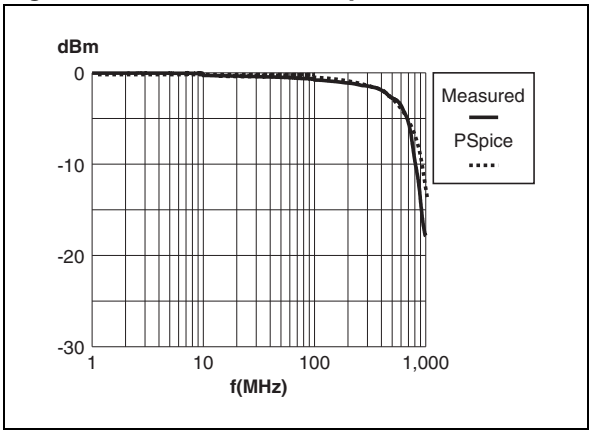
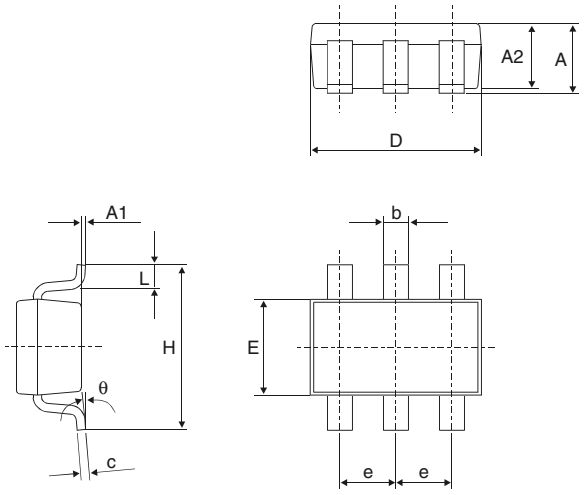


Figure 27: SOT23-6L Package Mechanical Data



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.10	0		0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.014		0.02
C	0.09		0.20	0.004		0.008
D	2.80		3.05	0.110		0.120
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ			10°			10°

Figure 28: Foot Print Dimensions (in millimeters)

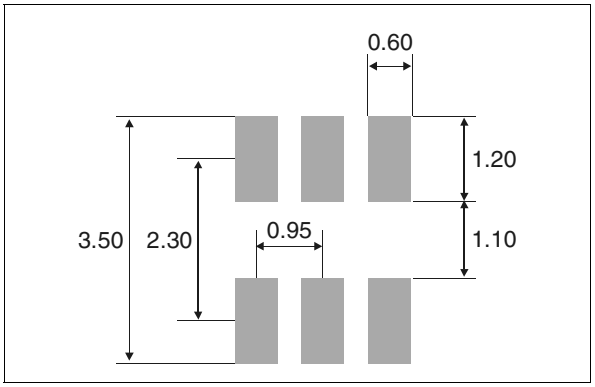


Table 6: Ordering Information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
DALC208SC6	DALC	SOT23-6L	16.7 mg	3000	Tape & reel

Table 7: Revision History

Date	Revision	Description of Changes
Feb-2002	5C	Last update.
28-Oct-2004	6	SOT23-6L package dimensions change for reference “D” from 3.0 millimeters (0.118 inches) to 3.05 millimeters (0.120 inches).