USBUFxxW6

A.S.D.™

EMI FILTER AND LINE TERMINATION FOR USB UPSTREAM PORTS

APPLICATIONS

EMI Filter and line termination for USB upstream ports on:
- USB Hubs
- PC peripherals

FEATURES

- Monolithic device with recommended line termination for USB upstream ports
- Integrated Rt series termination and Ct bypassing capacitors.
- Integrated ESD protection
- Small package size

DESCRIPTION

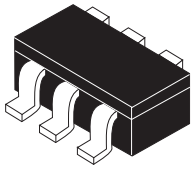
The USB specification requires upstream ports to be terminated with pull-up resistors from the D+ and D- lines to Vbus. On the implementation of USB systems, the radiated and conducted EMI should be kept within the required levels as stated by the FCC regulations. In addition to the requirements of termination and EMC compatibility, the computing devices are required to be tested for ESD susceptibility.

The USBUFxxW6 provides the recommended line termination while implementing a low pass filter to limit EMI levels and providing ESD protection which exceeds IEC61000-4-2 level 4 standard. The device is packaged in a SOT323-6L which is the smallest available lead frame package (50% smaller than the standard SOT23).

BENEFITS

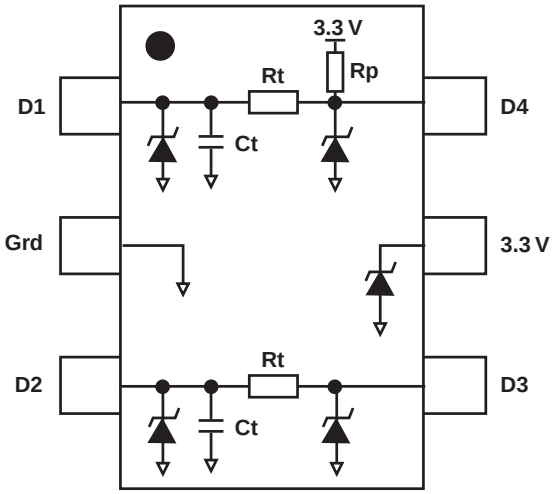
- EMI / RFI noise suppression
- Required line termination for USB upstream ports
- ESD protection exceeding IEC61000-4-2 level 4
- High flexibility in the design of high density boards
- Tailored to meet USB 1.1 standard

TM: ASD and TRANSIL are a trademarks of STMicroelectronics.



SOT323-6L

FUNCTIONAL DIAGRAM



	Rt	Rp	Ct
CODE 01	33Ω	1.5kΩ	47pF
CODE 02	22Ω	1.5kΩ	47pF
Tolerance	±10%	±10%	±20%

COMPLIES WITH THE FOLLOWING ESD STANDARDS:

IEC61000-4-2, level 4
±15 kV (air discharge)
±8 kV (contact discharge)

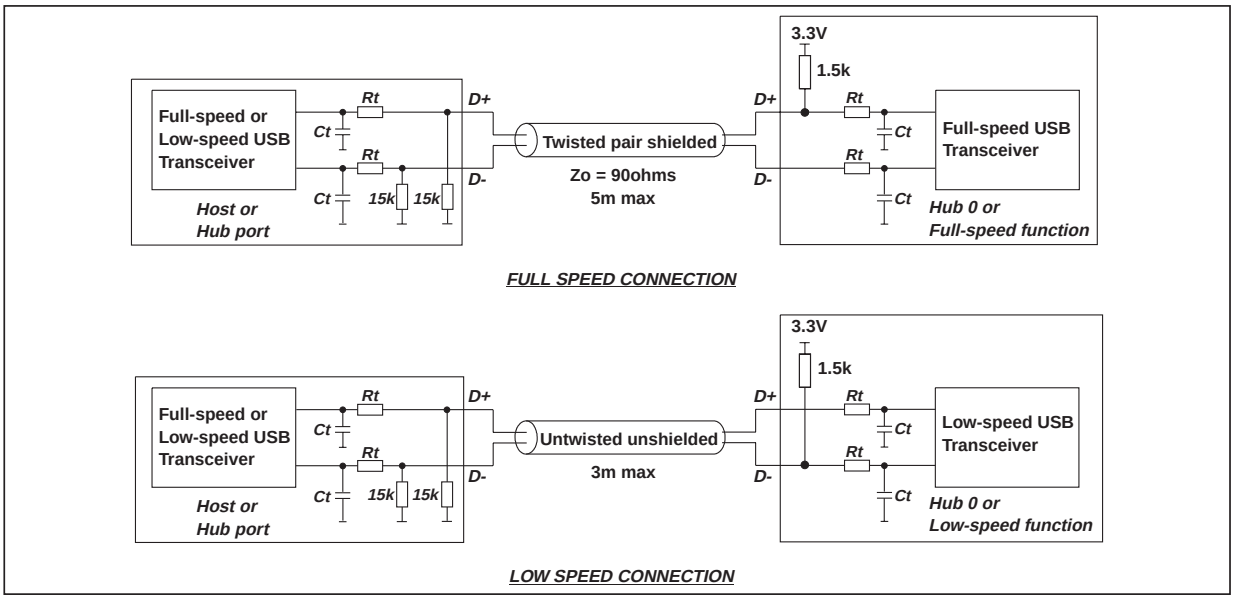
MIL STD 883E, Method 3015-7
Class 3 C = 100 pF R = 1500 Ω
3 positive strikes and 3 negative strikes (F = 1 Hz)

ABSOLUTE RATINGS (T_{amb} = 25°C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, air discharge ESD discharge IEC 61000-4-2, contact discharge ESD discharge - MIL STD 883E - Method 3015-7	±16 ±9 ±25	kV kV kV
T_j	Maximum junction temperature	150	°C
T_{stg}	Storage temperature range	- 55 to +150	°C
T_L	Lead solder temperature (10 second duration)	260	°C
T_{op}	Operating temperature range	0 to 70	°C
P_r	Power rating per resistor	100	mW

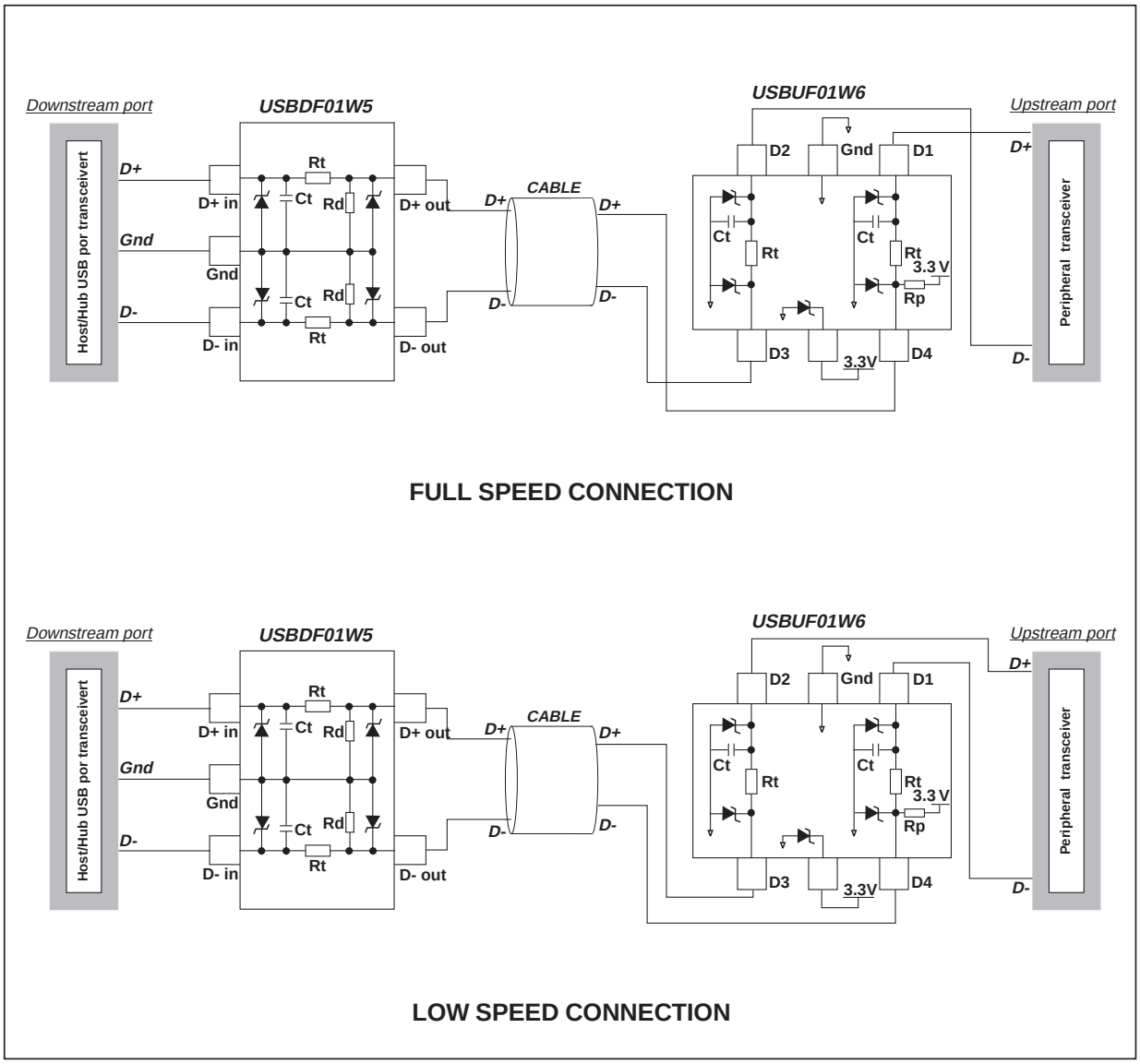
TECHNICAL INFORMATION

Fig. A1: USB Standard requirements



APPLICATION EXAMPLE

Fig. A2: Implementation of ST' solutions for USB ports



EMI FILTERING

Current FCC regulations requires that class B computing devices meet specified maximum levels for both radiated and conducted EMI.

- Radiated EMI covers the frequency range from 30MHz to 1GHz.
- Conducted EMI covers the 450kHz to 30MHz range.

For the types of devices utilizing the USB, the most difficult test to pass is usually the radiated EMI test. For this reason the USBUFxxW6 device is aiming to minimize radiated EMI.
The differential signal (D+ and D-) of the USB does not contribute significantly to radiated or conducted EMI because the magnetic field of both conductors cancels each other.
The inside of the PC environment is very noisy and designers must minimize noise coupling from the different sources. D+ and D- must not be routed near high speed lines (clocks spikes).
Induced common mode noise can be minimized by running pairs of USB signals parallel to each other and running grounded guard trace on each side of the signal pair from the USB controller to the USBUF device.
If possible, locate the USBUF device physically near the USB connectors. Distance between the USB controller and the USB connector must be minimized.
The 47pF (Ct) capacitors are used to bypass high frequency energy to ground and for edge control, and are placed between the driver chip and the series termination resistors (Rt). Both Ct and Rt should be placed as close to the driver chip as is practicable.

The USBUFxxW6 ensures a filtering protection against ElectroMagnetic and RadioFrequency Interferences thanks to its low-pass filter structure. This filter is characterized by the following parameters :

- cut-off frequency
- Insertion loss
- high frequency rejection.

Fig. A3: USBUFxxW6 typical attenuation curve.

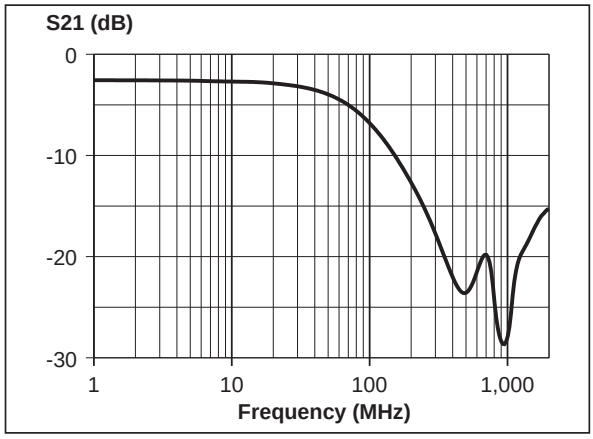
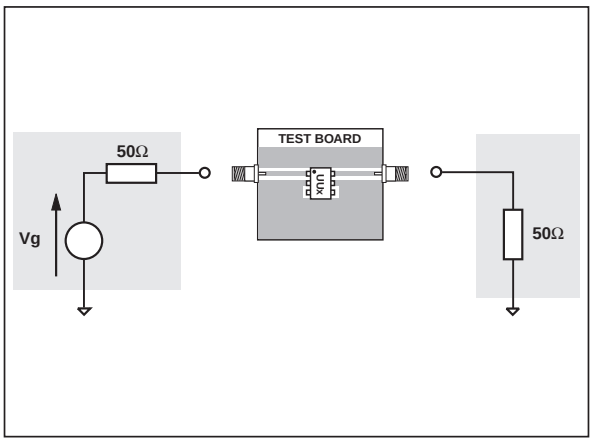


Fig. A4: Measurement configuration



ESD PROTECTION

In addition to the requirements of termination and EMC compatibility, computing devices are required to be tested for ESD susceptibility. This test is described in the IEC 61000-4-2 and is already in place in Europe. This test requires that a device tolerates ESD events and remains operational without user intervention.

The USBUFxxW6 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at :

$$V_{cl} = V_{BR} + R_d.I_{PP}$$

This protection function is splitted in 2 stages. As shown in figure A5, the ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor Rt. Such a configuration makes the output voltage very low at the output.

Fig. A5: USBUFxxW6 ESD clamping behavior

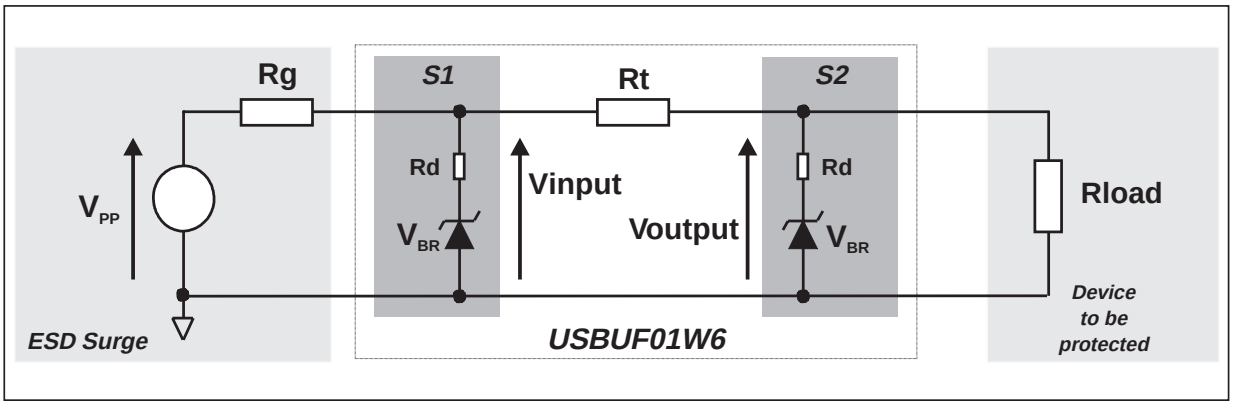
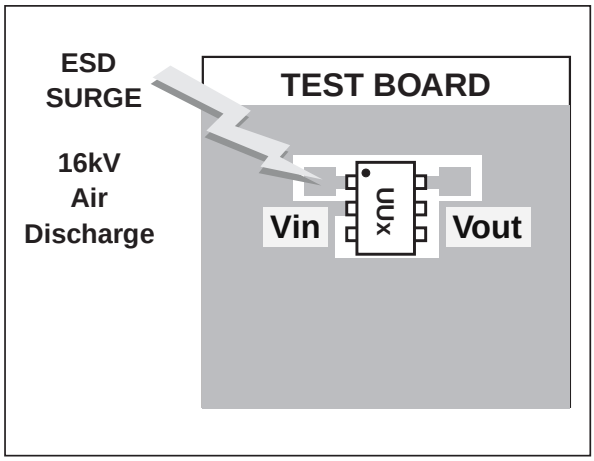


Fig. A6: Measurement board



To have a good approximation of the remaining voltages at both Vin and Vout stages, we give the typical dynamical resistance value Rd. By taking into account these following hypothesis : Rt>Rd, Rg>Rd and Rload>Rd, it gives these formulas:

$$Vinput = \frac{R_g.V_{BR} + R_d.V_g}{R_g}$$

$$Voutput = \frac{R_t.V_{BR} + R_d.Vinput}{R_t}$$

The results of the calculation done for Vg=8kV, Rg=330Ω (IEC61000-4-2 standard), V_{BR}=7V (typ.) and Rd = 1Ω (typ.) give:

Vinput = 31.2 V

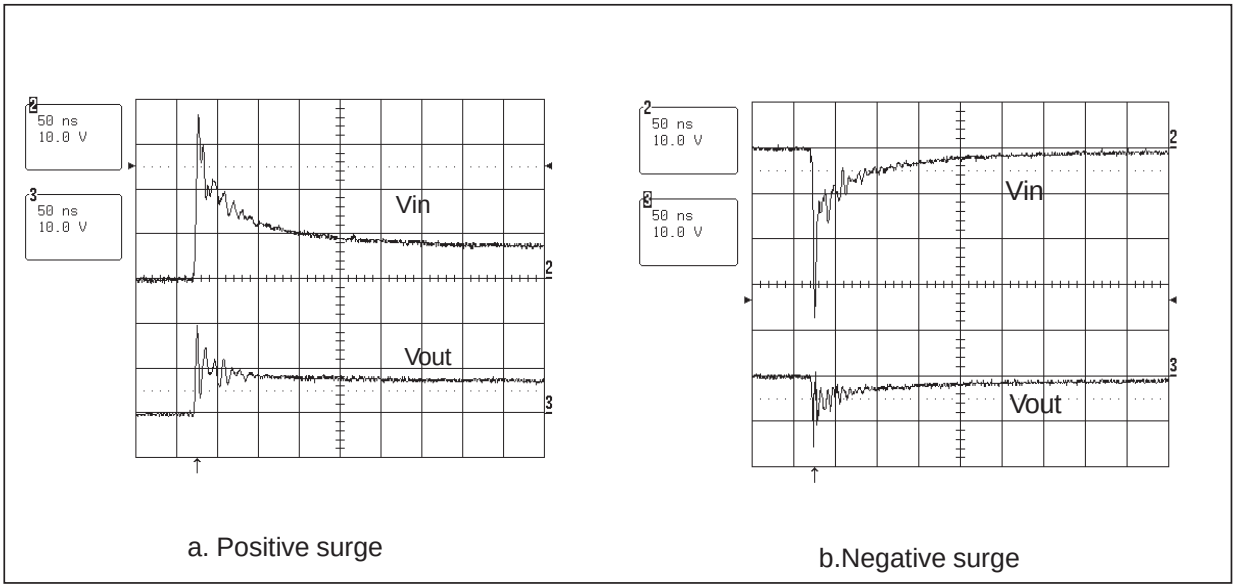
Voutput = 7.95 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the Vinput side. This parasitic effect is not present at the Voutput side due the low current involved after the resistance Rt.

The measurements done hereafter show very clearly (Fig. A7) the high efficiency of the ESD protection :

- no influence of the parasitic inductances on Voutput stage
- Voutput clamping voltage very close to V_{BR} (breakdown voltage) in the positive way and $-V_F$ (forward voltage) in the negative way

Fig. A7: Remaining voltage at both stages S1 (Vinput) and S2 (Voutput) during ESD surge.



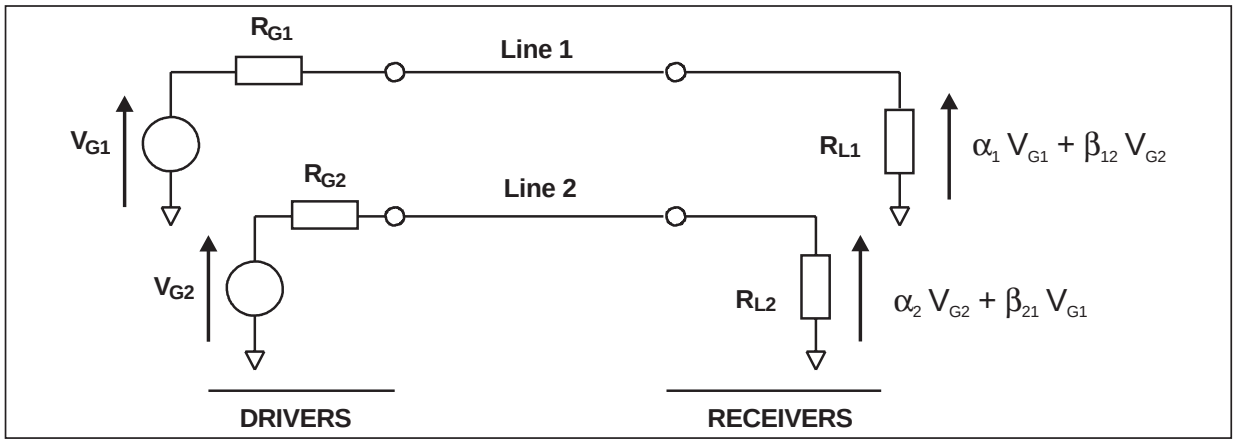
Please note that the USBUFxxW6 is not only acting for positive ESD surges but also for negative ones. For these kinds of disturbances it clamps close to ground voltage as shown in Fig. A7b.

LATCH-UP PHENOMENA

The early ageing and destruction of IC's is often due to latch-up phenomenon which is mainly induced by dV/dt. Thanks to its structure, the USBUFxxW6 provides a high immunity to latch-up phenomenon by smoothing very fast edges.

CROSSTALK BEHAVIOR

Fig. A8: Crosstalk phenomenon



The crosstalk phenomenon is due to the coupling between 2 lines. The coupling factor (β_{12} or β_{21}) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Fig. A9: Analog crosstalk measurements

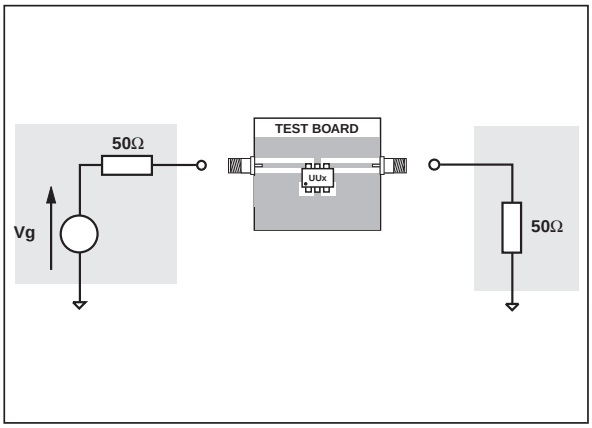


Fig. A10: Typical analog crosstalk results

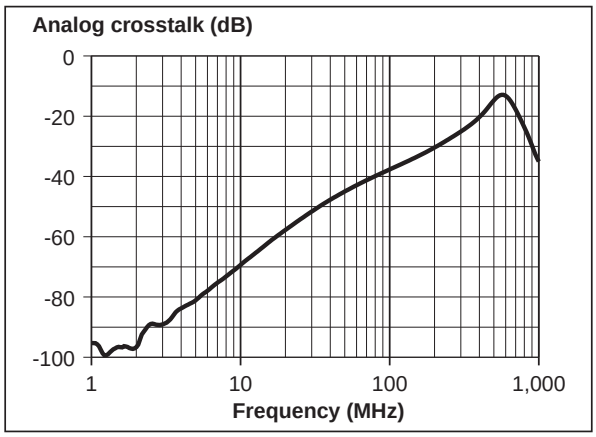


Figure A9 gives the measurement circuit for the analog crosstalk application. In figure A10, the curve shows the effect of the D+ cell on the D- cell. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -37dB.

Fig. A11: Digital crosstalk measurements configuration

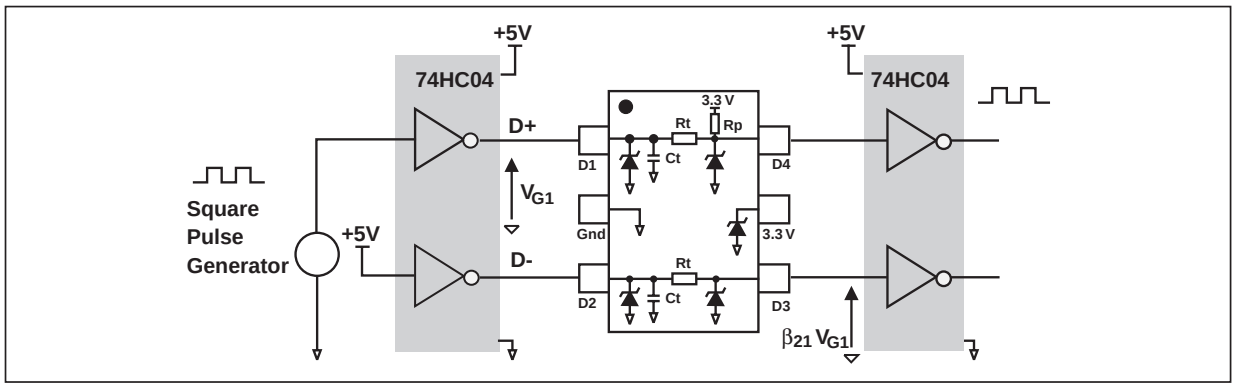


Figure A11 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Fig. A12: Digital crosstalk results

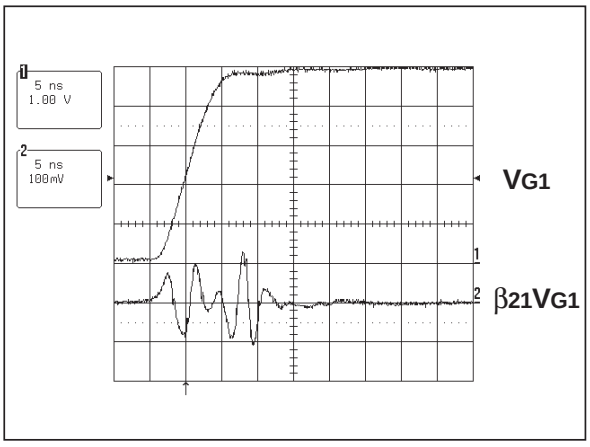


Figure A12 shows, with a signal from 0 to 5V and rise time of few ns, the impact on the disturbed line is less than 250mV peak to peak. No data disturbance was noted on the other line.The measurements performed with falling edges gives an impact within the same range.

TRANSITION TIMES

This low pass filter has been designed in order to meet the USB 1.1 standard requirements that implies the signal edges are maintained within the 4ns-20ns stipulated USB specification limits. To verify this point, we have measured the rise time of VD+ voltage (please refer to Fig. A13) with and without the USBUFxxW6 device.

Fig. A13: Typical rise and fall times: measurements configuration

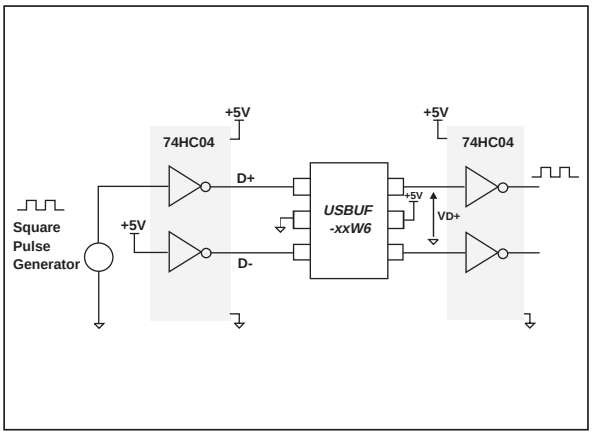


Fig. A14: Typical rise times with and without protection device

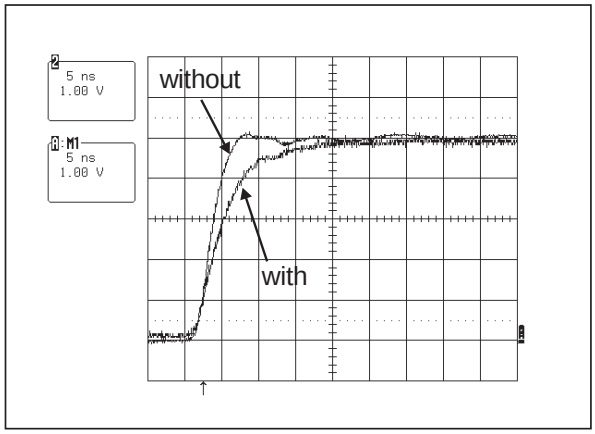


Figure A13 shows the circuit used to perform measurements of the transition times. In Figure A14, we see the results of such measurements:

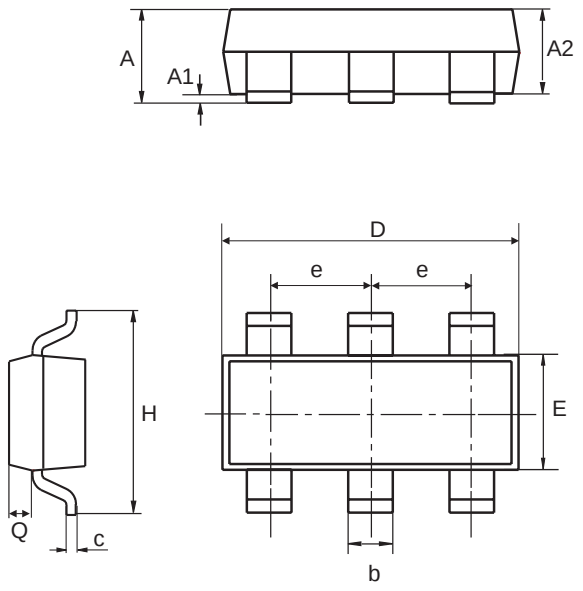
trise = 3.8ns driver alone
trise = 7.8ns with protection device

The adding of the protection device causes the rise time increase of roughly 4ns.

Note: Rise time has been measured between 10% and 90% of the signal (resp. 90% and 10%)

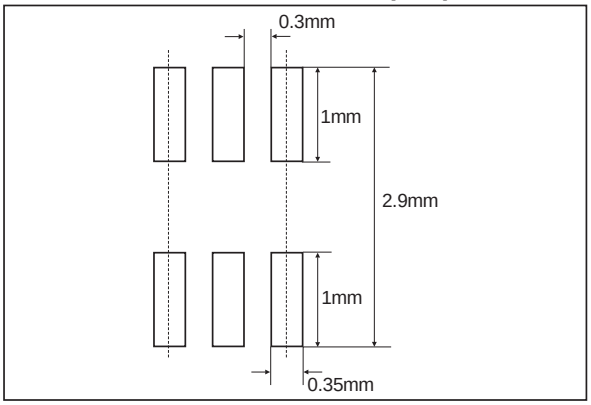
PACKAGE MECHANICAL DATA.

SOT323-6L



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.8	1.1	0.031	0.043
A1	0	0.1	0	0.004
A2	0.8	1	0.031	0.039
b	0.15	0.3	0.006	0.012
c	0.1	0.18	0.004	0.007
D	1.8	2.2	0.071	0.086
E	1.15	1.35	0.045	0.053
e	0.65 Typ.		0.025 Typ.	
H	1.8	2.4	0.071	0.094
Q	0.1	0.4	0.004	0.016

RECOMMENDED FOOTPRINT (mm)



MECHANICAL SPECIFICATIONS

Lead plating	Tin-lead
Lead plating thickness	5µm min 25µm max
Lead material	Sn / Pb (70% to 90%Sn)
Lead coplanarity	10µm max
Body material	Molded epoxy
Flammability	UL94V-0

MARKING

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
USBUF01W6	UU1	SOT323-6L	5.4 mg	3000	Tape & reel
USBUF02W6	UU2	SOT323-6L	5.4 mg	3000	Tape & reel