AN-991 Line Driving and System Design

Literature Number: SNLA043

Line Driving and System Design

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Application Note 991
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INTRODUCTION

Successful high-speed system design is dependent on careful system timing design and good board layout. The pitfalls are many and varied, and this section addresses some of those problem areas and simplifies the design requirements. All systems must interconnect signals either by short lines on printed circuit board, long lines on a backplane, twisted pair cables, or coaxial cables, etc. At high frequency, all of these mediums must be treated as transmission lines. Two properties of transmission lines, characteristic impedance (Z_O) and propagation delay (t_{PD}), are of concern. Transmission lines store energy, the magnitude of which is dependent on line length, impedance, applied voltage and source impedance. This stored energy must be dissipated by the terminating device and may couple to other circuits by crosstalk. The effects of termination on line reflection and crosstalk are discussed, as well as good board layout practices.

TRANSMISSION LINE CONCEPTS

The interactions between wiring and circuitry in high-speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuit, normalized pulse amplitudes are used in sample waveforms and calculations.

SIMPLIFYING ASSUMPTIONS

For the great majority of interconnections in digital systems, resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

CHARACTERISTIC IMPEDANCE

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic impedance Z_O. Whereas quiescent conditions on the line are determined by the circuits and terminations, Z_O is the ratio of transient voltage to transient current passing by a point on the line when a signal change or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows:

$$\frac{V}{I} = Z_O = \sqrt{\frac{L_O}{C_O}} \qquad \textbf{(E9-1)}$$

where L_O = inductance per unit length, and C_O = capacitance per unit length. Z_O is in ohms, L_O in Henries, and C_O in Farads.

PROPAGATION VELOCITY

Propagation velocity (ν) and its reciprocal, delay per unit length (δ), can also be expressed in terms of L_O and C_O. A consistent set of units is nanoseconds, microHenries and picoFarads, with a common unit of length.

$$\nu = \frac{1}{\sqrt{L_O C_O}} \quad \delta = \sqrt{L_O C_O} \qquad \textbf{(E9-2)}$$

Equations 9-1 and 9-2 provide a convenient means of determining the L_O and C_O of a line when delay, length and impedance are known. For a length l and delay T, δ is the ratio T/l. To determine L_O and C_O, combine Equations 9-1 and 9-2.

$$L_O = \delta Z_O \qquad \textbf{(E9-3)}$$

$$C_O = \frac{\delta}{Z_O} \qquad \textbf{(E9-4)}$$

More formal treatments of transmission line characteristics, including loss effects, are available from many sources.

TERMINATION AND REFLECTION

A transmission line with a terminating resistor is shown in *Figure 9-1*. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_O.

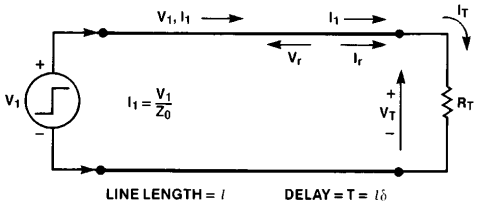

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FIGURE 9-1.

If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law,

always prevail at R_T. From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T had been connected directly across the terminals of the generator.

From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T.

When R_T is not equal to Z_O, the initial current starting down the line is still determined by V_1 and Z_O but the final steady state current, after all reflections have died out, is determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T. Therefore, at the instant the initial wave arrives at R_T, another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This reflected wave, indicated by V_r and I_r in *Figure 9-1*, starts to return toward the generator. Applying Kirchoff's laws to the end of the line at the instant the initial wave arrives results in the following:

(E9-5) $$I_1 + I_r = I_T = \text{Current into } R_T$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true:

$$V_1 + V_r = V_T$$

$$\text{thus} \quad I_T = \frac{V_T}{R_T} = \frac{V_1 + V_r}{R_T}$$

$$\text{also} \quad I_1 = \frac{V_1}{Z_O} \text{ and } I_r = -\frac{V_r}{Z_O}$$

(E9-6)

with the minus sign indicating that V_r is moving toward the generator.

Combining the foregoing relationships algebraically and solving for V_r yields a simplified expression in terms of V_1, Z_O and R_T.

$$\frac{V_1}{Z_O} - \frac{V_r}{Z_O} = \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T}$$

$$V_1\left(\frac{1}{Z_O} - \frac{1}{R_T}\right) = V_r\left(\frac{1}{R_T} + \frac{1}{Z_O}\right)$$

(E9-7) $$V_r = V_1\left(\frac{R_T - Z_O}{R_T + Z_O}\right) = \rho_L V_1$$

The term in parentheses is called the coefficient of reflection (ρ_L). With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between -1 and $+1$ respectively. The subscript L indicates that ρ_L refers to the coefficient at the load end of the line.

Equation 9-7 expresses the amount of voltage sent back down the line, and since

$$V_T = V_1 + V_r$$

$$\text{then} \quad V_T = V_1(1 + \rho_L)$$

(E9-8)

V_T can also be determined from an expression which does not require the preliminary step of calculating ρ_L. Manipulating $(1 + \rho_L)$ results in

$$1 + \rho_L = 1 + \frac{R_T - Z_O}{R_T + Z_O} = 2\left(\frac{R_T}{R_T + Z_O}\right)$$

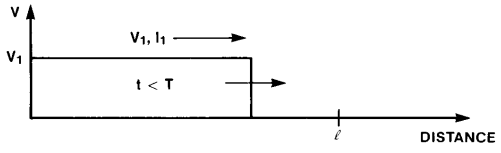
Substituting in Equation 9-8 gives

(E9-9) $$V_T = 2\left(\frac{R_T}{R_T + Z_O}\right) V_1$$

The foregoing has the same form as a simple voltage divider involving a generator V_1 with internal impedance Z_O driving a load R_T, except that the amplitude of V_T is doubled.

The arrow indicating the direction of V_r, in *Figure 9-1* correctly indicates the V_r direction of travel, but the direction of I_r flow depends on the V_r polarity. If V_r is positive, I_r flows toward the generator, opposing I_1. This relationship between the polarity of V_r and the direction of I_r can be deduced by noting in Equation 9-7 that if V_r is positive it is because R_T is greater than Z_O. In turn, this means that the initial current I_r is larger than the final quiescent current, dictated by V_1 and R_T. Hence I_r must oppose I_1 to reduce the line current to the final quiescent value. Similar reasoning shows that if V_r is negative, I_r flows in the same direction as I_1.

It is sometimes easier to determine the effect of V_r on line conditions by thinking of it as an independent voltage generator in series with R_T. With this concept, the direction of I_r is immediately apparent; its magnitude, however, is the ratio of V_r to Z_O i.e., R_T is already accounted for in the magnitude of V_r. The relationships between incident and reflected signals are represented in *Figure 9-2* for both cases of mismatch between R_T and Z_O.



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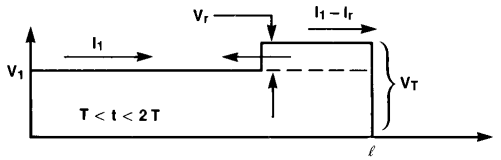
a. Incident Wave



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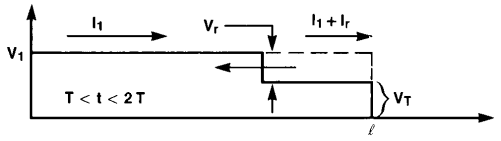
b. Reflected Wave for $R_T > Z_O$



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c. Reflected Wave for $R_T < Z_O$

FIGURE 9-2. Reflections for $R_T \neq Z_O$

The incident wave is shown in *Figure 9-2a*, before it has reached the end of the line. In *Figure 9-2b*, a positive V_r is returning to the generator. To the left of V_r the current is still I_1, flowing to the right, while to the right of V_r the net current in the line is the difference between I_1 and I_r. In *Figure 9-2c*, the reflection coefficient is negative, producing a negative V_r. This, in turn, causes an increase in the amount of current flowing to the right behind the V_r wave.

SOURCE IMPEDANCE, MULTIPLE REFLECTIONS

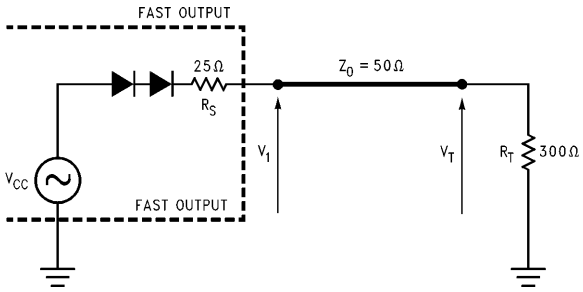
When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to V_r. The coefficient of reflection at the source is governed by Z_O and the source resistance R_S.

(E9-10)
$$\rho_S = \frac{R_S - Z_O}{R_S + Z_O}$$

If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

(E9-11) $V_T = V_1 + V_r$ and $I_T = I_1 - I_r$

If neither source impedance nor terminating impedance matches Z_O, multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in *Figure 9-3*. The source is a step function of $V_{CC} = 5.0V$ amplitude occurring at time t0. The initial value of V_1 starting down the line is 2.4V due to the voltage divider action of Z_O and R_S. The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.



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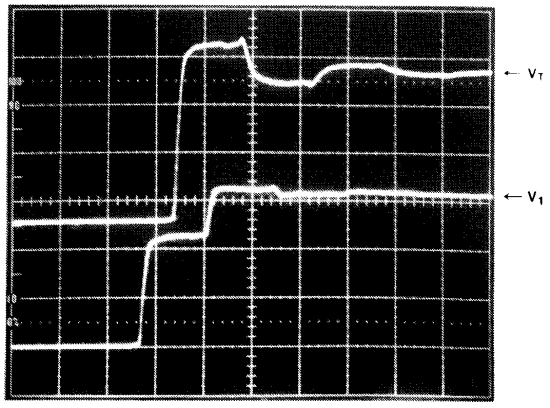
$$V_O = V_{CC} - 2 \bullet V_{BE} = 3.6V$$

$$\rho_S = \frac{(25 - 50)\Omega}{(25 + 50)\Omega} = -0.33$$

$$\text{Initially: } V_1 = \frac{Z_O}{Z_O + R_S} \bullet V_O$$

$$V_1 = \frac{50\Omega}{(50 + 25)\Omega}(3.6V) = 2.4$$

$$\rho_L = \frac{(300 - 50)\Omega}{(300 + 50)\Omega} = 0.71$$



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H = 20 ns/div
V = 1.0 V/div

FIGURE 9-3. Multiple Reflections Due to Mismatch at Load and Source

The amplitude and persistence of the ringing shown in *Figure 9-3* become greater with increasing mismatch between the line impedance and source and load impedances. Reducing R_S *(Figure 9-3)* to 13Ω increases ρ_S to −0.75, and the effects are illustrated in *Figure 9-4*. The initial value of V_T is 1.8V with a reflection of 0.9V from the open end. When this reflection reaches the source, a reflection of (0.9) × (−0.75V) starts back toward the open end. Thus, the second increment of voltage arriving at the open end is negative-going. In turn, a negative-going reflection of (0.9) × (−0.75V) starts back toward the source. This negative increment is again multiplied by −0.75V at the source and returned toward the open end. It can be deduced that the difference in amplitude between the first two positive peaks observed at the open end is:

$$V_T - V'_T = (1 + \rho_L)\, V_1 - (1 + \rho_L)\, V_1\, \rho^2_L \rho^2_S$$

(E9-12) $$= (1 + \rho_L)\, V_1\, (1 - \rho^2_L \rho^2_S).$$

The factor $(1 - \rho^2_L \rho^2_S)$ is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.

LATTICE DIAGRAM

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating the conditions which combines magnitude, polarity and time utilizes a graphic construction called a lattice diagram. A lattice diagram for the line conditions of *Figure 9-3* is shown in *Figure 9-5*.

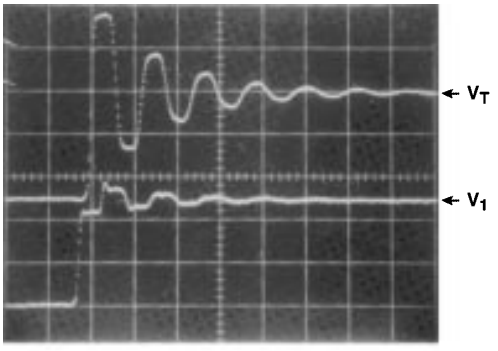

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FIGURE 9-4. Extended Ringing when R_S of *Figure 9-3* is Reduced to 13Ω

The vertical lines symbolize discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of 2T, starting at t_0 for V_1 and T for V_T. The diagonal lines indicate the incremental voltages traveling between the ends of the line; solid lines are used for positive voltages and dashed lines for negative. It is helpful to write the reflection and transmission multipliers ρ and (1 + ρ) at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that V_1 and V_T asymptotically approach 3.4V, as they must with a 3.4V source driving an open-ended line.

SHORTED LINE

The open-ended line in *Figure 9-3* has a reflection coefficient of 0.71 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of −1 and successive reflections must cause the line conditions to approach the steady state conditions of zero voltage and a line current determined by the source voltage and resistance.

Shorted line conditions are shown in *Figure 9-6a* with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. *Figure 9-6b* shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is about +2.4V, which is inverted at the shorted end and returned toward the source as −2.4V. Arriving back at the source end of the line, this voltage is multiplied by $(1 + \rho_S)$, causing a −1.61V net change in V_1. Concurrently, a reflected voltage of +0.80V (−2.4V times ρ_S of −0.33) starts back toward the shorted end of the line. The voltage at V_1 is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of 0V on the line.

When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in *Figure 9-6c*. The amplitude decreases by 50% with each successive occurrence as it did in *Figure 9-6b*.

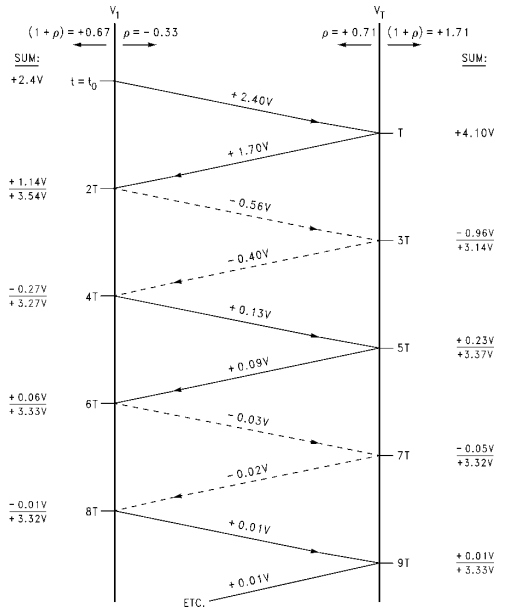

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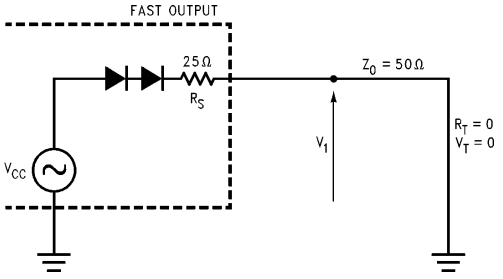
FIGURE 9-5. Lattice Diagram for the Circuit of *Figure 9-3*

SERIES TERMINATION

Driving an open-ended line through a source resistance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the backplane to another board with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. *Figure 9-7* shows a 93Ω line driven from a 1V generator through a source impedance of 93Ω. The photograph illustrates that the amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude ($1 + \rho_L = 2$). The reflected voltage arriving back at the source raises V_1 to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of line to avoid receiving a 2-step input signal.

A TTL output driving a series-terminated line is limited in fanout due to the IR drop associated with the collective I_{IL} drops of the inputs being driven. For most TTL families other than FAST®, series termination should not be considered since either the input currents are so high (TTL, S, H) or the input threshold is very low (LS). In either case the noise margins are severely degraded to the point where the circuit becomes unusable. In FAST, however, the I_{IL} of 0.6 mA, through a 25Ω resistor used as a series terminator, will reduce the low level noise margin by 15.0 mV for each standard FAST input driven.



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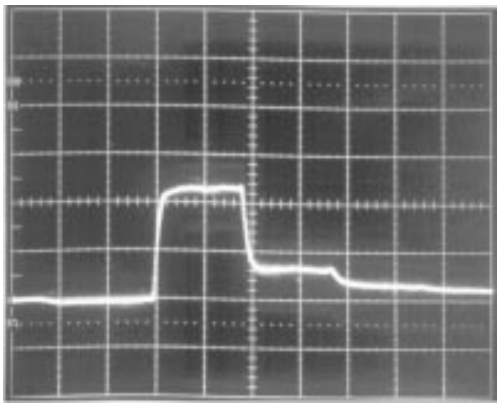
a. Reflection Coefficients for Shorted Line



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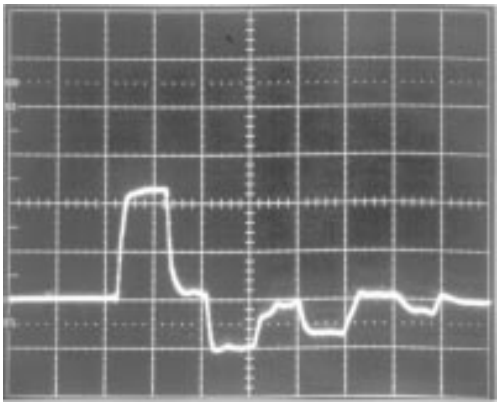
b. Input Pulse Duration ≫ Line Delay



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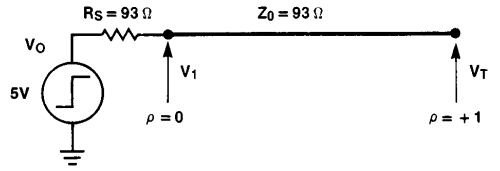
c. Input Pulse Duration < Line Delay

FIGURE 9-6. Reflections of Long and Short Pulses on a Shorted Line



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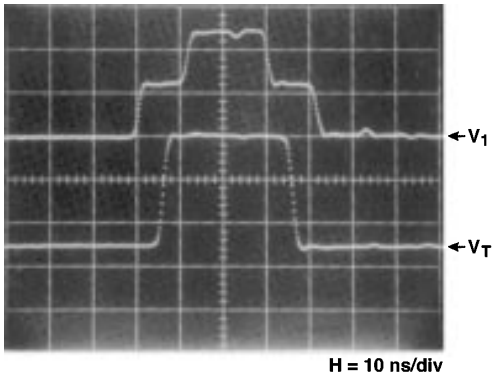

H = 10 ns/div
V = 2.0 V/div

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FIGURE 9-7. Series-Terminated Line Waveforms

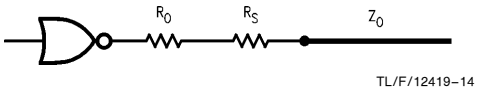

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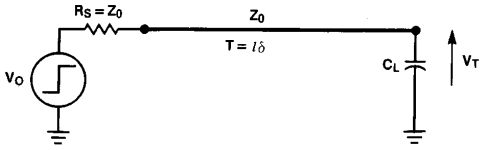
FIGURE 9-8. TTL Element Driving a Series-Terminated Line



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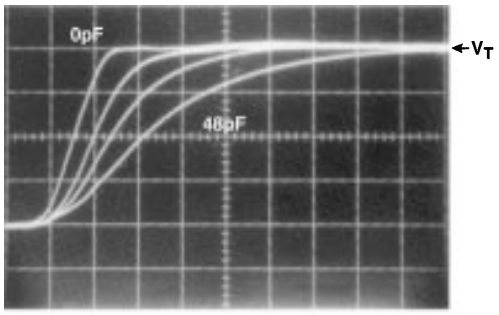
a. Series-Terminated Line with Load Capacitance



H = 1 ns/div
V = 1.0 V/div

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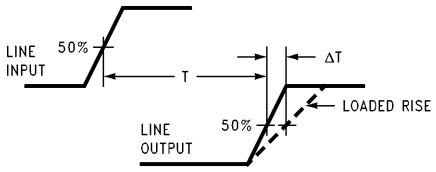
b. Output Rise Time Increase with Increasing Load Capacitance



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c. Extra Delay ΔT Due to Rise Time Increase

FIGURE 9-9. Extra Delay with Termination Capacitance

EXTRA DELAY WITH TERMINATION CAPACITANCE

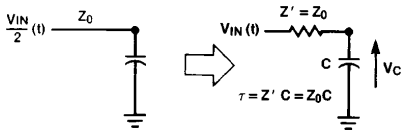
Designers should consider the effect of the load capacitance at the end of the line when using series termination. *Figure 9-9* shows how the output waveform changes with increasing load capacitance. *Figure 9-9b* shows the effect of load capacitances of 0, 12, 24, 48 pF. With no load, the delay between the 50% points of the input and output is just the line delay T. A capacitive load at the end of the line causes an extra delay ΔT due to the increase in rise time of the output signal. The midpoint of the signal swing is a good approximation of the FAST threshold since V_{OL} = 0.5V and V_{OH} = 2.7V and the actual input switching threshold of FAST is 1.5V at 25°C.

The increase in propagation delay can be calculated by using a ramp approximation for the incident voltage and characterizing the circuit as a fixed impedance in series with the load capacitance, as shown in *Figure 9-10*. One general solution serves both series and parallel termination cases by using an impedance Z′ and a time constant, τ, defined in *Figure 9-10a* and *9-10b*.

Calculated and observed increases in delay time to the 50% point show close agreement when τ is less than half the ramp time. At large ratios of τ/a (where a = ramp time),

measured delays exceed calculated values by approximately 7%. *Figure 9-11*, based on measured values, shows the increase in delay to the 50% point as a function of the Z′C time constant, both normalized to the 10% to 90% rise time of the input signal. As an example of using the graph, consider a 100Ω series-terminated line with 30 pF load capacitance at the end of the line. The 3 ns rise time assumed is typical of FAST in an actual line driving application. From *Figure 9-10a*, Z′ is equal to 100Ω; the ratio $\frac{Z'C}{t_r}$ is 1. From the graph, the ratio $\Delta T/t_r$ is 0.8. Thus the increase in the delay to the 50% point of the output waveform is 0.8 t_r, or 2.4 ns, which is then added to the no-load line delay T to determine the total delay.

Had the 100Ω line in the foregoing example been parallel rather than series terminated at the end of the line, Z′ would be 50Ω. The added delay would be only 1.35 ns with the same 30 pF loading at the end. The added delay would be only 0.75 ns if the line were 50Ω and parallel-terminated. The various trade-offs involving type of termination, line impedance, and loading are important considerations for critical delay paths.



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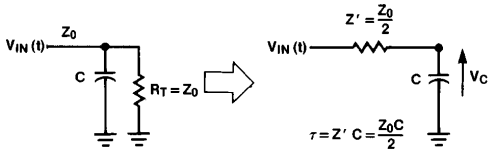
a.Thevenin Equivalent for Series-Terminated Case



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b. Thevenin Equivalent for Parallel-Terminated Case

FIGURE 9-10. Determining the Effect of End-of-Line Capacitance

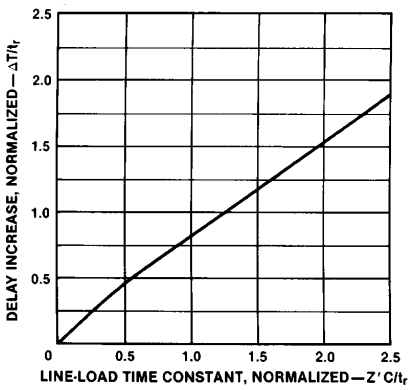

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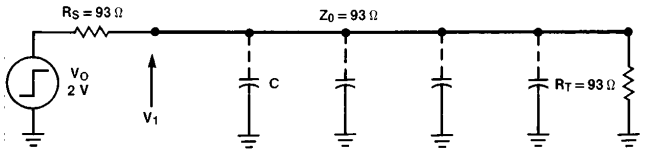
FIGURE 9-11. Increase in 50% Point Delay Due to Capacitive Loading at the End of the Line, Normalized to t_r

DISTRIBUTED LOADING EFFECTS ON LINE CHARACTERISTICS

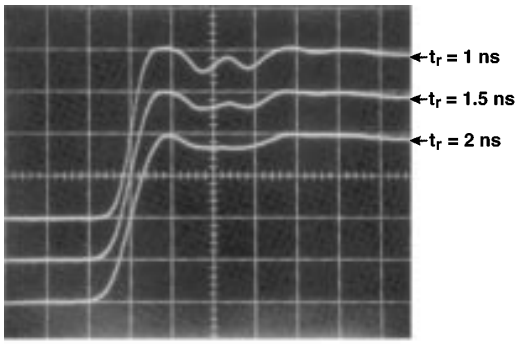
When capacitive loads such as TTL inputs are connected along a transmission line, each one causes a reflection with a polarity opposite to that of the incident wave. Reflections from two adjacent loads tend to overlap if the time required for the incident wave to travel from one load to the next is equal to or less than the signal rise time. *Figure 9-12a* illustrates an arrangement for observing the effects of capacitive loading, while *Figure 9-12b* shows an incident wave followed by reflections from two capacitive loads. The two capacitors causing the reflections are separated by a distance requiring a travel time of 1 ns. The two reflections return to the source 2 ns a part, since it takes 1 ns longer for the incident wave to reach the second capacitor and an additional 1 ns for the second reflection to travel back to the source. In the upper trace of *Figure 9-12b*, the input signal rise time is 1 ns and there are two distinct reflections, although the trailing edge of the first overlaps the leading edge of the second. The input rise time is longer in the middle trace, causing a greater overlap. In the lower trace, the 2 ns input rise time causes the two reflections to merge and appear as a single reflection which is relatively constant (at $\approx -10\%$) for half its duration. This is about the same reflection that would occur if the 93Ω line had a middle section with an impedance reduced to 75Ω.

With a number of capacitors distributed all along the line of *Figure 9-12a*, the combined reflections modify the observed input waveform as shown in the top trace of *Figure 9-12c*. The reflections persist for a time equal to the 2-way line delay (15 ns), after which the line voltage attains its final value. The waveform suggests a line terminated with a resistance greater than its characteristic impedance ($R_T > Z_O$). This analogy is strengthened by observing the effect of reducing R_T from 93Ω to 75Ω which leads to the middle waveform of *Figure 9-12c*. Note that the final (steady state) value of the line voltage is reduced by about the same amount as that caused by the capacitive reflections. In the lower trace of *Figure 9-12c* the source resistance R_S is reduced from 93Ω to 75Ω, restoring both the initial and final line voltage values to the same amplitude as the final value in the upper trace. From the standpoint of providing a desired signal voltage on the line and impedance matching at either end, the effect of distributed capacitive loading can be treated as a reduction in line impedance.



TL/F/12419–21

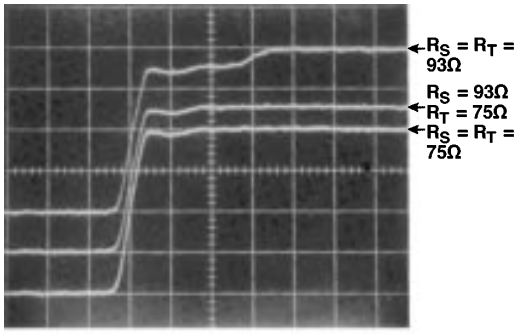
a. Arrangement for Observing Capacitive Loading Effects



H = 2 ns/div
V = 0.25 V/div

TL/F/12419–22

b. Capacitive Reflections Merging as Rise Time Increases



H = 5 ns/div
V = 0.25 V/div

TL/F/12419–23

c. Matching the Altered Impedance of a Capacitively Loaded Line

FIGURE 9-12. Capacitive Reflections and Effects on Line Characteristics

The reduced line impedance can be calculated by considering the load capacitance C_L as an increase in the intrinsic line capacitance C_O along that portion of the line where the loads are connected. Denoting this length of line as l, the distributed value C_D of the load capacitance is as follows:

$$C_D = \frac{C_L}{l}$$

C_D is then added to C_O in Equation 9-1 to determine the reduced line impedance Z_O.

$$Z'_O = \sqrt{\frac{L_O}{C_O + C_D}} = \sqrt{\frac{L_O}{C_O\left(1 + \frac{C_D}{C_O}\right)}}$$

$$Z'_O + \frac{\sqrt{\frac{L_O}{C_O}}}{\sqrt{1 + \frac{C_D}{C_O}}} = \frac{Z_O}{\sqrt{1 + \frac{C_D}{C_O}}} \qquad \textbf{(E9-13)}$$

In the example of *Figure 9-12c*, the total load capacitance (lC_O) is 60 pF. Note that the ratio C_D/C_O is the same as C_L/lC_O. The calculated value of the reduced impedance is thus

$$Z'_O = \frac{93}{\sqrt{1 + \frac{33}{60}}} = \frac{93}{\sqrt{1.55}} = 75\Omega \qquad \textbf{(E9-14)}$$

This correlates with the results observed in *Figure 9-12c* when R_T and R_S are reduced to 75Ω.

The distributed load capacitance also increases the line delay, which can be calculated from Equation 9-2.

$$\delta' = \sqrt{L_O\,(C_O + C_D)} = \sqrt{L_O C_O}$$

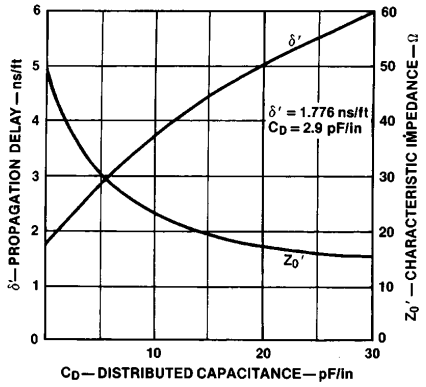
$$\sqrt{1 + \frac{C_D}{C_O}} = \delta\sqrt{1 + \frac{C_D}{C_O}} \qquad \textbf{(E9-15)}$$

The line used in the example of *Figure 9-12c* has an intrinsic delay of 6 ns and a loaded delay of 7.5 ns which checks with Equation 9-15.

$$\textbf{(E9-16)} \qquad l\delta' = l\delta\sqrt{1.55} = 6\sqrt{1.55} = 7.5 \text{ ns}$$

Equation 9-15 can be used to predict the delay for a given line and load. The ratio C_D/C_O (hence the loading effect) can be minimized for a given loading by using a line with a high intrinsic capacitance C_O.

A plot of Z' and δ' for a 50Ω line as a function of C_D is shown in *Figure 9-13*. This figure illustrates that relatively modest amounts of load capacitance will add appreciably to the propagation delay of a line. In addition, the characteristic impedance is reduced significantly.



TL/F/12419–24

FIGURE 9-13. Capacitive Loading Effects on Line Delay and Impedance

Worst case reflections from a capacitively loaded section of transmission line can be accurately predicted by using the modified impedance of Equation 9-9. When a signal originates on an unloaded section of line, the effective reflection coefficient is as follows:

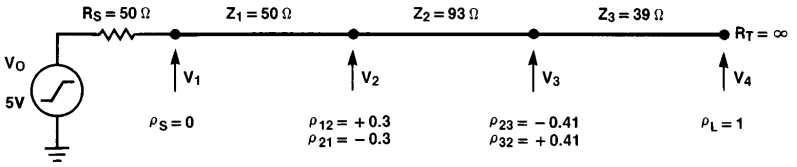
$$\rho = \frac{Z'_O - Z_O}{Z'_O + Z_O} \qquad \textbf{(E9-17)}$$

MISMATCHED LINES

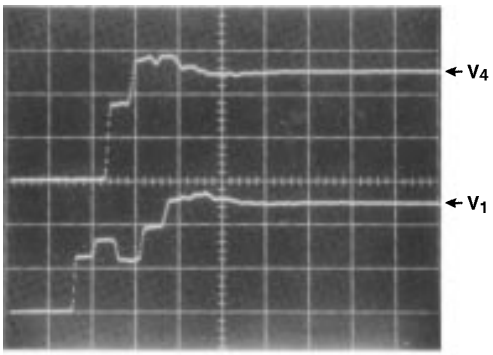
Reflections occur not only from mismatched load and source impedances but also from changes in line impedance. These changes could be caused by bends in coaxial cable, unshielded twisted-pair in contact with metal, or mismatch between PC board traces and backplane wiring. With the coax or twisted-pair, line impedance changes run about 5% to 10% and reflections are usually no problem since the percent reflection is roughly half the percent change in impedance. However, between PC board and backplane wiring, the mismatch can be 2 or 3 to 1. This is illustrated in *Figure 9-14* and analyzed in the lattice diagram of *Figure 9-15*. Line 1 is driven in the series-terminated mode so that reflections coming back to the source are absorbed.

The reflection and transmission at the point where impedances differ are determined by treating the downstream line as though it were a terminating resistor. For the example of *Figure 9-14*, the reflection coefficient at the intersection of lines 1 and 2 for a signal traveling to the right is as follows:

$$\rho_{12} = \frac{Z2 - Z1}{Z2 + Z1} = \frac{93 - 50}{143} = +0.3 \qquad \textbf{(E9-18)}$$



TL/F/12419–25



TL/F/12419–26

FIGURE 9-14. Reflections from Mismatched Lines

Thus the signal reflected back toward the source and the signal continuing along line 2 are, respectively, as follows:

$$V_{1r} = \rho 12\, V_1 = +0.3\, V_1$$

(E9-19) $$V_2 = (1 + \rho 12)\, V_1 = +1.3\, V_1$$

At the intersection of lines 2 and 3, the reflection coefficient for signals traveling to the right is determined by treating Z_3 as a terminating resistor.

(E9-20) $$\rho 23 = \frac{Z_3 - Z_2}{Z_3 + Z_2} = \frac{39 - 93}{132} = -0.41$$

When V_2 arrives at this point, the reflected and transmitted signals are as follows:

$$V_{2r} = \rho 23\, V_2 = -0.41\, V_2$$

$$= (-0.41)\,(1.3)\, V_1$$

(E9-21a) $$= -0.53\, V_1$$

$$V_3 = (1 + \rho 23)\, V_2 = 0.59\, V_2$$

$$= (0.59)\,(1.3)\, V_1$$

(E9-21b) $$= 0.77\, V_1$$

Voltage V_3 is doubled in magnitude when it arrives at the open-ended output, since ρ_L is $+1$. This effectively cancels the voltage divider action between R_S and Z_1.

$$V_4 = (1 + \rho_L)\,(1 + \rho 23)\, V_2$$

(E9-22) $$= (1 + \rho_L)\,(1 + \rho 23)\,(1 + \rho 12)\, V_1$$

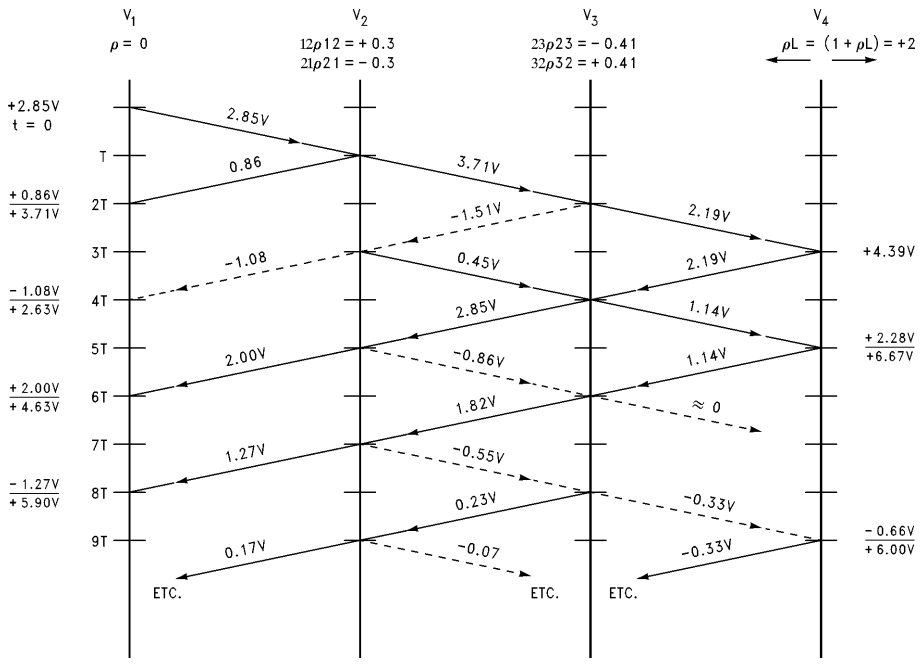
$$= (1 + \rho_L)\,(1 + \rho 23)\,(1 + \rho 12)\,\frac{V_O}{2}$$

$$V_4 = (1 + \rho 23)\,(1 + \rho 12)\, V_O$$

Thus, Equation 9-22 is the general expression for the initial step of output voltage for three lines when the input is series-terminated and the output is open-ended. Note that the reflection coefficients at the intersections of lines 1 and 2 and lines 2 and 3 in *Figure 9-15* have reversed signs for signals traveling to the left. Thus the voltage reflected from the open output and the signal reflecting back and forth on line 2 both contribute additional increments of output voltage in the same polarity as V_O. Lines 2 and 3 have the same delay time; therefore, the two aforementioned increments arrive at the output simultaneously at time 5T on the lattice diagram *(Figure 9-15)*.

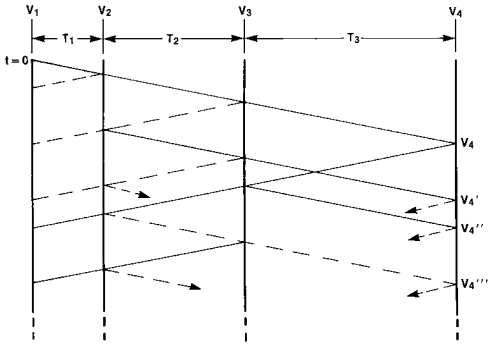
In the general case of series lines with different delay times, the vertical lines on the lattice diagram should be spaced apart in the ratio of the respective delays. *Figure 9-16* shows this for a hypothetical case with delay ratios 1:2:3. For a sequence of transmission lines with the highest impedance line in the middle, at least three output voltage increments with the same polarity as V_O occur before one can occur of opposite polarity. On the other hand, if the middle line has the lowest impedance, the polarity of the second increment of output voltage is the opposite of V_O. The third increment of output voltage has the opposite polarity, for the time delay ratios of *Figure 9-16*.

When transmitting logic signals, it is important that the initial step of line output voltage passes through the threshold region of the receiving circuit, and that the next two increments of output voltage augment the initial step. Thus in a series-terminated sequence of three mismatched lines, the middle line should have the highest impedance.



TL/F/12419–27

FIGURE 9-15. Lattice Diagram for the Circuit of *Figure 9-14*



TL/F/12419–28

FIGURE 9-16. Lattice Diagram for Three Lines with Delay Ratios 1:2:3

RISE TIME VERSUS LINE DELAY

When the 2-way line delay is less than the rise time of the input wave, any reflections generated at the end of the line are returned to the source before the input transition is completed. Assuming that the generator has a finite source resistance, the reflected wave adds algebraically to the input wave while it is still in transition, thereby changing the shape of the input. This effect is illustrated in *Figure 9-17*, which shows input and output voltages for several comparative values of rise time and line delay.

In *Figure 9-17b* where the rise time is much shorter than the line delay, V_1 rises to an initial value of 1V. At time T later, V_T rises to 0.5V, i.e., $1 + \rho_L = 0.5$. The negative reflection arrives back at the source at time 2T, causing a net change of -0.4V, i.e., $(1 + \rho_S)(-0.5) = -0.4$.

The negative coefficient at the source changes the polarity of the other 0.1V of the reflection and returns it to the end of the line, causing V_T to go positive by another 50 mV at time 3T. The remaining 50 mV is inverted and reflected back to the source, where its effect is barely distinguishable as a small negative change at time 4T.

In *Figure 9-17c*, the input rise time (0% to 100%) is increased to such an extent that the input ramp ends just as the negative reflection arrives back at the source end. Thus the input rise time is equal to 2T.

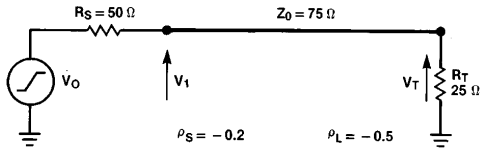
The input rise time is increased to 4T in *Figure 9-17d*, with the negative reflection causing a noticeable change in input slope at about its midpoint. This change in slope is more visible in the double exposure photo of *Figure 9-17e*, which shows V_1 (t_r still set for 4T) with and without the negative reflection. The reflection was eliminated by terminating the line in its characteristic impedance.

The net input voltage at any particular time is determined by adding the reflection to the otherwise unaffected input. It must be remembered that the reflection arriving back at the input at a given time is proportional to the input voltage at a time 2T earlier. The value of V_1 in *Figure 9-17d* can be calculated by starting with the 1V input ramp.

$$V_1 = \frac{1}{t_r} \bullet t \text{ for } 0 \leq t \leq 4T$$

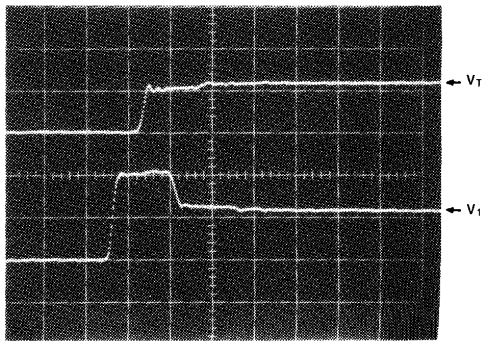
(E9-23)

$$= 1\text{V for } t \geq 4T$$



TL/F/12419–29

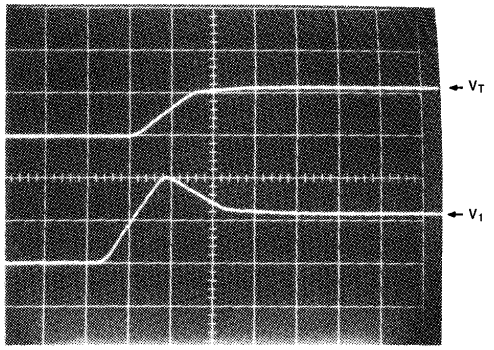
a. Test Arrangement for Rise Time Analysis



H = 10 ns/div
V = 0.5 V/div

TL/F/12419–30

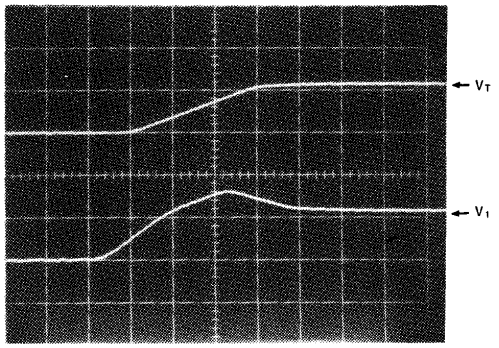
b. Line Voltages for $t_r < < T$



H = 10 ns/div
V = 0.5 V/div

TL/F/12419–31

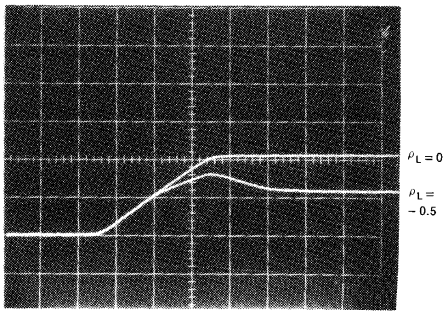
c. Line Voltages for $t_r = 2T$



H = 10 ns/div
V = 0.5 V/div

TL/F/12419–32

d. Line Voltages for $t_r = 4T$



H = 10 ns/div
V = 0.5 V/div

TL/F/12419–33

e. Input Voltage With and Without Reflection

FIGURE 9-17. Line Voltages for Various Ratios of Rise Time to Line Delay

The reflection from the end of the line is

$$V_r = \frac{\rho_L\,(t - 2T)}{t_r}; \qquad \textbf{(E9-24)}$$

the portion of the reflection that appears at the input is

$$V'_r = \frac{(1 + \rho_S)\,\rho_L\,(t - 2T)}{t_r}; \qquad \textbf{(E9-25)}$$

the net value of the input voltage is the sum.

$$V'_1 = \frac{t}{t_r} + \frac{(1 + \rho_S)\,\rho_L\,(t - 2T)}{t_r} \qquad \textbf{(E9-26)}$$

The peak value of the input voltage in *Figure 9-17d* is determined by substituting values and letting t equal 4T.

$$V'_1 = \frac{(0.8)\,(-0.5)\,(4T - 2T)}{t_r}$$

$$= 1 - 0.04\,(0.5) = 0.8V \qquad \textbf{(E9-27)}$$

After this peak point, the input ramp is no longer increasing but the reflection is still arriving. Hence the net value of the input voltage decreases. In this example, the later reflections are too small to be detected and the input voltage is thus stable after time 6T. For the general case of repeated reflections, the net voltage $V_{1(t)}$ seen at the driven end of the line can be expressed as follows, where the signal caused by the generator is $V_{1(t)}$:

$$V'_{1(t)} = V_{1(t)} \quad \text{for } 0 < t < 2T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t - 2T)} \quad \text{for } 2T < t < 4T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t - 2T)} + (1 + \rho_S)\,\rho_S\rho_L^2\,(V_{1(t - 4T)} \quad \text{for } 4T < t < 6T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t - 2T)} + (1 + \rho_S)\,\rho_S\rho_L^2\,V_{1(t - 4T)} + (1 + \rho_S)\,\rho_S^2\rho_L^3\,V_{1(t - 6T)} \quad \text{for } 6T < t < 8T, \text{ etc.} \qquad \textbf{(E9-28)}$$

The voltage at the output end of the line is expressed in a similar manner.

$$V_{T(t)} = 0 \quad \text{for } 0 < t < T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t - T)} \quad \text{for } T < t < 3T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t - T)} + (1 + \rho_L)\,\rho_S\rho_L\,V_{1(t - 3T)} \quad \text{for } 3T < t < 5T$$

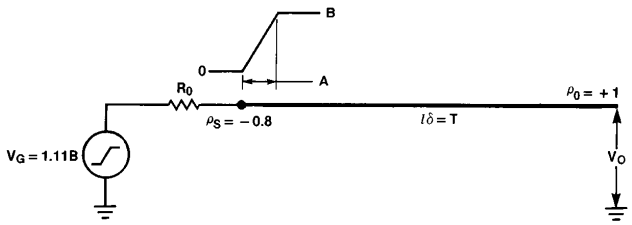
$$V_{T(t)} = (1 + \rho_L)\,V_{1(t - T)} + (1 + \rho_L)\,\rho_S\rho_L\,V_{1(t - 3T)} + (1 + \rho_L)\,\rho_S^2\rho_L^2\,V_{1(t - 5T)} \quad \textbf{(E9-29)} \quad \text{for } 5T < t < 7T, \text{ etc.}$$

RINGING

Multiple reflections occur on a transmission line when neither the signal source impedance nor the termination (load) impedance matches the line impedance. When the source reflection coefficient ρ_S and the load reflection coefficient ρ_L are of opposite polarity, the reflections alternate in polarity. This causes the signal voltage to oscillate about the final steady state value, commonly recognized as ringing.

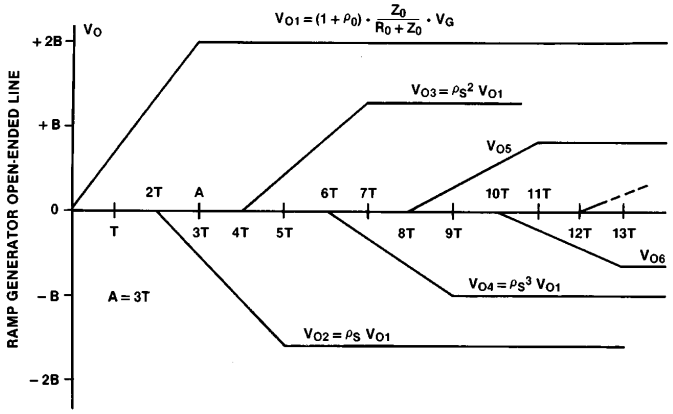
When the signal rise time is long compared to the line delay, the signal shape is distorted because the individual reflections overlap in time. The basic relationships among rise time, line delay, overshoot and undershoot are shown in a simplified diagram, *Figure 9-18*. The incident wave is a ramp of amplitude B and rise duration A. The reflection coefficient at the open-ended line output is $+1$ and the source reflection coefficient is assumed to be -0.8, i.e., $R_O = Z_O/9$.

Figure 9-18b shows the individual reflections treated separately. Rise time A is assumed to be three times the line delay T. The time scale reference is the line output and the first increment of output voltage V_O rises to 2B in the time interval A. Simultaneously, a positive reflection (not shown) of amplitude B is generated and travels to the source, whereupon it is multiplied by -0.8 and returns toward the end of the line. This negative-going ramp starts at time 2T (twice the line delay) and doubles to -1.6B at time 2T + A.



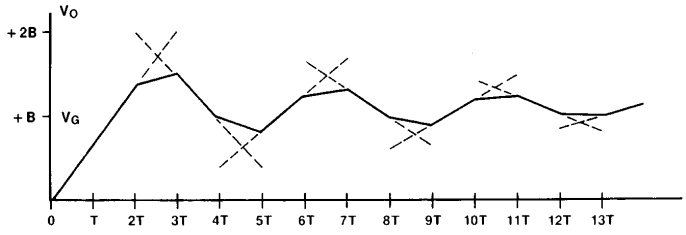
TL/F/12419–34

a. Ramp Generator Driving Open-Ended Line



TL/F/12419–35

b. Increments of Output Voltage Treated Individually



TL/F/12419–36

c. Net Output Signal Determined by Superposition

FIGURE 9-18. Basic Relationships Involved in Ringing

The negative-going increment also generates a reflection of amplitude −0.8B which makes the round trip to the source and back, appearing at time 4T as a positive ramp rising to +1.28B at time 4T+A. The process of reflection and re-reflection continues, and each successive increment changes in polarity and has an amplitude of 80% of the preceding increment.

In *Figure 9-18c*, the output increments are added algebraically by superposition. The starting point of each increment is shifted upward to a voltage value equal to the algebraic sum of the quiescent levels of all the preceding increments (i.e., 0, 2B, 0.4B, 1.68B, etc.). For time intervals when two ramps occur simultaneously, the two linear functions add to produce a third ramp that prevails during the overlap time of the two increments.

It is apparent from the geometric relationships, that if the ramp time A is less than twice the line delay, the first output increment has time to rise to the full 2B amplitude and the second increment reduces the net output voltage to 0.4B. Conversely, if the line delay is very short compared to the ramp time, the excursions about the final value V_G are small.

Figure 9-18c shows that the peak of each excursion is reached when the earlier of the two constituent's ramps reaches its maximum value, with the result that the first peak occurs at time A. This is because the earlier ramp has a greater slope (absolute value) than the one that follows.

Actual waveforms such as produced by TTL do not have a constant slope and do not start and stop as abruptly as the ramp used in the example of *Figure 9-18*. Predicting the time at which the peaks of overshoot and undershoot occur is not as simple as with ramp excitation. A more rigorous treatment is required, including an expression for the driving waveform which closely simulates its actual shape. In the general case, a peak occurs when the sum of the slopes of the individual signal increment is zero.

SUMMARY

The foregoing discussions are by no means an exhaustive treatment of transmission line characteristics. Rather, they are intended to focus attention on the general methods used to determine the interactions between high-speed logic circuits and their interconnections. Considering an interconnection in terms of distributed rather than lumped inductance and capacitance leads to the line impedance concept, i.e., mismatch between this characteristic impedance and the terminations causes reflections and ringing.

Series termination provides a means of absorbing reflections when it is likely that discontinuities and/or line impedance changes will be encountered. A disadvantage is that the incident wave is only one-half the signal swing, which limits load placement to the end of the line. TTL input capacitance increases the rise time at the end of the line, thus increasing the effective delay. With parallel termination, i.e., at the end of the line, loads can be distributed along the line. TTL input capacitance modifies the line characteristics and should be taken into account when determining line delay.

Series termination provides a means of absorbing reflections when it is likely that discontinuities and/or line impedance changes will be encountered. A disadvantage is that the incident wave is only one-half the signal swing, which limits load placement to the end of the line. TTL input capacitance increases the rise time at the end of the line, thus increasing the rise time at the end of the line, thus increasing the effective delay. With parallel termiantion, i.e., at the end of the line, loads can be distributed along the line. TTL input capacitance modifies the line characteristics and should be taken into account when determining line delay.

LINE DRIVING

All interconnects, such as coaxial cable, defined impedance transmission lines and feeders, can be considered as transmission lines, whereas printed circuit traces and hook-up wire tend to be ignored as transmission lines. With any high-speed logic family, all interconnects should be considered as transmission lines, and evaluated as such to see if termination is required. Of the many properties of transmission lines, two are of major interest to us: Z_O (the effective equivalent resistive value that causes zero reflection) and t_{PD} (propagation delay down the transmission line). Both of these parameters are geometry dependent. Here are some common configurations:

PRINTED CIRCUIT CONFIGURATIONS

h = dielectric thickness

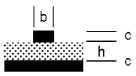
c = trace thickness

L = trace length

K = dielectric thickness between ground planes

b = trace width

ϵ_r = dielectric constant

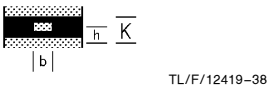


TL/F/12419–37

FIGURE 9-19. Micro Stripline

$$Z_O = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8\,b + c}\right)\Omega$$

(E9-30) $$t_{PD} = 1.017\sqrt{0.475\,\epsilon_r + 0.67}\ \text{ns/ft.}$$

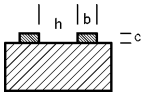


TL/F/12419–38

FIGURE 9-20. Stripline

$$Z_O = \frac{60}{\sqrt{\epsilon_r}} \ln\left(\frac{4K}{0.67\,\pi b\left(0.8 + \frac{c}{b}\right)}\right)\Omega$$

(E9-31) $$t_{PD} = 1.017\sqrt{\epsilon_r}\ \text{ns/ft.}$$

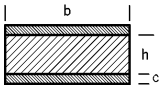


TL/F/12419–39

FIGURE 9-21. Side by Side

$$Z_O = \frac{120}{\sqrt{\epsilon_r}} ln\left(\frac{\pi h}{b + c}\right) \Omega$$

(E9-32) $t_{PD} = 1.017\sqrt{0.475\,\epsilon_r + 0.67}$ ns/ft.

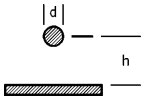


TL/F/12419–40

FIGURE 9-22. Flat Parallel Conductors for b ≫ h and h ≫ c

$$Z_O = \frac{377}{\sqrt{\epsilon_r}} ln\left(\frac{h}{b}\right) \Omega$$

(E9-33) $t_{PD} = 1.017\sqrt{0.475\epsilon_r + 0.67}$ ns/ft.

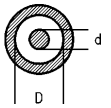


TL/F/12419–41

a. Wire Over Ground Plane

$$Z_O = \frac{60}{\sqrt{\epsilon_r}} ln\left(\frac{4h}{d}\right) \Omega$$

(E9-34)



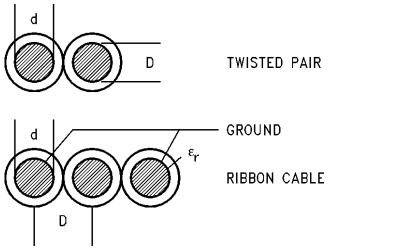
TL/F/12419–42

b. Coaxial Cable

$$Z_O = \frac{60}{\sqrt{\epsilon_r}} ln\left(\frac{D}{d}\right) \Omega$$

(E9-35)

FIGURE 9-23. Wiring



TL/F/12419–43

$$Z_O = \frac{120}{\sqrt{\epsilon_r}} ln\left(\frac{2D}{d}\right) \Omega$$

(E9-36)

FIGURE 9-24. Twisted Pair or Ribbon Cable

All of the above rely on the complex relationship

$$Z_O = \sqrt{\frac{R_O + j\,\omega L_O}{G_O + j\,\omega\,C_O}}\ \Omega$$

(E9-37)

and can be simplified to

$$Z_O = \sqrt{\frac{L_O}{C_O}}$$

if we assume

$$G_O \cong R_O \cong 0$$

Note that Z_O is real, not complex, appears resistive and is not a function of length.

Also,

$$t_{PD} = \sqrt{L_O C_O}$$

(E9-38)

The inductance of PC trace can be determined by the formula

$$L_O = \left[0.0051\, Ln\left(\frac{4h}{\alpha}\right)\right] + 0.00127\ \mu H/inch$$

(E9-39)

where $\alpha = \sqrt{\frac{4bc}{\pi}}$

For power and ground planes in a multilayer board, the capacitance of the plane can be calculated by the formula for parallel plates separated by a dielectric:

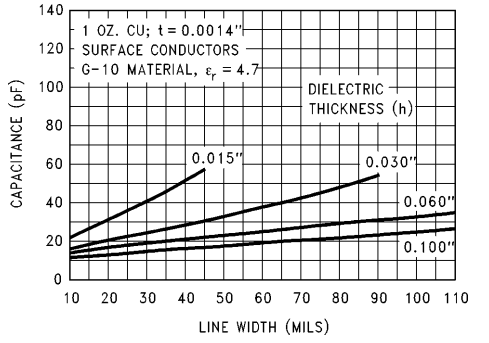
$$C = 0.2212\,\frac{\epsilon_r A}{h}\,pF$$

(E9-40)

where A = surface area of one plate.

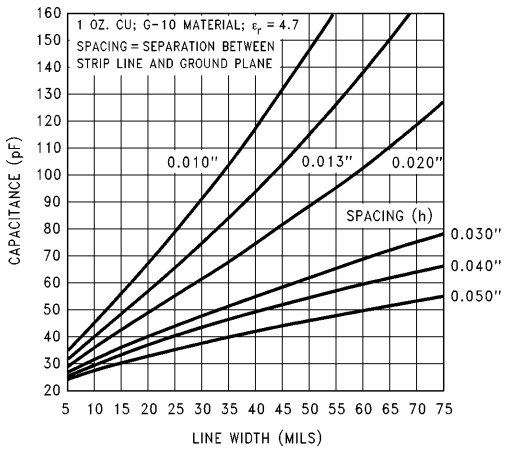
The above formula (E9-40) cannot be used to calculate PC trace capacitance. This must either be measured or an appropriate value may be taken from the following curves.

The impedance of striplines and microstriplines can be found quickly from the following curves. For characteristics of cables, refer to manufacturers' data.



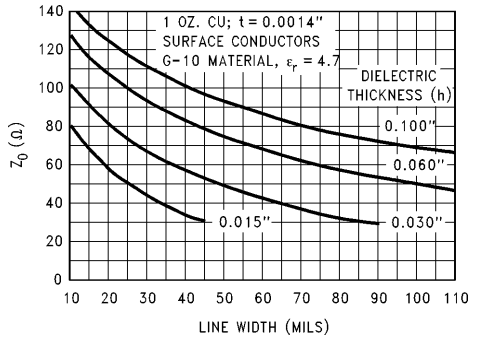
TL/F/12419–44

FIGURE 9-25. Capacitance of Microstriplines



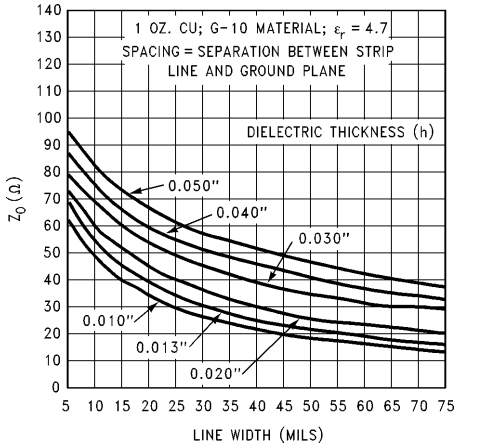
TL/F/12419–45

FIGURE 9-26. Capacitance of Striplines



TL/F/12419–46

FIGURE 9-27. Impedance of Microstriplines



TL/F/12419–47

FIGURE 9-28. Impedance of Striplines

TABLE 9-1. Relative Dielectric Constants of Various Materials

Material	ϵ_r
Air	1.0
Polyethylene Foam	1.6
Cellular Polyethylene	1.8
Teflon	2.1
Polyethylene	2.3
Polystyrene	2.5
Nylon	3.0
Silicon Rubber	3.1
Polyvinylchloride (PVC)	3.5
Epoxy Resin	3.6
Delrin	3.7
Epoxy Glass	4.7
Mylar	5.0
Polyurethane	7.0

All the above information on impedance and propagation delays are for the circuit interconnect only. The actual impedance and propagation delays will differ from this by the loading effects of gate input and output capacitances, and by any connectors that may be in line. The effective impedance and propagation delay can be determined from the following formula:

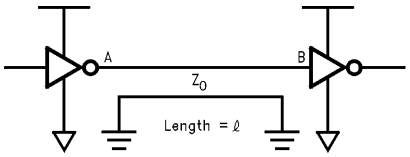
$$Z_O' = \frac{Z_O}{\sqrt{1 + \left(\frac{C_L}{C_O}\right)}}\ \Omega$$

$$t_{PD} = \sqrt{L_O C_O} \quad \therefore\ t_{PD}' = t_{PD}\sqrt{1 + \left(\frac{C_L}{C_O}\right)} \qquad \textbf{(E9-41)}$$

where C_L is the total of all additional loading.

The results of these formulas will frequently give effective impedances of less than half Z_O, and interconnect propagation delays greater than the driving device propagation delays, thus becoming the predominant delay.

DRIVING TRANSMISSION LINES



TL/F/12419–48

FIGURE 9-29

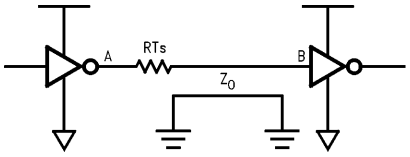
1. Unterminated

The maximum length for an unterminated line can be determined by

(E9-42) $$\ell_{max} = \frac{t_r}{2t_{PD}'} \text{ (For FAST, } t_r = 3 \text{ ns)}$$

$\therefore \ell_{max} = 10$ inches for trace on G10 epoxy glass P.C.

The voltage wave propagated down the transmission line (V step) is the full output drive of the deivce into Z_O'. Reflections will not be a problem if $\ell \leq \ell_{max}$. Lines longer than ℓ_{max} will be subject to ringing and reflections and will drive the inputs and outputs below ground.



TL/F/12419–49

FIGURE 9-30

2. Series-Terminated

$RT_S = Z_O$

Series termination has limited use in TTL interconnect schemes due to the voltage drop across RT_S in the LOW state, reducing noise margins at the receiver. Series termination is the ideal termination for highly capacitive memory arrays whose DC loadings are minimal. RT_S values of 10Ω to 50Ω are normally found in these applications.

3. Parallel-Terminated

Four possibilities for parallel termination exist:

A. Z'_O to V_{CC}. This will consume current from V_{CC} when output is LOW;

B. Z'_O to GND. This will consume current from V_{CC} when output is HIGH;

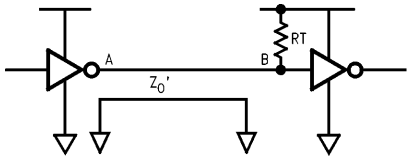
C. Thevenin equivalent termination. This will consume half the current of A and B from the output stage, but will have reduced noise margins, and consume current from V_{CC} with outputs HIGH or LOW. If used on a TRI-STATE® bus, this will set the quiescent line voltage to half.

D. AC Termination. An RC termination to GND, $R + X_C = Z_O'$, X_C to be less than 2% of Z_O' at

(E9-43) $$f = \frac{1}{2t_r}$$

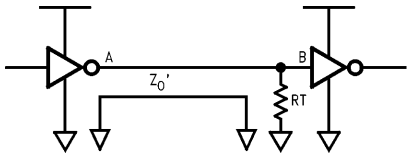
This consumes no DC current with outputs in either state. If this is used on a TRI-STATE bus, then the quiescent voltage on the line can be established at V_{CC} or GND by a high value pull up (down) resistor to the appropriate supply rail.

Parallel-Terminated



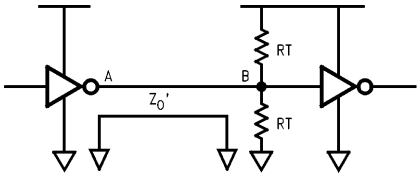
TL/F/12419–50

A. RT to V_{CC}
RT = Z_O'



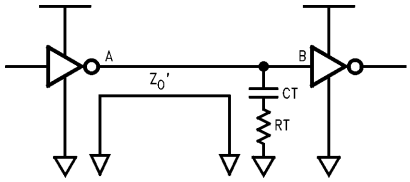
TL/F/12419–51

B. RT to GND
RT = Z_O'



TL/F/12419–52

C. Thevenin Termination
RT = 2 Z_O'



TL/F/12419–53

D. AC Termination to GND
RT + X_{CT} = Z_O'
Choose capacitor, C_T, such that: $T_{RC} > 3_{TD}$ (Line Delay)

FIGURE 9-31

DECOUPLING

TYPICAL DYNAMIC IMPEDANCE OF UNBYPASSED V_{CC} RUNS

Figure 9-32 shows several schemes for power and ground distribution on logic boards. *Figure 9-32* is a cross-section, with *a, b,* and *c* showing a 0.1 inch wide V_{CC} bus and ground on the opposite side. *Figure 9-32d* shows side-by-side V_{CC} and ground strips, each 0.04 inch wide. *Figure 9-32e* shows a four layer board with embedded power and ground planes.

In *Figure 9-32a*, the dynamic impedance of V_{CC} with respect to ground is 50Ω, even though the V_{CC} trace width is generous and there is a complete ground plane. In *Figure 9-32b*, the ground plane stops just below the edge of the V_{CC} bus and the dynamic impedance doubles to 100Ω. In *Figure 9-32c*, the ground bus is also 0.1 inch wide and runs along under the V_{CC} bus and exhibits a dynamic impedance of about 68Ω. In *Figure 9-32d*, the trace widths and spacing are such that the traces can run under a DIP, between two rows of pins. The impedance of the power and ground planes in *Figure 9-32e* is typically less than 2Ω.

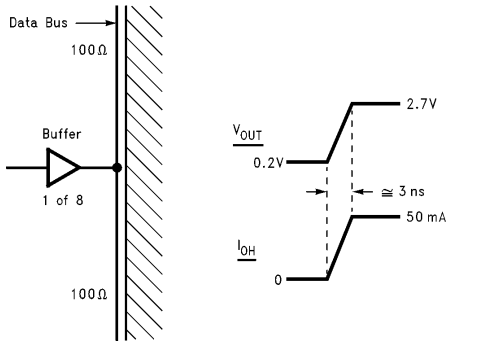
These typical dynamic impedances point out why a sudden current demand due to an IC output switching can cause a momentary reduction in V_{CC}, unless a bypass capacitor is located near the IC.

I_{CC} DRAIN DUE TO LINE DRIVING

Figure 9-33 illustrates the sudden demand for current from V_{CC} when a buffer output forces a LOW-to-HIGH transition into the midpoint of a data bus. The sketch shows a wire-over-ground transmission line, but it could also be twisted pair, flat cable or PC interconnect.

The buffer output effectively sees two 100Ω lines in parallel and thus a 50Ω load. For this value of load impedance, the buffer output will force an initial LOW-to-HIGH transition from 0.2V to 2.7V in about 3 ns. This net charge of 2.5V into a 50Ω load causes an output-HIGH current change of 50 mA.

If all eight outputs of an octal buffer switch simultaneously, in this application the current demand on V_{CC} would be 0.4A. Clearly, a nearby V_{CC} bypass capacitor is needed to accommodate this demand.

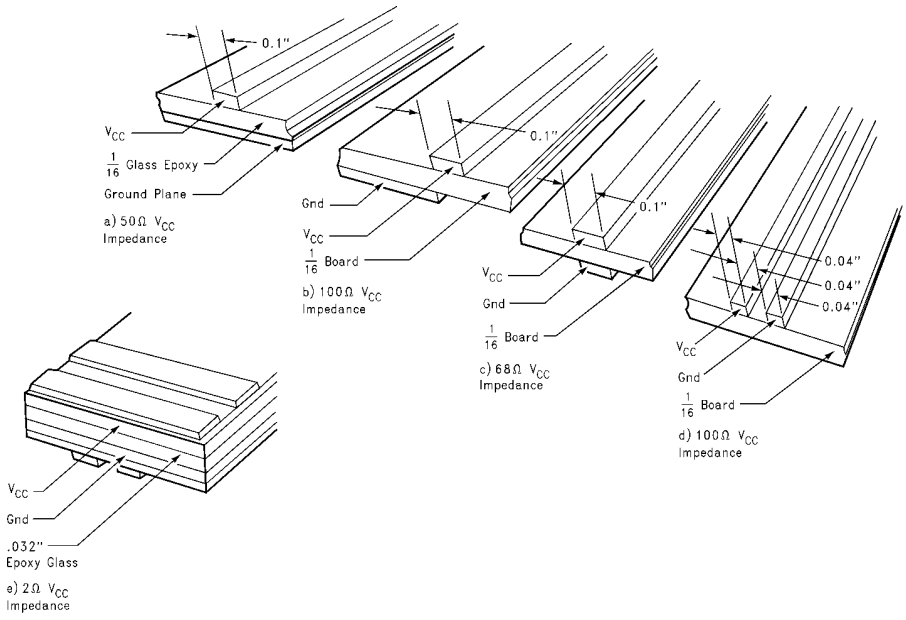


TL/F/12419–55

Buffer Output Sees Net 50Ω Load.
50Ω Load Line on $I_{OH} - V_{OH}$ Characteristic
Shows LOW-to-HIGH Step of Approx. 2.5V.

Worst-Case Octal Drain = 8 × 50 mA = 0.4A

FIGURE 9-33



TL/F/12419–54

FIGURE 9-32

V_{CC} BYPASS CAPACITOR FOR OCTAL DRIVER

A V_{CC} bus with bypass capacitors connected periodically along its length is shown in *Figure 9-34*. Also shown is a current source representing the current demand of the buffer in the preceding application.

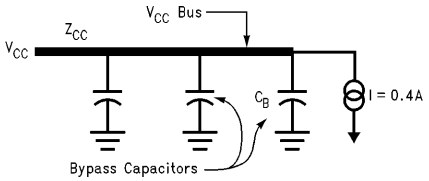
The equations illustrate an approximation method of estimating the size of a bypass capacitor based on the current demand, the drop in V_{CC} that can be tolerated and the length of time that the capacitor must supply the charge. While the current demand is known, the other two parameters must be chosen. A V_{CC} droop of 0.1V will not cause any appreciable change in performance, while a time duration of 3 ns is long enough for other nearby bypass capacitors to help supply charge. If the current demand continues over a long period of time, charge must be supplied by a very large capacitor on the board. This is the reason for the recommendation that a large capacitor be located where V_{CC} comes onto a board. If the buffers are also located near the connector end of the board, the large capacitor helps supply charge sooner.

DESIGN CONSIDERATIONS

GROUND—AN ESSENTIAL LINK

With the advent of Fairchild Advanced Schottky Technology (FAST) with considerably faster edge rates and switching times, proper grounding practice has become of primary concern in printed circuit layout. Poor circuit grounding layout techniques may result in crosstalk and slowed switching rates. This reduces overall circuit performance and may necessitate costly redesign. Also when FAST chips are substituted for standard TTL-designed printed circuit boards, faster edge rates can cause noise problems. The source of these problems can be sorted into three categories:

1. V_{CC} droop due to faster load capacitance charging;
2. Coupling via ground paths adjacent to both signal sources and loads; and
3. Crosstalk caused by parallel signal paths.



TL/F/12419–56

$Q = CV$
$I = C\Delta V/\Delta t$
$C = I\Delta t/\Delta V$
$\Delta t = 3 \times 10^{-9}$

Specify V_{CC} Droop = 0.1V Max.

$$C = \frac{0.4 \times 3 \times 10^{-9}}{0.1} 12 \times 10^{-9} = 0.012\ \mu F$$

Select $C_B \geq 0.02\ \mu F$

Place one bypass capacitor near each buffer package. Distribute other bypass capacitors evenly throughout the logic, one capacitor per two packages.

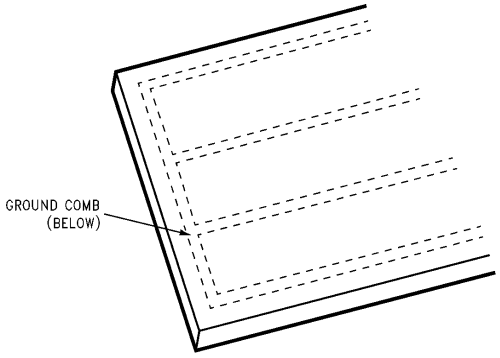
FIGURE 9-34

V_{CC} droop can be remedied with better or more bypassing to ground. The rule here is to place 0.01 μF capacitors from V_{CC} to ground for every two FAST circuits used, as near the IC as possible. The other two problems are not as easily corrected, because PC boards may already be manufactured and utilized. In this case, simply replacing TTL circuits with FAST compatible circuits is not always as easy as it may seem, especially on two-sided boards. In this situation IC placement is critical at high speeds. Also when designing high density circuit layout, a ground-plane layer is imperative to provide both a sufficiently low inductance current return path and to provide electromagnetic and electrostatic shielding thus preventing noise problem 2 and reducing, by a large degree, noise problem 3.

ILLUSTRATIONS

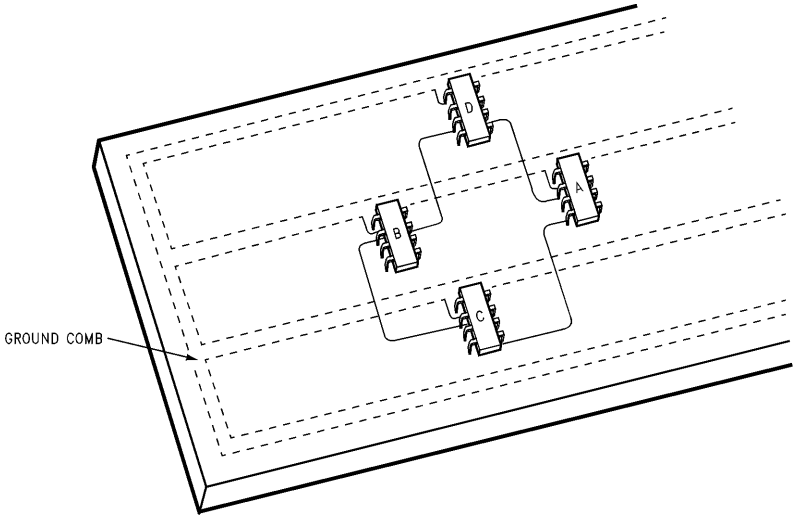
TWO-SIDED PC BOARD LAYOUT

When considering the two-sided PC board, more than one ground trace is often found in a parallel or non-parallel configuration. For this illustration parallel traces tied together at one end are shown. This arrangement is referred to as a ground comb. The ground comb is placed on one side of the PC board while the signal traces are on the other side, thus the two-sided circuit board *(Figure 9-35)*.



TL/F/12419–57

FIGURE 9-35



TL/F/12419–58

FIGURE 9-36

Figure 9-36 illustrates how noise is generated even though there is no apparent means of crosstalk between the circuits. If package A has an output which drives package D input and package B output drives package C input, there is no apparent path for crosstalk since mutual signal traces are remotely located. What is significant, and must be emphasized here, is that circuit packages A and B accept their ground link from the same trace. Hence, circuit A may well couple noise to circuit B via the common or shared portion of the trace. This is especially true at high switching speeds.

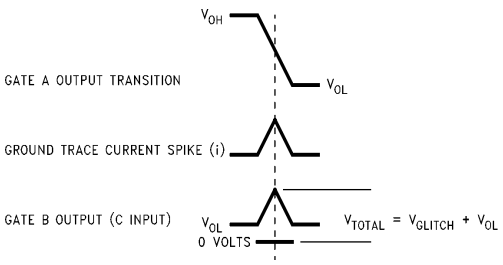
GROUND TRACE COUPLING

Ground trace noise coupling is illustrated by a model circuit in *Figure 9-37*. With the ground comb configuration, the ground strips may be shown to contain distributed inductance, as is indeed the case. Referring to the above illustration we can see that if we switch gate A from HIGH to LOW, the current for the transition is drawn from ground strip number two. Current flows in the direction indicated by the arrow to the common tie point. It can be seen that gate B shares ground strip number two with gate A from the point where gate B is grounded back to the common tie point. This length is represented by L_1. When A switches states there is a current transient which occurs on the ground strip in the positive direction. This current spike is caused by the ground strip inductance and it is ''felt'' by gate B. If gate B is in a LOW state (V_{OL}) the spike will appear on the output since gate B's V_{OL} level is with reference to ground. Thus if gate B's ground reference rises momentarily V_{OL} will also rise. Consequently, if gate B is output to another gate (C in the illustration) problems may arise.

PROBLEM

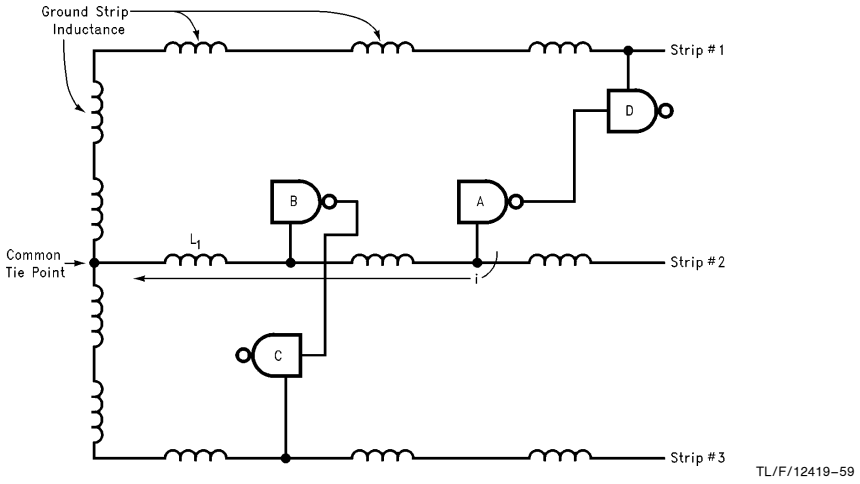
System faults occur if the sum of V_{OL} quiescent level plus current spike amplitude reaches the threshold region of gate C. From this it can be seen that erroneous switching may be transmitted throughout the system. In the illustration the glitch at gate B's output is given by the following formula:

(E9-44) $L_1 (d_i/d_t)$



TL/F/12419–60

FIGURE 9-38

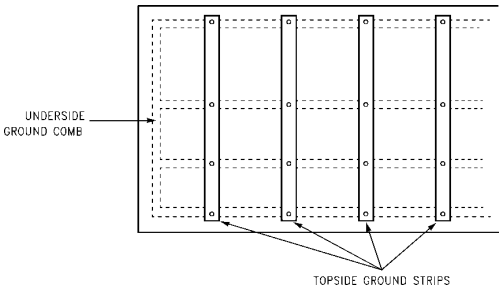


TL/F/12419–59

FIGURE 9-37

Solution

The following sketch *(Figure 9-39)* shows one method of effectively reducing ground path length when using the ground comb layout. By using topside traces to tie the underside ground comb together we can reduce ground strip distributed inductances. Therefore, current transients are significantly smaller or nonexistent in amplitude. In the application of these topside strips, care need not be exercised in their spacing or arrangement. Parallelism is not of paramount importance either. Another advantage is evident: if one or more of these strips is placed between topside signal traces, crosstalk can be eliminated between those traces.



TL/F/12419–61

FIGURE 9-39

BUS DRIVER PACKAGES

An area which warrants special consideration is bus driver/buffer package placement. Here we refer to products such as the 'F240, 'F241, 'F244, 'F540, 'F827 and 'F828. These units have a minimum of eight outputs. A problem may arise if all eight outputs happen to switch from HIGH to LOW or vice versa at the same time. In this case the chance for a large current transient on the ground circuit is apparent. This is possible even on short runs of ground strip (1 to 2 inches). Here, extra care is advised and it is suggested that buffer/driver groups driving backplanes be segregated to one area in the circuit. This area should have its own ground reference. Ideally it should be a ground plane configuration or contain minimal or negligible length ground trace connections.

GENERAL-PURPOSE BOARDS (BREADBOARD)

It is important when breadboarding, creating prototype circuits for evaluation or making special function generators, to use optimum techniques for connecting V_{CC} and ground. Breadboard-type selection is of certain consequence here and should be attended to wisely.

The best choice, when designing with high-speed logic, is board material which has power and ground already connected to circuit trace grids. Boards may offer the designer the option of using IC sockets although these are not recommended for high-speed applications. Socket layout is convenient and may be necessary when special or one-of-a-kind circuits are utilized in initial circuit arrangements. However, when designing with FAST products, consider that sockets increase total lead inductance and interlead capacitance, thus circuit performance may be adversely affected. If boards without ground and power grids must be used or if non-standard pin connections must be accommodated, the use of copper strips or braid is recommended. Copper strip is readily available as shim stock while a brand of solder wick can be used for braid material. Please note here that jumper wires must be avoided because of wire inductance. Wire inductance, like stripline inductance, will slow rise and fall times. Jumpers also promote crosstalk coupling.

NOISE DECOUPLING

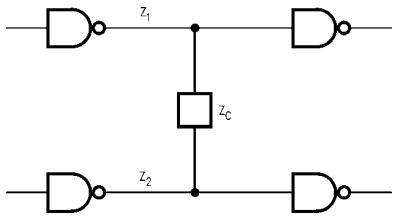
As stated earlier under ''Ground—An Essential Link'', it was noted that the common rule of thumb is to decouple every other FAST package with 0.01 μF capacitors. This is fine for most gates in the majority of applications. However, with buffer/driver packages, decoupling should occur at each package since the possibility of all outputs switching coincidentally exists and can cause large loads on V_{CC}.

An alternative to standard decoupled power traces on the two-sided P.C. board is a product called Q/PAC*. Q/PAC is a low impedance, high capacitance power distribution system which uses wide V_{CC} and ground conductors in close proximity with ceramic insulators to effectively represent integral decoupling capacitors. Packages are available in varying lengths and pinout spacings.

CROSSTALK

Crosstalk is an interference effect of an active signal line on an inactive signal line in close proximity to the active line. There are two forms of crosstalk that are of concern in system design: forward and reverse crosstalk. The causes of both kinds are similar, but the effects are significantly different. Four possible crosstalk conditions can exist at the inactive receiver: (1) a positive pulse on a LOW, (2) a negative pulse on a LOW, (3) a positive pulse on a HIGH, (4) a negative pulse on a HIGH. Of the four previously mentioned conditions (1) and (4) are of major concern in logic systems, and (2) and (3) are less problematic. Crosstalk is caused by a number of interrelated factors which fall into two groups: mutual impedance and velocity difference.

Mutual impedance is caused by the mutual inductance and mutual capacitance distributed along two signal lines in close proximity. The electrical effects are akin to transformer action with well defined polarities. The induced crosstalk voltage pulse is of opposite polarity to the inducing pulse. *Figure 9-40* shows the schematic representation.

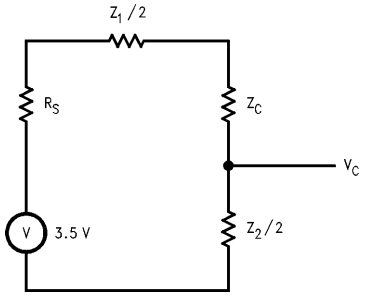


TL/F/12419–62

FIGURE 9-40

*Rogers Corporation
Q/PAC Division, 5750 East McKellips Road
Mesa, AZ 85205 Telephone: 602-830-3370

Here Z_1 and Z_2 represent the adjacent signal line impedances, and Z_C is the mutual impedance coupling the two signal lines. An equivalent circuit is shown in *Figure 9-41*.



TL/F/12419–63

FIGURE 9-41

R_S is the effective source resistance; for V_{OH}, $R_S = 33\Omega$ and V_{OL}, $R_S = 3\Omega$. These are the typical FAST gate sink and source resistances. V_C is the crosstalk voltage and should be adjusted for polarity. The crosstalk voltage can be calculated with the following simplified formula:

$$V_C = \frac{Z_2/2}{R_S + Z_C + Z_1/2 + Z_2/2} \times V_{OUT} \quad \textbf{(E9-45)}$$

Velocity differences are caused when a signal propagates along a conductive medium that is in contact with substances of different dielectric constants, i.e., epoxy glass and air in printed circuit board applications. The different dielectric constants of the materials cause the wave propagating at the epoxy glass interface to be traveling slower than the wave at the air interface. This has the effect of generating a pulse that will couple electrostatically into the adjacent signal line and add to the pulse caused by mutual impedance coupling. The velocity difference pulse will have the same rise time as the signal on the active line and its duration will be twice the difference between the arrival of the wave front in air and the wave front in epoxy glass.

Forward Crosstalk

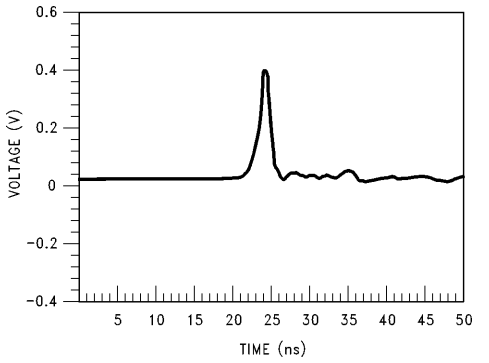
Forward crosstalk is the effect when the active driver and the driver on the non-active line are at the same end: the wave front propagates toward the active and non-active receiver simultaneously. Forward crosstalk is classically attributed almost entirely to velocity differences, but in practice it is a mixture of both velocity difference and mutual impedance effects.

Reverse Crosstalk

Reverse or backward crosstalk is the effect when the active driver and the non-active receiver are at the same end of the signal lines: the wave front propagates toward the active receiver and the non-active driver simultaneously. Reverse crosstalk is due entirely to mutual impedance effects. Forward and reverse crosstalk tests have been performed on both parallel circuit board traces and ribbon cable.

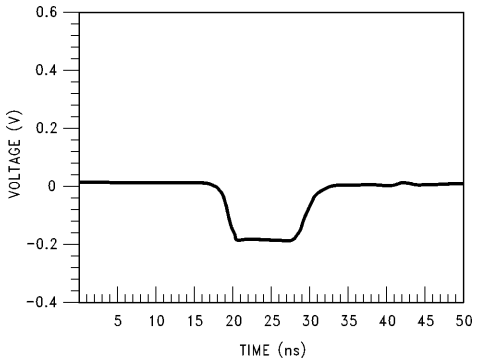
CROSSTALK ON PC TRACE

Crosstalk on printed circuit traces exhibits both velocity difference and mutual impedance effects. This can be seen clearly in *Figure 9-42*. The jig, two 50Ω parallel traces, 34 inches long and 0.100 inches apart, was characterized using a 5V 3 ns rise time signal from a 50Ω source and all traces terminated in 50Ω. *Figures 9-43* through *9-50* show the effects of forward and reverse crosstalk on terminated and unterminated cases using the jig of *Figure 9-42*. All of the cases show no approach to the logic threshold on this test jig; other circuit configurations and impedances may not act in a similar fashion and crosstalk avoidance procedures may have to be taken.



TL/F/12419–64

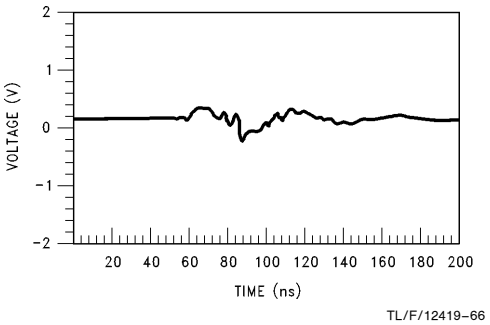
a. Velocity Difference



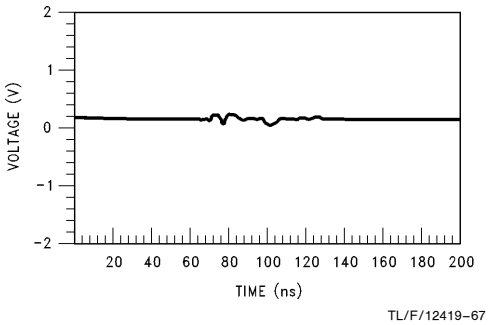
TL/F/12419–65

b. Mutual Impedance

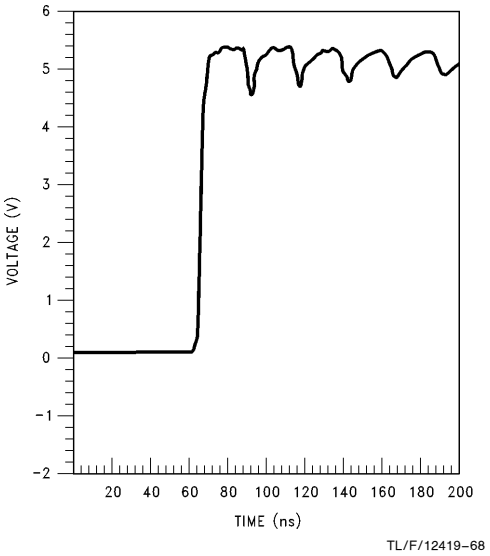
FIGURE 9-42. 34-Inch, 50Ω Crosstalk Jig



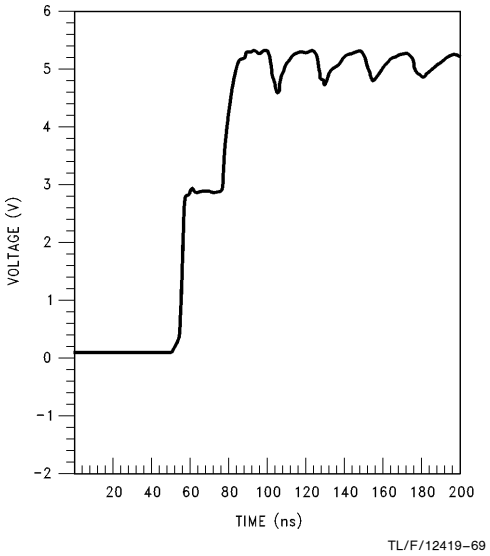
a. Adjacent Receiver



b. Adjacent Driver

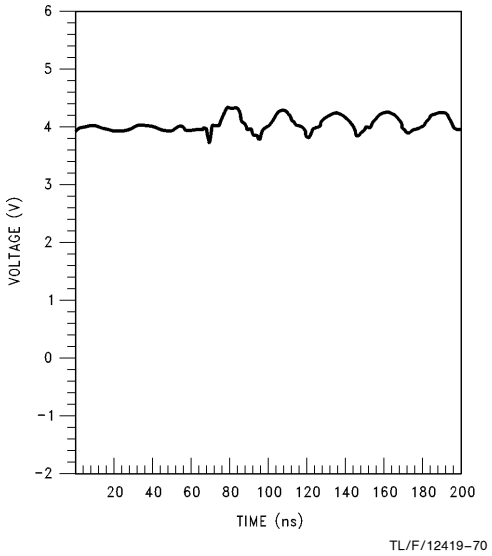


c. Active Receiver

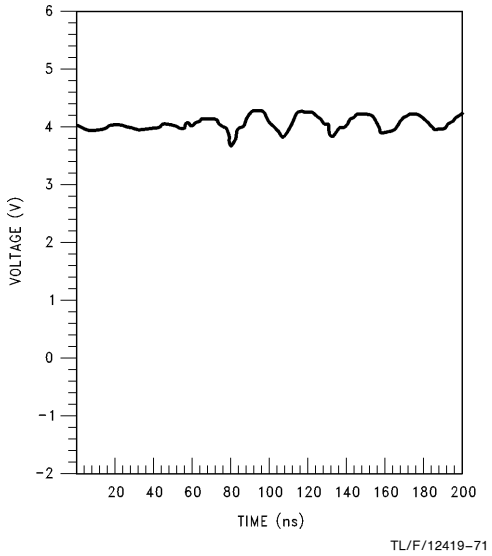


d. Active Driver

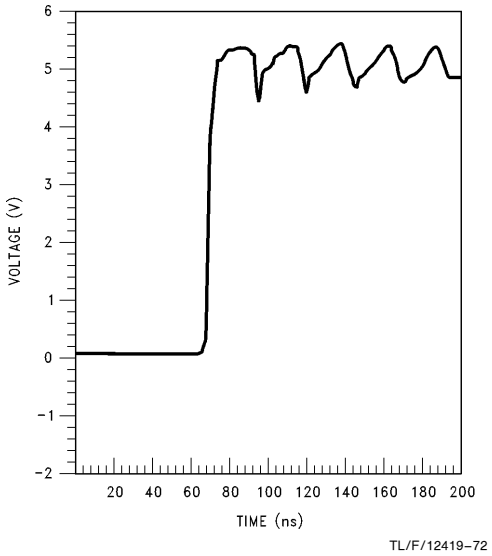
FIGURE 9-43. Reverse PC Board Crosstalk through 34-Inch, 0.100 Trace Unterminated



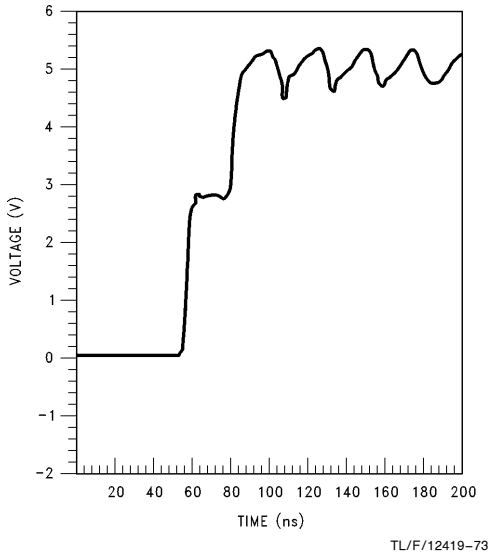
a. Adjacent Receiver



b. Adjacent Driver

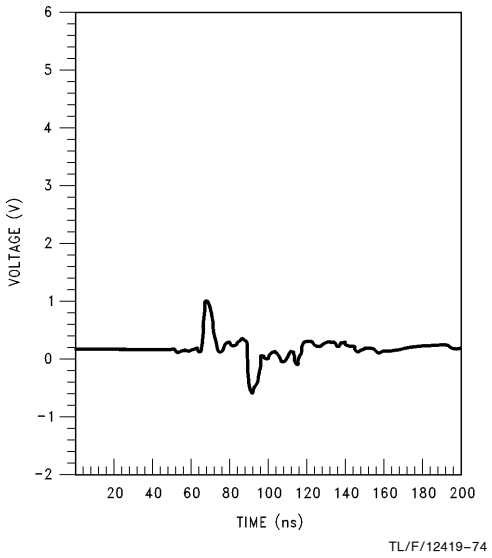


c. Active Receiver



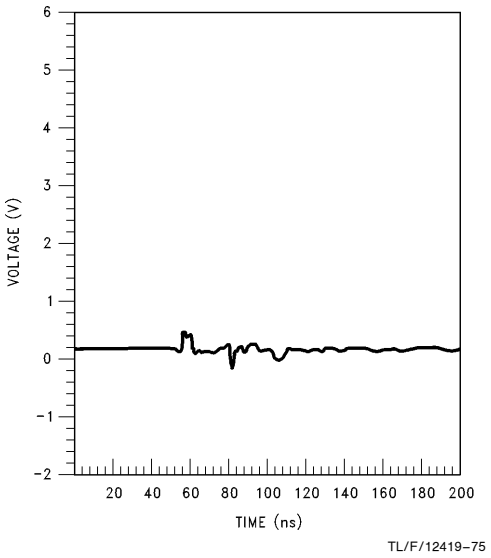
d. Active Driver

FIGURE 9-44. Forward PC Board Crosstalk through 34-Inch Trace Unterminated



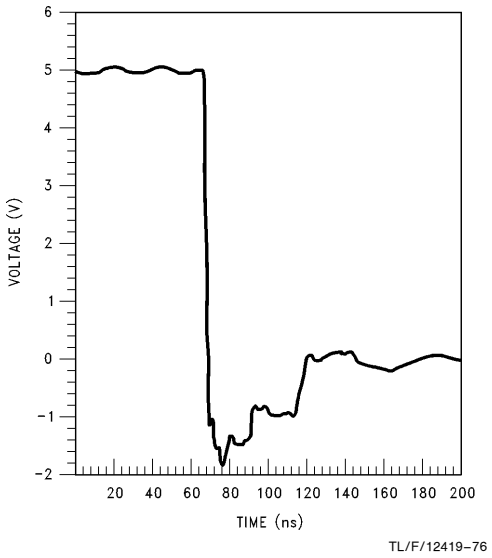
TL/F/12419–74

a. Adjacent Receiver



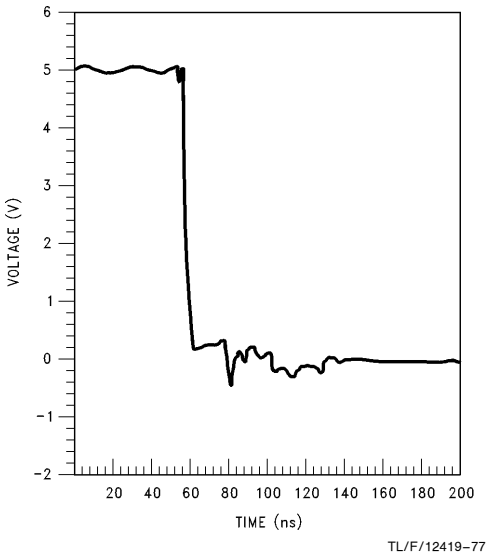
TL/F/12419–75

b. Adjacent Driver



TL/F/12419–76

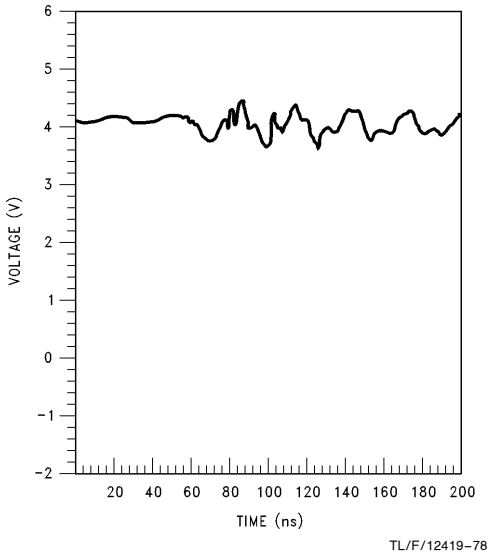
c. Active Receiver



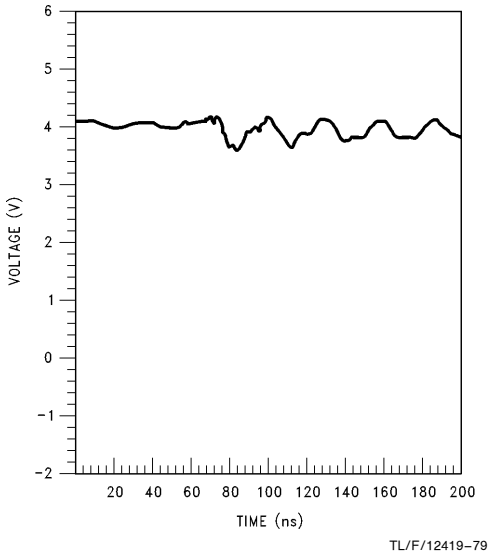
TL/F/12419–77

d. Active Driver

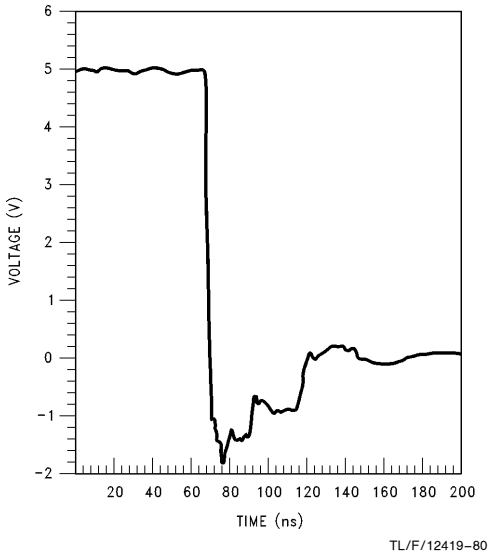
FIGURE 9-45. PC Board Crosstalk through 36-Inch, 0.100 Trace, Forward with No Termination



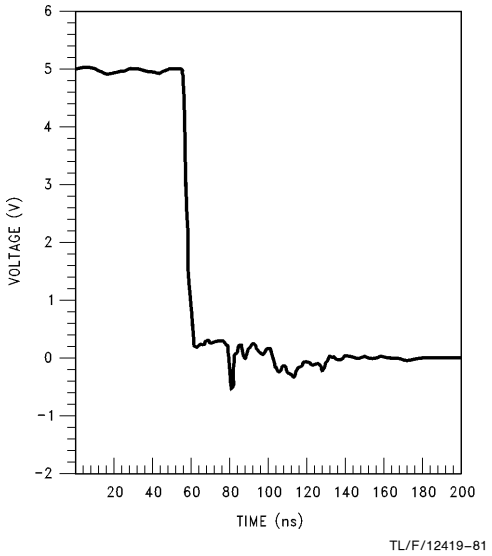
a. Adjacent Receiver



b. Adjacent Driver

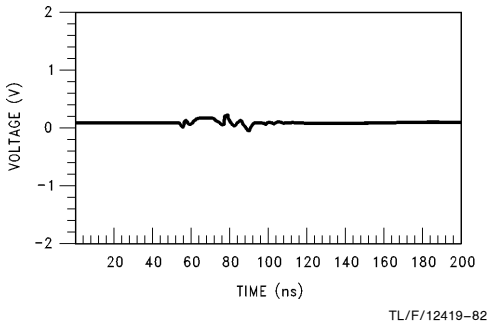


c. Active Receiver



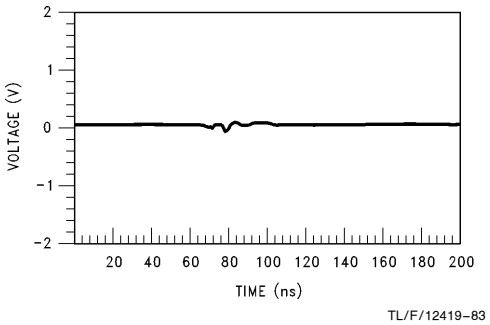
d. Active Driver

FIGURE 9-46. Reverse PC Board Crosstalk through 34-Inch, 0.100 Trace Unterminated



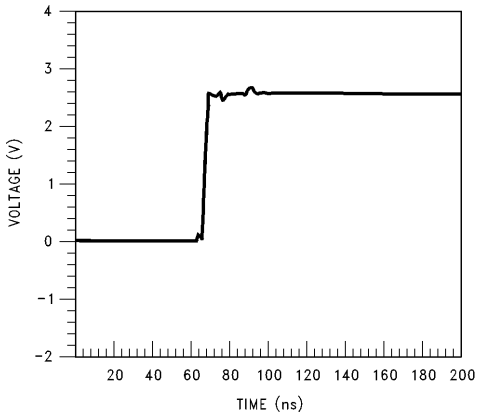
TL/F/12419–82

a. Adjacent Receiver



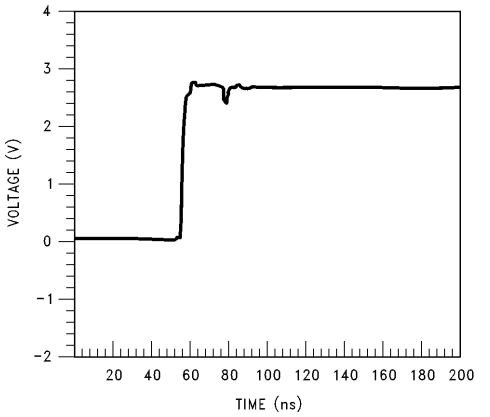
TL/F/12419–83

b. Adjacent Driver



TL/F/12419–84

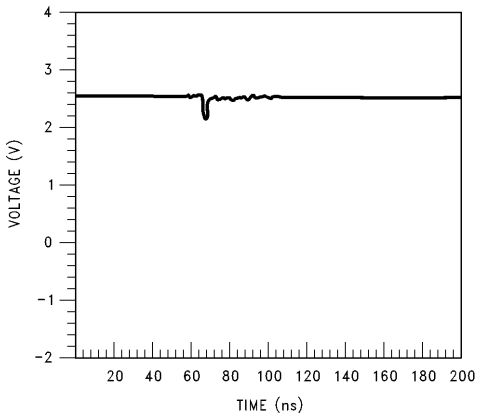
c. Active Receiver



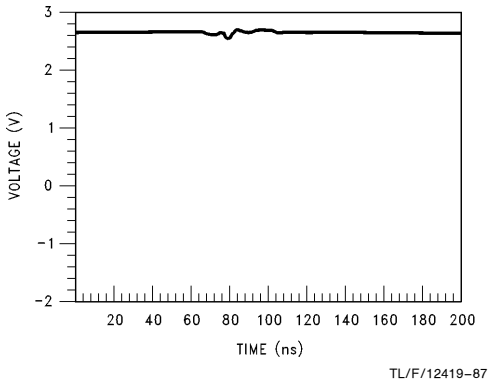
TL/F/12419–85

d. Active Driver

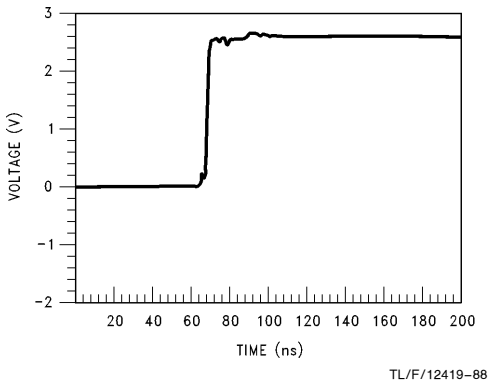
FIGURE 9-47. Reverse PC Board Crosstalk through 34-Inch, 0.100 Trace Terminated



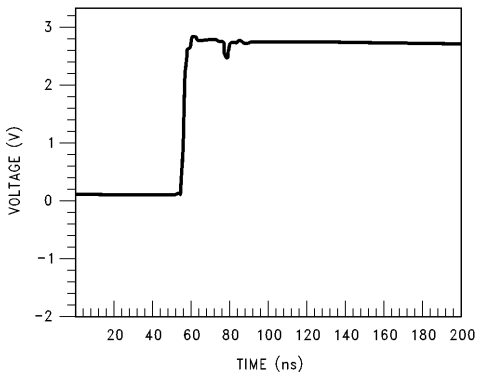
a. Adjacent Receiver



b. Adjacent Driver

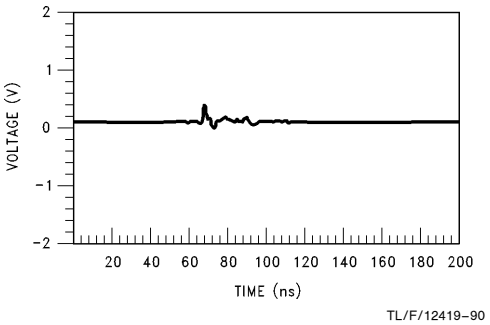


c. Active Receiver



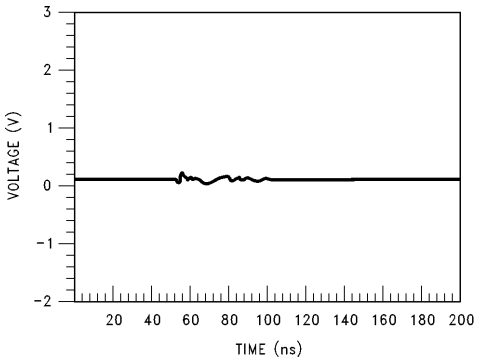
d. Active Driver

FIGURE 9-48. Forward PC Board Crosstalk through 34-Inch Trace Terminated



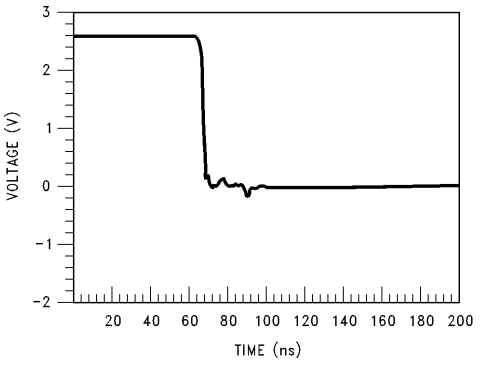
TL/F/12419–90

a. Adjacent Receiver



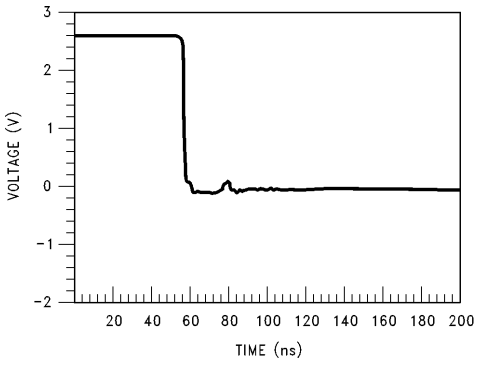
TL/F/12419–91

b. Adjacent Driver



TL/F/12419–92

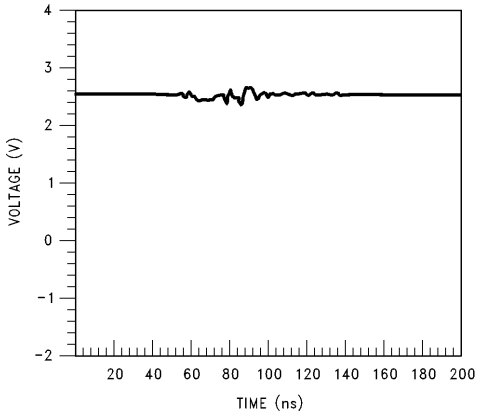
c. Active Receiver



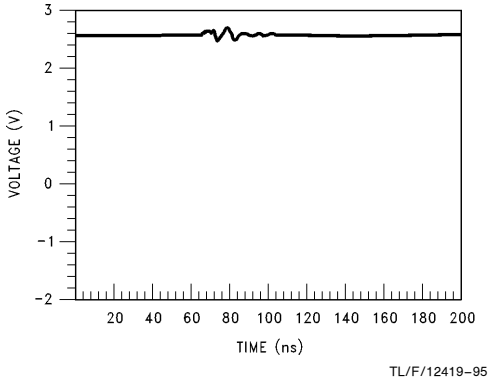
TL/F/12419–93

d. Active Driver

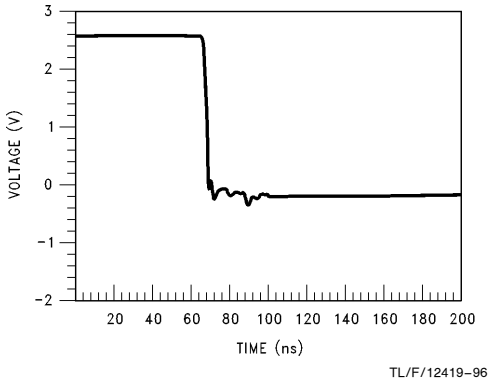
FIGURE 9-49. Forward PC Board Crosstalk through 34-Inch Trace with Termination



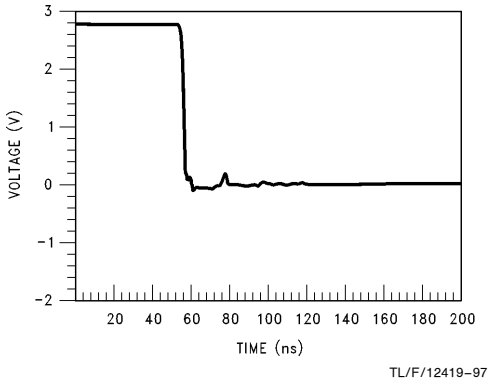
a. Adjacent Receiver



b. Adjacent Driver



c. Active Receiver

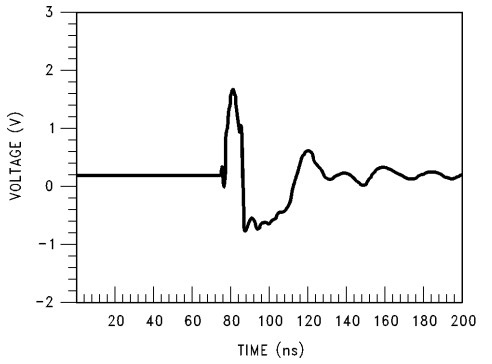


d. Active Driver

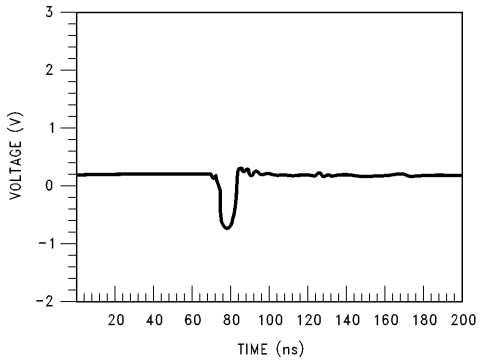
FIGURE 9-50. Reverse PC Board Crosstalk through 34-Inch, 0.100 Trace Terminated

Crosstalk on Ribbon Cable

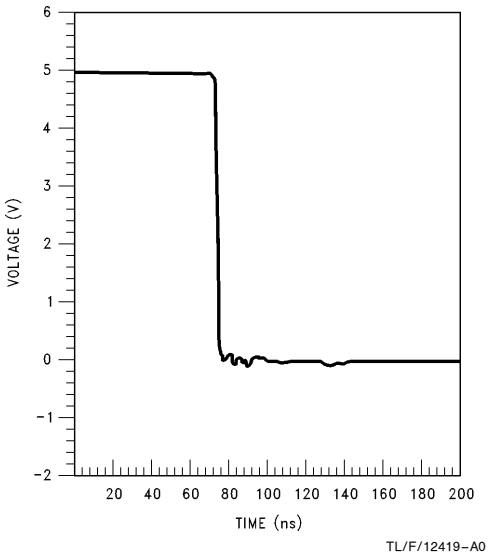
Crosstalk on ribbon cable shows no velocity difference effects—because the cable insulation is a homogeneous medium, all effects are due to mutual impedance. The results of tests on three foot sections of 160Ω ribbon cable are shown in *Figures 9-51* through *9-58*. From these it can be seen that the unterminated lines exhibit large amounts of ringing due to unterminated energy being transferred between lines. Note also that when the adjacent line is in a HIGH state a charge pump effect occurs, forcing the HIGH output above the V_{CC} supply and into a high impedance state with the output structure turned off and the input exhibiting only leakage currents. This high impedance state causes the current that has been induced into the line to reflect from both ends and induce crosstalk back into the active line. This action will continue until damped by circuit resistance and leakages. The charge pump effect will leave the adjacent line at around 7V. If this line is then switched low, twice the normal energy is required to switch the line, thus almost doubling the crosstalk generated in the previous case. The terminated lines show the true magnitude of the crosstalk. Note that when the adjacent line is in the LOW state, the crosstalk will cause the driver output to turn off until clamped by the diode in the output structure.



a. Adjacent Receiver

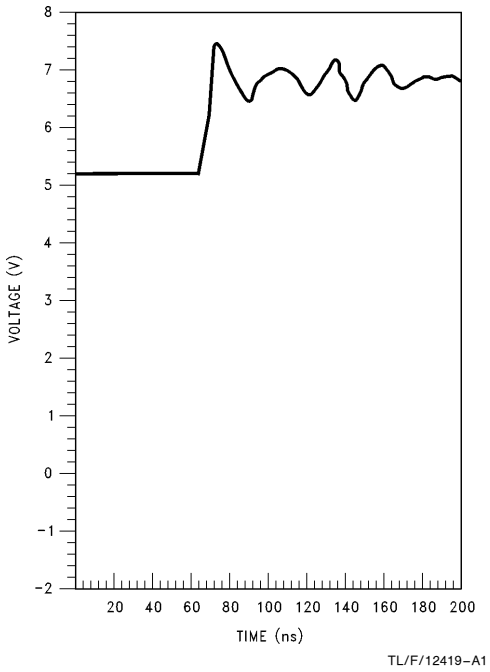


b. Adjacent Driver

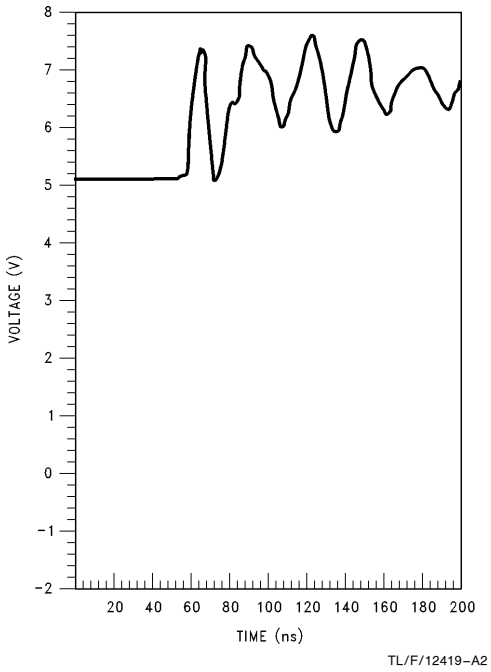


c. Active Driver

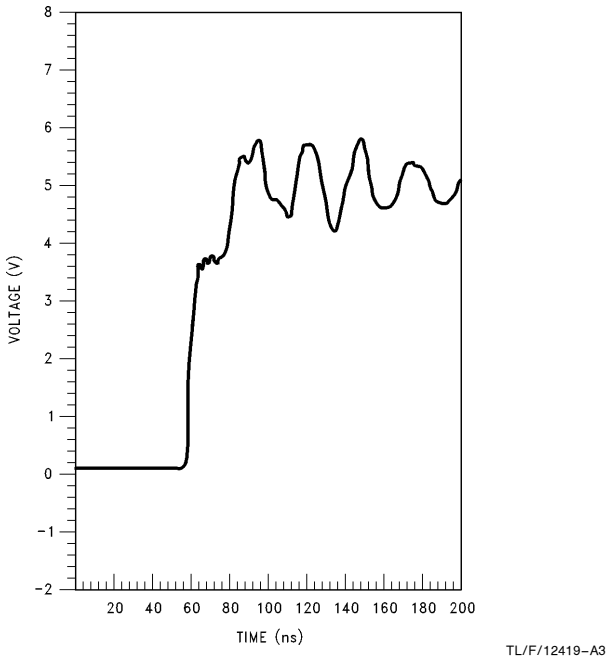
FIGURE 9-51. Forward Crosstalk Using FAST and 3-Foot Ribbion Cable, Unterminated



a. Adjacent Receiver

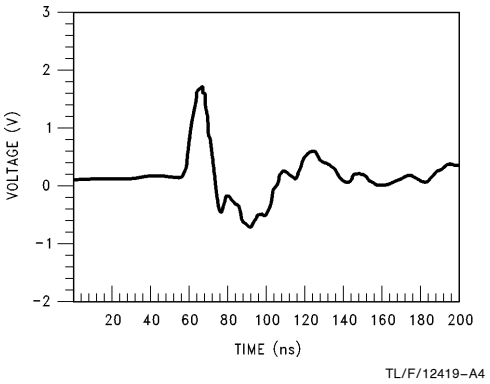


b. Adjacent Driver

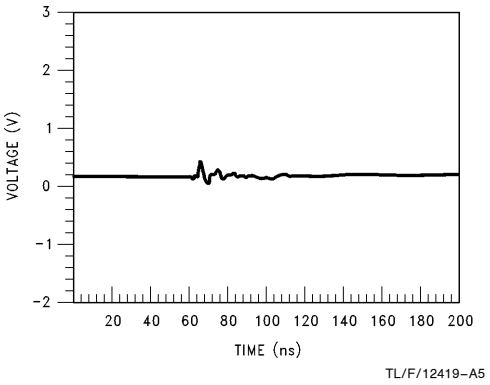


c. Active Driver

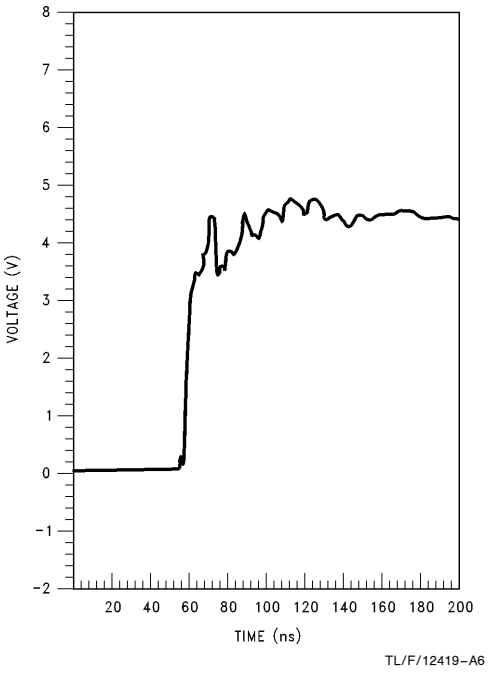
FIGURE 9-52. Forward Crosstalk Using FAST and 3-Foot, 2-Conductor Ribbon Cable, Unterminated



a. Adjacent Receiver

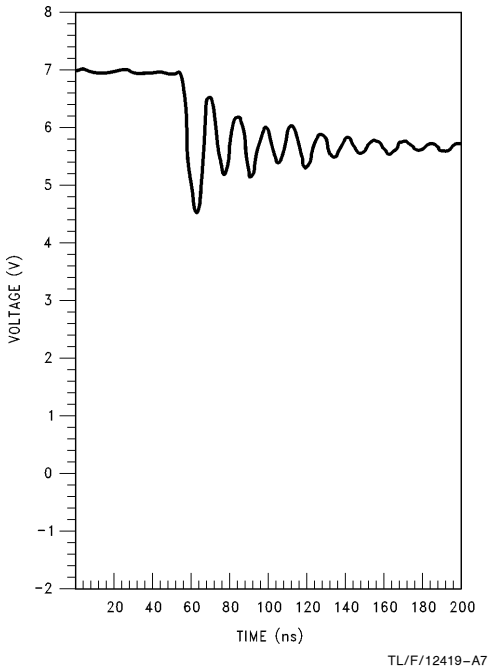


b. Adjacent Driver

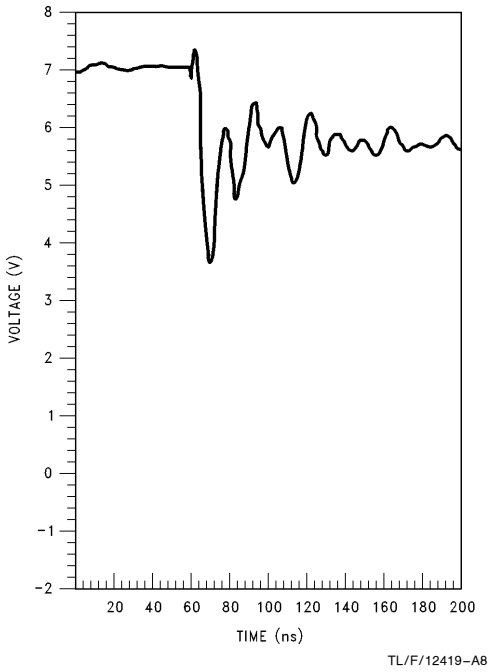


c. Active Driver

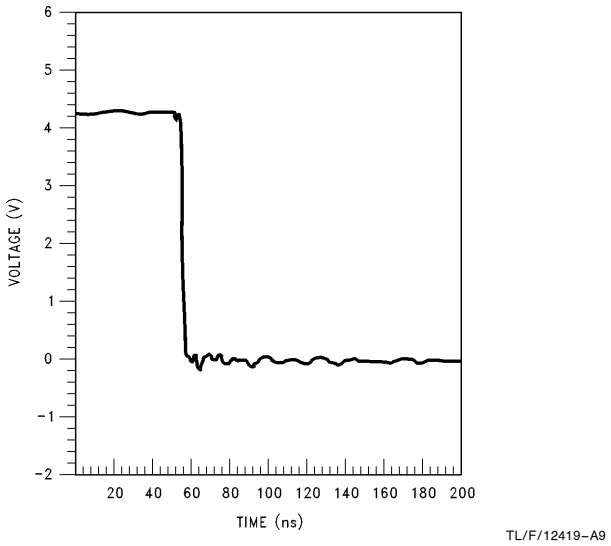
FIGURE 9-53. Reverse Crosstalk Using FAST and 3-Foot, 2-Conductor Ribbon Cable, Unterminated



a. Adjacent Receiver

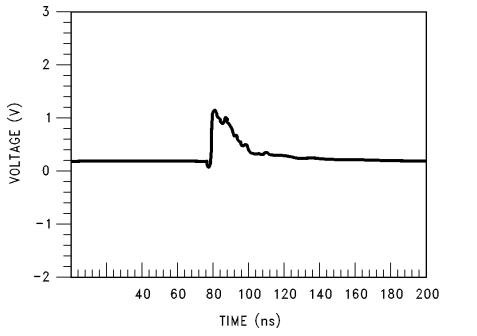


b. Adjacent Driver



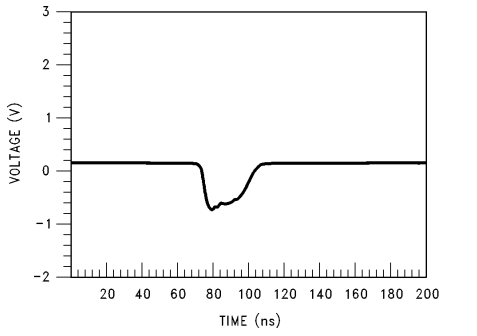
c. Active Driver

FIGURE 9-54. Reverse Crosstalk Using FAST and 3-Foot, 2-Conductor Ribbon Cable, Unterminated



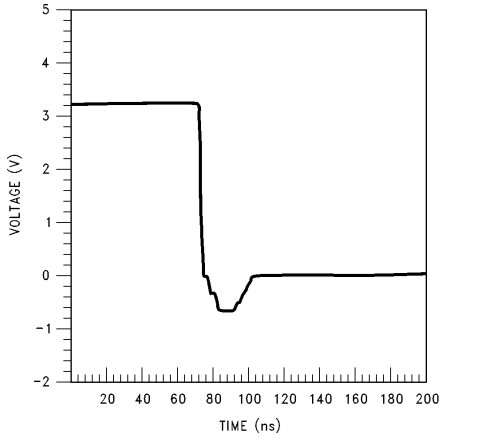
TL/F/12419–B0

a. Adjacent Receiver



TL/F/12419–B1

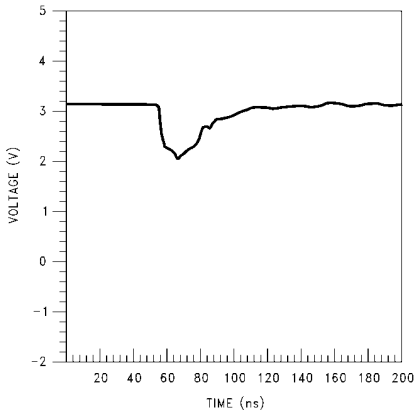
b. Adjacent Driver



TL/F/12419–B2

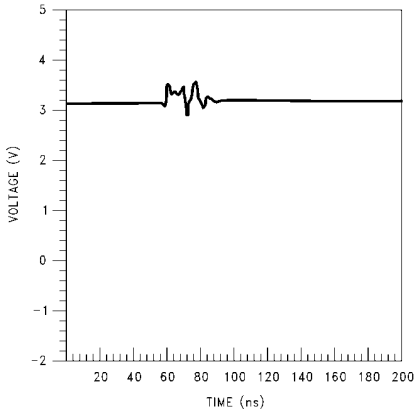
c. Active Driver

FIGURE 9-55. Forward Crosstalk Using FAST and 3-Foot, 2-Conductor Ribbon Cable, Terminated



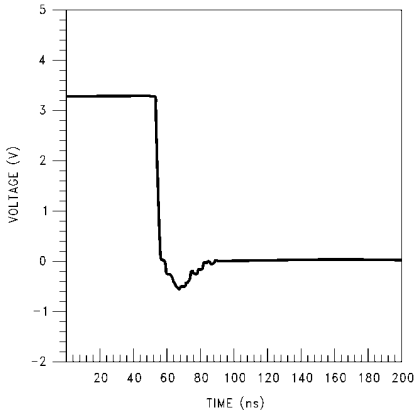
TL/F/12419–B3

a. Adjacent Receiver



TL/F/12419–B4

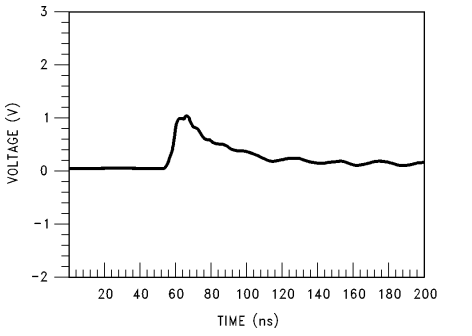
b. Adjacent Driver



TL/F/12419–B5

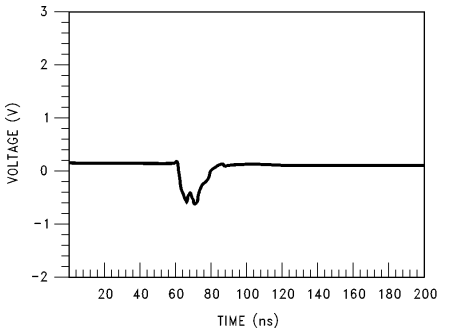
c. Active Driver

FIGURE 9-56. Reverse Crosstalk Using FAST and 3-Foot, 2-Conductor Ribbon Cable, Terminated



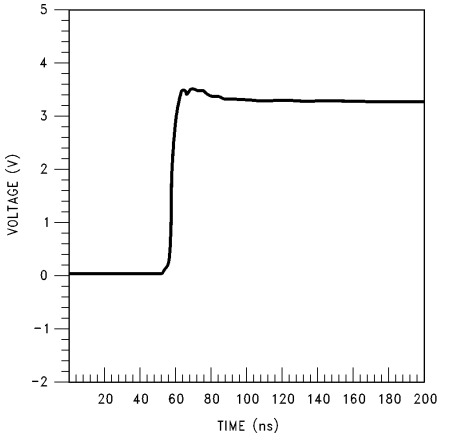
TL/F/12419–B6

a. Adjacent Receiver



TL/F/12419–B7

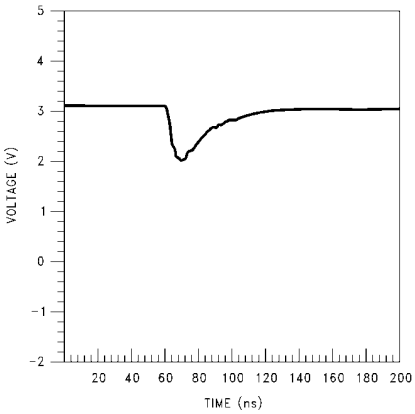
b. Adjacent Driver



TL/F/12419–B8

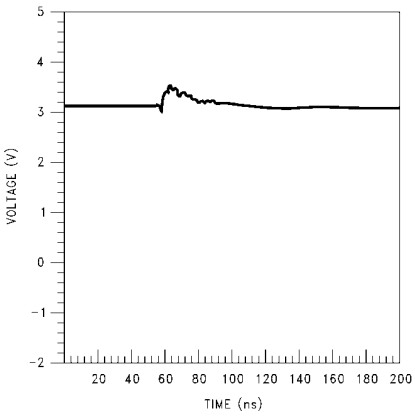
c. Active Driver

FIGURE 9-57. Reverse Crosstalk Using FAST and 3-Foot, 2-Conductor Ribbon Cable, Terminated



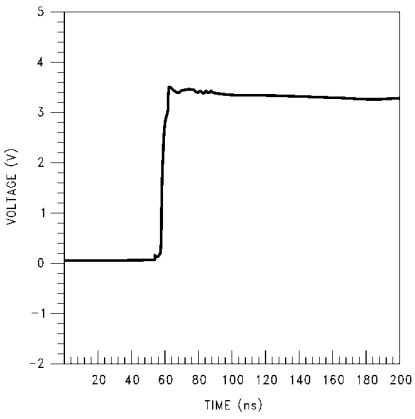
TL/F/12419–B9

a. Adjacent Receiver



TL/F/12419–C0

b. Adjacent Driver



TL/F/12419–C1

c. Active Driver

FIGURE 9-58. Forward Crosstalk Using FAST and 3-Foot, 2-Conductor Ribbon Cable, Terminated

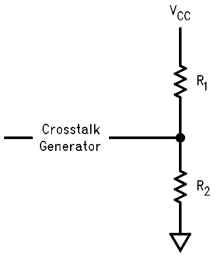
RECOMMENDATIONS

In order to minimize crosstalk it is necessary to consider the causes during the design of systems. Some preventative measures are as follows:

1. Always use maximum allowable spacing between signal lines;
2. Minimize spacing between signal lines and ground lines;
3. Run ground strips alongside either the cross-talker or the cross-listener and between the two when possible;
4. In backplane and wire-wrap applications use twisted pair for sensitive functions such as clocks, asynchronous set or clear, asynchronous parallel load (especially leading to LS inputs); and
5. For ribbon or flat cabling make every other conductor a ground line.

In the case where systems or boards are already built and problems are encountered, some temporary or quick fixes may be utilized. They are:

1. With printed circuit boards, glue a source of ground, either a wire or a copper strip, alongside the cross-talker or cross-listener—preferably between them;
2. For the backplane or wire-wrap situation, spiral a ground wire around the talker to confine its electromagnetic field or around the listener in order to shield it, or do both;
3. Try the split-resistor termination on the offending line *(Figure 9-41)*;



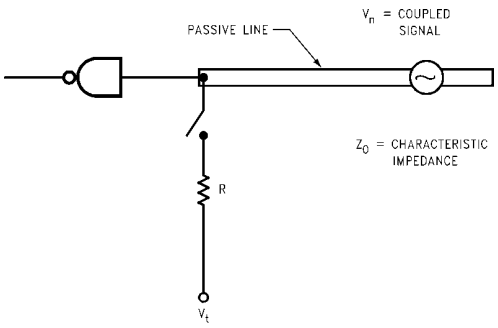
TL/F/12419–C2

where R1/R2 = Equivalent Thevenin Resistance of Termination

FIGURE 9-59

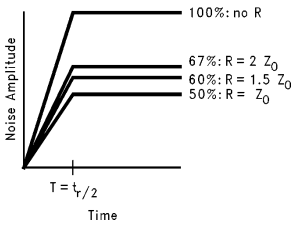
4. Cut the offending crosstalk trace from the PC board and replace it with a wire. In this method reverse and forward crosstalk can be reduced. The line in this case may be lengthened, thereby increasing propagation delays, but a rerouting of the generating signal line may eliminate the crosstalk.

Termination can be used to reduce the effects of crosstalk. It can be seen here that a little termination is better than no termination.



TL/F/12419–C3

FIGURE 9-60



TL/F/12419–C4

FIGURE 9-61

SUMMARY

Trace proximity and coupled trace length are the two main factors which affect the amount of reverse crosstalk that occurs. Therefore, if coupled length is long, noise will be at a maximum. For short lengths, noise may appear only as a short spike which can cause difficulties and even system failures.

When two lines do not run between the same points but are in proximity over part of their length, signal propagation time (line delay) along this coupled length is T. If T is long compared to the rise of the signal on the active line, the crosstalk pulse has time to develop its full amplitude. The trailing edge of the noise pulse is caused by the reflection from the driven end of the passive line. When T is half the rise time, the reflection from the driven end of the passive line arrives and beings to pull the noise pulse down just as it reaches full amplitude. Any value of T less than half the rise time of the active signal will cause a reflection to arrive and oppose the noise pulse voltage before it can reach full amplitude. The noise will therefore be lower in amplitude.

THE CAPACITOR

GENERAL INFORMATION

A capacitor is a component which is capable of storing electrical energy. It consists of conductive plates (electrodes) separated by insulating material which is called the dielectric. A typical formula for determining capacitance is:

(E9-45)
$$C = \frac{0.224\ KA}{t}$$

C = Capacitance (farads)
K = Dielectric constant (Vacuum = 1)
A = Area in square inches
t = Separation between plates in inches (thickness of dielectric)
0.224 = Conversion constant (0.0884 for metric system in cm)

Capacitance—The standard unit of capacitance is the farad. A capacitor has a capacitance of 1 farad when 1 coulomb charges it to 1V. One farad is a very large unit and most capacitors have values in the micro (10^{-6}), nano (10^{-9}), or pico farad (10^{-12}) level.

Dielectric Constant—In the formula for capacitance given above, the dielectric constant of a vacuum is arbitrarily chosen as the number 1. Dielectric constants of other materials are then compared to the dielectric constant of a vacuum. Dielectric constants of some typical materials are as follows:

Ruby Mica	7
Glass	10
Ceramic (Class 1)	5–450
Ceramic (Class 2)	200–12,000
Paper	2.5
Mylar	3
Polystyrene	2.6
Polycarbonate	3
Aluminum Oxide	7
Tantalum Oxide	11

Dielectric Thickness—Capacitance is indirectly proportional to the separation between electrodes. Lower voltage requirements mean thinner dielectrics and greater capacitance per volume.

Area—Capacitance is directly proportional to the area of the electrodes. Since the other variables in the equation are usually set by the performance desired, area is the easiest parameter to modify to obtain a specific capacitance within a material group.

Energy which can be stored in a capacitor is given by the formula:

(E9-46)
$$E = \tfrac{1}{2}\,CV^2$$

E = Energy in joules (watts-sec)
V = Applied voltage
C = Capacitance in farads

A capacitor is a reactive component which reacts against a change in potential across it. This is shown by the equation for the linear charge of a capacitor:

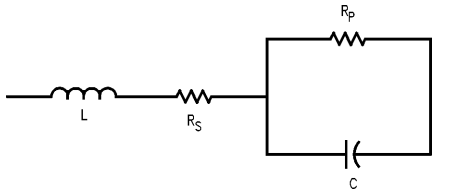
(E9-47)
$$I_{ideal} = C\frac{dV}{dt}$$

where

I = Current
C = Capacitance
dV/dt = Slope of voltage transition across capacitor

Thus an infinite current would be required to instantly change the potential across a capacitor, and the amount of current a capacitor can ''sink'' is given by the above equation.

A capacitor, as a practical device, exhibits not only capacitance but also resistance and inductance. A simplified schematic for the equivalent circuit is:



TL/F/12419–C5

C = Capacitance
R_S = Series Resistance
L = Inductance
R_p = Parallel Resistance

FIGURE 9-62

All the factors shown above are important in the application of capacitors. The inductance determines the usefulness of the capacitor at high frequency, the parallel resistance affects performance in timing and coupling circuits (normally expressed as Insulation Resistance) and the series resistance is a measure of the loss in the capacitor and is a major factor in Power Factor and/or Dissipation Factor.

Since the insulation resistance (R_p) is normally very high, the total impedance of a capacitor is:

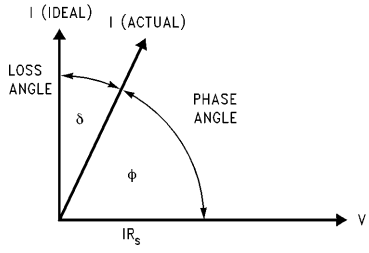
(E9-48)
$$Z = \sqrt{R_S^2 + (X_C - X_L)^2}$$

where

Z = Total Impedance
R_S = Series Resistance
X_C = Capacitive Reactance = $\frac{1}{2}\pi fc$
X_L = Inductive Reactance = $2\pi fL$

The variation of a capacitor's impedance with frequency determines its effectiveness in many applications.

Power Factor and Dissipation Factor are often confused since they are both measures of the loss in a capacitor under AC application and are often almost identical in value. In a ''perfect'' capacitor the current in the capacitor will lead the voltage by 90°.



TL/F/12419–C6

FIGURE 9-63

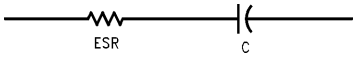
In practice the current leads the voltage by some other phase angle due to the series resistance R_S. The complement of this angle is called the loss angle and:

Power Factor (PF) $=$ cos ϕ or sine δ

Dissipation Factor (DF) $=$ tan δ

For small values of δ the tan and sine are essentially equal, which has led to the common interchangeability of the two terms in the industry.

The term ESR or Equivalent Series Resistance combines all losses, both series and parallel, in a capacitor at a given frequency so that the equivalent circuit is reduced to a simple R-C series connection.



TL/F/12419–C7

FIGURE 9-64

$$\text{Dissipation Factor} = \frac{\text{ESR}}{X_C} = (2\pi\ \text{fc})\ (\text{ESR})$$

(E9-49)

The DF/PF of a capacitor tells what percent of the apparent power input will turn to heat in the capacitor. The watts loss is:

(E9-50) Watts Loss $= (2\pi\ \text{fcE}^2)\ (\text{DF})$

Very low values of dissipation factor are expressed as their reciprocal for convenience. These are called the ''Q'', or Quality factor of capacitors.

Insulation Resistance is the resistance measured across the terminals of a capacitor and consists principally of the parallel resistance R_p shown in the equivalent circuit. As capacitance values and hence the area of dielectric increases, the IR decreases. The product (C $\times$ IR or RC) is often specified in ohm farads or commonly megohm microfarads.

Dielectric Strength is an expression of the ability of a material to withstand an electrical stress. Although dielectric strength is ordinarily expressed in volts, it is actually dependent on the thickness of the dielectric and thus is also more generically a function of volts/mil.

Other specialized factors which may be of interest to the user, especially in high voltage applications, are corona and dielectric absorption.

The phenomenon of Dielectric Absorption is exhibited in the following manner: charging current from a steady unidirectional source continues to flow at a gradually decreasing rate into a capacitor of negligible series resistance for some time after the almost instantaneous charge is completed. A steady value proportional to the capacitor parallel resistance is finally reached. The additional charge apparently is absorbed by the dielectric. Conversely, a capacitor does not discharge instantaneously upon application of a short circuit, but drains gradually after the capacitance proper has been discharged. It is common practice to measure the dielectric absorption by determining the ''reappearing voltage'' which develops across a capacitor at some point in time after it has been fully discharged under short circuit conditions.

Corona is the ionization of air or other vapors which causes them to conduct current. It is especially prevalent in high voltage units but can occur with low voltages as well where high voltage gradients occur. The energy discharged degrades the performance of the capacitor and can in time cause catastrophic failures.

The usual characteristics that are specified for a capacitor include Capacitance, Dissipation Factor or ESR, Insulation Resistance or Leakage Current and Dielectric Strength. The electrical and environmental parameters that are of most interest with respect to these four basic measurements are temperature, voltage and test frequency. The reference temperature for most capacitor measurements is 25°C. Voltage is dependent on the rating applied by the manufacturer and the test frequency typically depends on the class of product.

As the ambient temperature changes, the dielectric constant and hence the capacitance of many capacitors changes. In general, when the dielectric constant is lower, materials tend to change capacitance less with temperature or with relatively predictable changes that are linear with temperature. High dielectric constant meterials tend to have capacitance changes that are non-linear and expressed as percent capacitance change over a temperature range. Increasing temperature usually reduces Insulation Resistance, increases Leakage Current and Power Factor/Dissipation Factor and reduces the voltage rating of the part. Some ceramic capacitors actually exhibit a decrease in DF with increasing temperature. Conversely, reducing temperature normally improves most characteristics.

The effects of applied voltage on capacitors are a prime consideration in use. Capacitance and other parameter changes occur under both AC and DC applied voltages. Even those cases where voltage application does not change the parametric characteristics of a capacitor, the level of voltage applied will determine the life expectancy of the capacitor.

Frequency is the third factor which is of great concern in the application of capacitors. This is an area that is often overlooked by designers. Earlier an equivalent circuit was given for a capacitor. Inductance which is caused by the leads and the electrodes was depicted. As the frequency applied to the capacitor increases it eventually passes through self-resonance and becomes inductive with gradually increasing impedance. Even though a capacitor is beyond the self-resonant point it still blocks DC and has a low impedance and thus is useful in bypass, coupling and many other applications. Care should be taken in feedback, tuning, phase shift and such applications.

CERAMIC CAPACITORS

Ceramic capacitors are the most widely used capacitors. They come in an extremely wide range of mechanical configurations and electrical characteristics. The common mechanical variations are discs, tubulars, feed throughs and monolithics. A 0.01 μF disc is about ½ inch in diameter while the 0.01 μF monolithic chip capacitor is only 0.050″ x 0.075″ x 0.030″. Electrically, ceramic capacitors are broken

into two classes. Class 1 ceramic dielectrics are also called temperature compensating ceramics and feature zero TC and other predictable and relatively linear TC bodies. The insulation resistance is high, the losses are low and the parts are essentially unaffected by voltage or frequency and are usually used for tuned circuits, timing applications and other precision circuits.

Where Class 1 ceramics are completely predictable, Class 2 general purpose ceramics are full of surprises for the unsuspecting engineer. Not only does capacitance change with temperature but the ''high K'' units which are so enticingly small in size may lose 90% of their room temperature capacitance at −55°C. Further care must be exercised when voltage is applied, particularly with monolithic capacitors with their thin dielectrics. AC voltage caused the capacitance to increase and DC voltage causes a capacitance loss. A change in frequency also changes capacitance and DF.

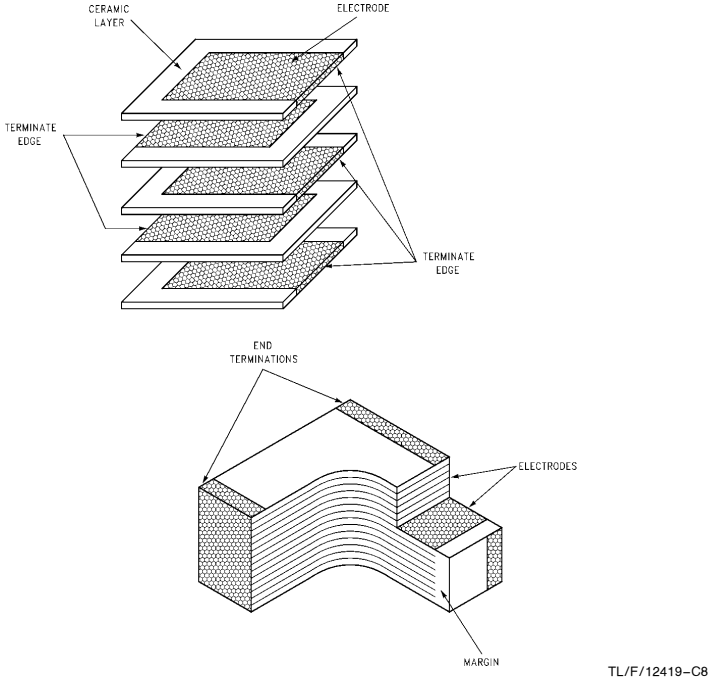
The fact that more ceramic Class 2 capacitors are used than all other types combined proves that the variability of characteristics not only can be overcome by wise selection but can in many cases be an advantage. Considerably more detailed information is given below and a number of articles and booklets are also available on this subject.

The ceramic capacitor is defined as a capacitor manufactured from metallic oxides, sintered at a high temperature. As a general rule, the electrical ceramics used in capacitors are based on complex titanate compounds, principally barium titanate, rare earth titanates, calcium titanates, sodium titanate, etc. Occasionally other materials, such as lead niobiate, may be used.

From a mechanical point of view, ceramic capacitors are manufactured by two basic techniques. One method involves pressing or extruding the ceramic material, firing (sintering) the ceramic and subsequently applying electrodes (typically with silver materials) which are fired onto the ceramic at lower temperatures after the maturation of the ceramic. This is the method employed in the fabrication of single layer devices. The most common form of single layer capacitors is disc capacitors with radial leads or tubular capacitors which are available with axial leads, radial leads or in feed-through form with both bolt and eyelet types being common. There are specialized versions of pressed ceramic capacitors, such as high voltage cartwheels and double cup high voltage units. These and other types may be considered as jumbo size disc pressed units.

The second method of fabricating ceramic capacitors evolved in recent years as a result of the demand for lower voltages and smaller sizes consistent with the advent of semiconductor usage. The miniaturization in the ceramic capacitor area was made possible through the manufacture of monolithic types of ceramic capacitors. These capacitors are manufactured by mixing the ceramic powder in an organic binder (slurry) and casting it by one technique or another into thin layers typically ranging from about 3 mils in thickness down to 1 mil or thinner.

Metal electrodes are deposited onto the green ceramic layers which are then stacked to form a laminated structure. The metal electrodes are arranged so that their terminations alternate from one edge of the capacitor to another. Upon sintering at high temperature the part becomes a monolithic block which can provide extremely high capacitance values in small mechanical volumes. *Figure 9-65* shows a pictorial view of a monolithic ceramic capacitor.



TL/F/12419–C8

FIGURE 9-65

While pressed and extruded ceramic capacitors are in general low cost and provide limited capacitance values, monolithic units are typically smaller in size, feature excellent high frequency characteristics because of the small size and provide considerably higher capacitance values with low voltage ratings.

Ceramic capacitors are available in a tremendous variety of characteristics. Electronic Industries Association (EIA) and the military have established categories to help divide the basic characteristics into more easily specified classes. The basic industry specifications for ceramic capacitors is EIA specification RS-198 and as noted in the general section it specifies temperature compensating capacitors as Class 1 capacitors. These are specified by the military under specification MIL-C-20. General purpose capacitors with non-linear temperature coefficients are called Class 2 capacitors by EIA and are specified by the military under MIL-C-11015 and MIL-C-39014. EIA specifications further include a Class 3 category which is defined as reduced titanates.

Class 1 or temperature compensating capacitors are usually made from mixtures of titanates where barium titanate is normally not a major part of the mix. They have predictable temperature coefficients and in general do not have any aging characteristics. Thus they operate in a manner similar to mica capacitors except for the TC which is controllable. Normally the TCs of Class 1 capacitors are deemed to run between P100 and N750. Class 1 extended temperature compensating capacitors are also manufactured in TCs from negative 1400 through negative 5600, however, these may start developing a slight aging characteristic and voltage susceptibility.

Most TC formulations are available in pressed and extruded construction while only NPO (zero TC) is provided by most manufacturers in monolithic construction. NPO ceramics in monolithic capacitors are available in high enough values to cover most applications requiring extreme stability. With the exception of some NPO capacitors almost all temperature compensating capacitors have a TC curve which is a true curve and not a straight line. The TC tends to become more negative at the cold end than it is from the 25°C reference to +85°C. Both EIA specification RS-198 and military specification MIL-C-20 contain information about curvature. This informatin is contained in Table II. These charts are based on industry accepted standard TC values.

TABLE 9-2. TC Tolerances (Note 1)

Capacitance in pF	NPO	N030	N080	N150	N220	N330	N470	N750	N1500	N2200
−55°C to +25°C in PPM/°C										
10 and Over	+30 −75	+30 −80	+30 −90	+30 −105	+30 −120	+60 −180	+60 −210	+120 −340	+250 −670	+500 −1100
+25°C to +85°C in PPM/°C										
10 and over	±30	±30	±30	±30	±30	±60	±60	±120	±250	±500
Closest MIL-C-20D Equivalent	CG	HG	LG	PG	RG	SH	TH	UJ	None	None
EIA Desig.	C0G	S1G	U1G	P2G	R2G	S2H	T2H	U2J	P3K	R3L

Note 1: Table II indicates the tolerance available on specific temperature characteristics. It may be noted that limits are established on the basis of measurements at +25°C and +85°C and that TC becomes more negative at low temperature. Wider tolerances are required on low capacitance values because of the effects of stray capacitance.

General purpose ceramic capacitors are called Class 2 capacitors and have become extremely popular because of the high capacitance values available in very small size. Class 2 capacitors are ''ferro electric'' and vary in capacitance value under the influence of the environmental and electrical operating conditions. Class 2 capacitors are affected by temperature, voltage (both AC and DC), frequency and time. Temperature effects for Class 2 are exhibited as non-linear capacitance changes with temperature.

In specifying capacitance change with temperature, EIA expresses capacitance change over an operating temperature range by a 3-symbol code. The first symbol represents the cold temperature end of the range, the second represents the upper limit of the operating range and a third symbol represents the capacitance change allowed over the operating temperature range. Table 9-3 provides a detailed explanation of the EIA system. As an example, a capacitor with a characteristic X7R would change ±15% over the temperature range −55°C to +125°C and is often identical to military characteristics BX. Parts with characteristics are also sometimes called ''K1200'' but most manufacturers now use higher dielectric constants than 1200 so the term is now taken to mean only X7R and is commonly called semi-stable material.

A Z5U temperature characteristic is also extremely popular. It allows a capacitance change of +22% to −56% over the temperature range of +10°C to +85°C, and is usually made with materials with a dielectric constant in the range of 5000 to 10,000.

EFFECTS OF VOLTAGE

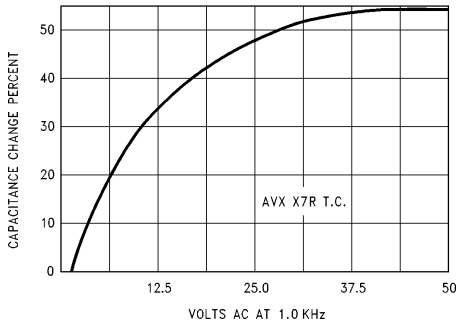
Whereas variations in temperature affect all of the parameters of ceramic capacitors, voltage basically affects only the capacitance and dissipation factor. The application of DC voltage reduces both the capacitance and dissipation factor while the application of an AC voltage within a reasonable range tends to increase both capacitance and dissipation factor readings. If a high enough AC voltage is applied, eventually it will reduce capacitance just as a DC voltage will. However, the application of this high an AC voltage is normally not encountered.

TABLE 9-3

MIL-C-11015D Code			EIA Code Percent Capacity Change Over Temperature Range	
Symbol	**Temperature Range**		**RS198**	**Temperature Range**
A	−55°C to +85°C		X7	−55°C to +125°C
B	−55°C to +125°C		X5	−55°C to +85°C
C	−55°C to +150°C		Y5	−30°C to +85°C
			Z5	+10°C to +85°C
Symbol	**Cap. Change Zero Volts**	**Cap. Change Rated Volts**	**Code**	**Per Cent Capacity Change**
R	+15%, −15%	+15%, −40%	D	±3.3%
			E	±4.7%
W	+22%, −56%	+22%, −66%	F	±7.5%
			P	±10%
X	+15%, −15%	+15%, −25%	R	±15%
			S	±22%
Y	+30%, −70%	+30%, −80%	T	+22%, −33%
			U	+22%, −56%
Z	+20%, −20%	+20%, −30%	V	+22%, −82%
Temperature characteristic is specified by combining range and change symbols, for example BR or AW. Specification slash sheets indicate the characteristic applicable to a given style of capacitor.			Example—A capacitor is desired with the capacitance value at 25°C to increase no more than 7.5% or decrease no more than 7.5% from −30°C to +85°C. EIA Code will be Y5F.	

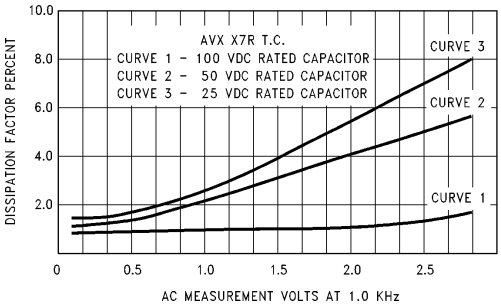
Since the magnitude of the effect is dependent on the thickness of the dielectric versus the voltage applied (volts per mil) the curve is based on percent of rated voltage in order to give a basic idea of the order of magnitude of the changes in question. *Figure 9-66* shows the effects of AC voltage.

These are of major significance in some applications but are perhaps of even more significance when it comes to measuring the capcitance value and dissipation factor of the capacitors. Capacitor specifications specify the AC voltage at which to measure (normally 1 VAC) and application of the wrong voltage can cause spurious readings. *Figure 9-67* gives the voltage coefficient of dissipation factor for AC based on 1000 cycles reading a 1 kHz readings. Applications of different frequencies will affect the percentage changes versus voltages.



TL/F/12419–C9

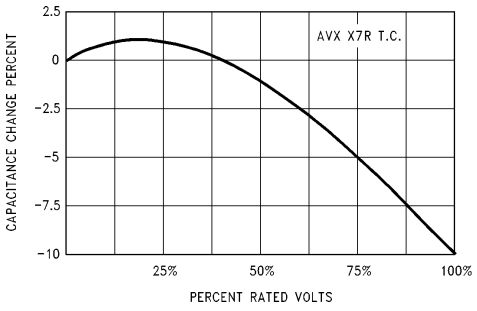
FIGURE 9-66



TL/F/12419–D0

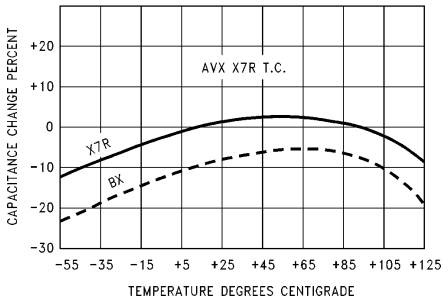
FIGURE 9-67

The effect of the application of DC voltage is once again dependent on the thickness of the dielectric (volts per mil) and is shown in a similar manner in *Figure 9-68*. As will be noted in general, the voltage coefficient is more pronounced for higher K dielectrics. These figures are shown for room temperature conditions. Of considerable interest to the user is a combination characteristic known as voltage temperature limit which shows the effects of rated voltage over the operating temperature range. *Figure 9-69* shows a capacitor of military specification type BX.



TL/F/12419–D1

FIGURE 9-68

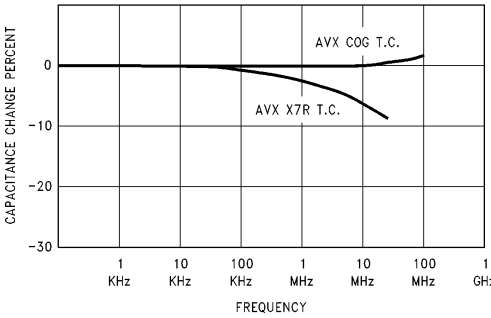


TL/F/12419–D2

FIGURE 9-69

EFFECTS OF FREQUENCY

Frequency affects capacitance and dissipation factor as is the case with voltage. Curves of capacitance change and dissipation factor change with normal type ceramics are shown in *Figure 9-70* and *9-71*.



TL/F/12419–D3

FIGURE 9-70

Variation of impedance with frequency is an important consideration for decoupling capacitor applications. Lead length, lead configuration and body size all affect the impedance level as well as the ceramic formulation variations.

Special ceramic materials are also made for use at extremely high frequencies.

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