

SERVICE MANUAL

BBK921D



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1.SAFETY PRICAUTIONS

1.1 GENERAL GUIDELINES

- 1.When servicing,observe the original lead dress.if a short circuit is found,replace all parts which have been overheated or damaged by the short circuit.**
- 2.After servicing,see to it that all the protective devices such as insulation bamiers,insulation papers shields are properly installed.**
- 3.After servicing,make the following leakage current checks to prevent the customer from being exposed to thock hazards.**

2.PREVENTION OF ELECTRO STATIC DISCHARGE(ESD) TO ELECTROSTATECALLY SENSITIVE(ES) DEVICES

Some semiconductor(solid state)devices can be damaged easily by static electricity.Such components commonly are called Electrostatically Sensitive(ES)Devices.Examples of typical ES devices are integrated circuits and some field-effect transistorsand semiconductor chip components.The following techniques should be used to help reduce the incidence of component damage caused by electro static discharge(ESD).

- 1.Immediately before handling any semiconductor component or semiconductor-equipped assembly,drain off any ESDon your body by touching a known earth ground.Alteatively,obtain and wear a commercially availabel discharging ESD wrist strap,which should be removed for potential shock reasons prior to applying power to the unit under test.**
- 2.After removing an electrical assembly equipped with ES devices,place the assembly on a conductive surface such as alminum foil,to prevent electrostatic charge buildup or exposure of the assembly.**
- 3.Use only a grounded-tip soldering iron to solder or unsolder ES devices.**
- 4.Use only an anti-static solder removal device.Some solder removal devices not classified as anti-static (ESD protected)can generate electrical charge sufficient to damage ES devices.**
- 5.Do not use freon-propelled chemicals.These can generate electrical charges sufficient to damage ES devices.**
- 6.Do not remove a replacement ES device from its protective package until immediately before you are ready to install if.(Most replacement ES devices are packaged with leads electrically shorted together by conductive foam,alminum foil or comparable conductive material).**
- 7.Immediately before removing the protective material from the leads of a aeplacement ES device,touch the protective material to the chassis or circuit assembly into which the device will be installed.**

Caution

Be sure no power is applied to the chassis or circuit,and observe all other safety precautions.

- 8.Minimize bodily motions when handling unpackaged replacement ES devices.(Otherwise hamless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity(ESD)**

notice (1885x323x2 tiff)

IMPORTANT SAFETY NOTICE

There are special components used in this equipment which are imortant for safety.
These parts are marked by Δ in the schematic diagrams, Exploded Views and replacement parts list. It is essential that these critical parts should be replaced with manufacturer's specified parts to prevent shock, fire, or other hazards. Do not modify the original design without permission of manufacturer.

3. Precaution of Laser Diode

CAUTION:

This product utilizes a laser diode with the unit turned "on", invisible laser radiation is emitted from the pickup lens.

Wave length: 780 nm

Maximum output radiation power from pickup: 100 μ

W/VDE

Laser radiation from the pickup lens is safety level, but be sure the followings:

1. Do not disassemble the optical pickup unit, since radiation from exposed laser diode is dangerous.
2. Do not adjust the variable resistor on the pickup unit. It was already adjusted.
3. Do not look at the focus lens using optical instruments.
4. Recommend not to look at pickup lens for a long time.

ACHTUNG:

Dieses Produkt enthält eine Laserdiode.

Im eingeschalteten Zustand wird unsichtbare

Leserstrahlung von der Laserinheit abgestrahlt.

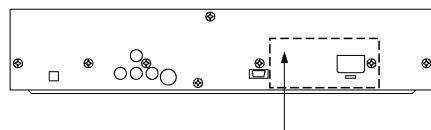
Wellenlänge: 780 nm

Maximale Strahlungsleistung der Lasereinheit: 100 μ

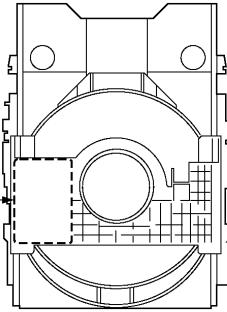
W/VDE

Die Strahlung der Lasereinheit ungefährlich, wenn folgende Punkte beachtet werden:

1. Die Lasereinheit nicht zerlegen, da die Strahlung an der freigelegten Laserdiode gefährlich ist.
2. Den werkseitig justierten Einstellregler der Lasereinheit nicht verstören.
3. Nicht mit optischen Instrumenten in die Fokussierlinien blicken.
4. Nicht über längere Zeit in die Fokussierlinien blicken.



Product complies with DHHS
rules 21 CFR Subchapter J in
effect at date of manufacture.
Matsushita Electric Industrial
Co., Ltd.
Kadoma, Osaka, Japan



CAUTION!

THIS PRODUCT UTILIZES A LASER.

USE OF CONTROLS OR ADJUSTMENTS OR PERFORMANCE OF PROCEDURES OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.

Control Button Locations and Explanations

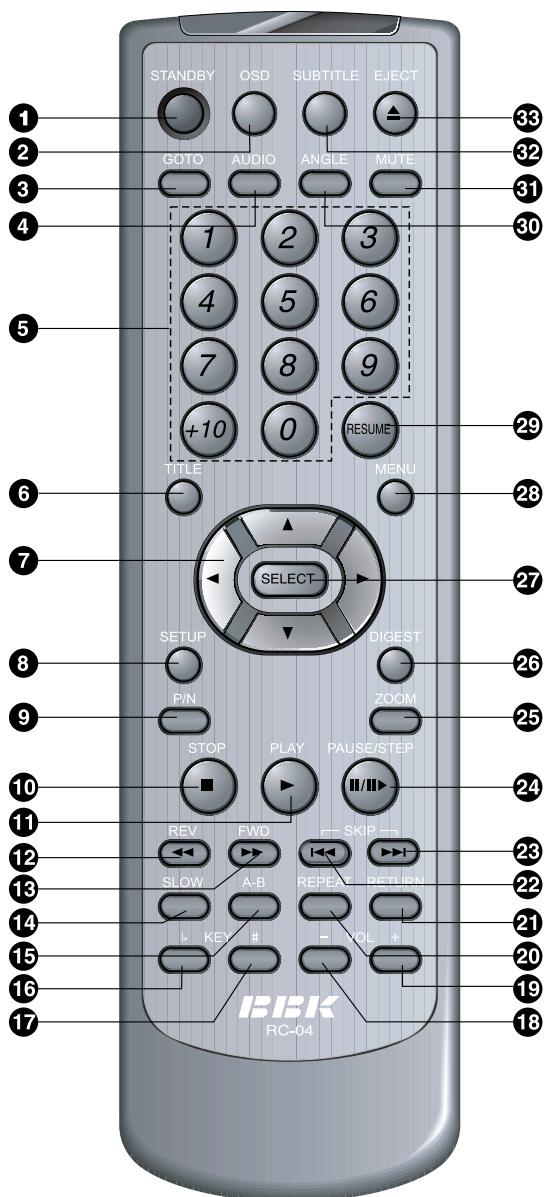
Front Panel Illustration



- | | | |
|----------------------------|--------------------------|-----------------------------|
| ① POWER switch | ⑥ NEXT button | ⑪ VFD display window |
| ② Disc tray | ⑦ FWD button | ⑫ STOP button |
| ③ OPEN/CLOSE button | ⑧ MIC 1 jack | ⑬ PLAY button |
| ④ AUDIO button | ⑨ MIC 2 jack | ⑭ PAUSE button |
| ⑤ REV button | ⑩ MIC VOLUME knob | ⑮ PREV button |

Control Button Locations and Explanations(Continued)

Remote Control Illustration



- ① **STANDBY** Button
Press once to stand by, Press twice to play.
- ② **OSD** Button
Display or hide disc information.
- ③ **GOTO** Button
Play from the desired location.
- ④ **AUDIO** Button
Change the audio language or audio channel.
- ⑤ **NUMBER** Buttons
DVD titles.
- ⑥ **TITLE** Button
Normal playback.
- ⑦ **CURSOR** Buttons
Function setup.
- ⑧ **SETUP** Button
Function setup.
- ⑨ **P/N** Button
Switch the TV system between PAL, NTSC and AUTO.
- ⑩ **STOP** Button
Stop playback.
- ⑪ **PLAY** Button
Normal playback.
- ⑫ **REV** Button
Fast backward play.
- ⑬ **FWD** Button
Fast forward play.
- ⑭ **SLOW** Button
Slow play.
- ⑮ **A-B** Button
Repeat the select.
- ⑯ **KEY ♯** Button
Fall tone.
- ⑰ **KEY #** Button
Rise tone.
- ⑱ **VOLUME-**
Decrease volume.
- ⑲ **VOLUME+**
Increase volume.
- ⑳ **REPEAT** Button
Repeat play.
- ㉑ **RETURN** Button
Back to the previous menu.
- ㉒ **PREV** Button
Skip backward.
- ㉓ **NEXT** Button
Skip forward.
- ㉔ **PAUSE/STEP** Button
Pause or play frame by frame.
- ㉕ **ZOOM** Button
Zoom in the displayed frame.
- ㉖ **DIGEST** Button
9-Picture view.
- ㉗ **SELECT** Button

① STANDBY Button

Press once to stand by, Press twice to play.

② OSD Button

Display or hide disc information.

③ GOTO Button

Play from the desired location.

④ AUDIO Button

Change the audio language or audio channel.

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DVD titles.

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Pause or play frame by frame.

㉕ ZOOM Button

Zoom in the displayed frame.

㉖ DIGEST Button

9-Picture view.

㉗ SELECT Button

5.PREVENTION OF STATIC ELECTRICITY DISCHARGE

The laser diode in the traverse unit (optical pickup) may break down due to static electricity of clothes or human body. Use due caution to electrostatic breakdown when servicing and handling the laser diode.

5.1.Grounding for electrostatic breakdown prevention

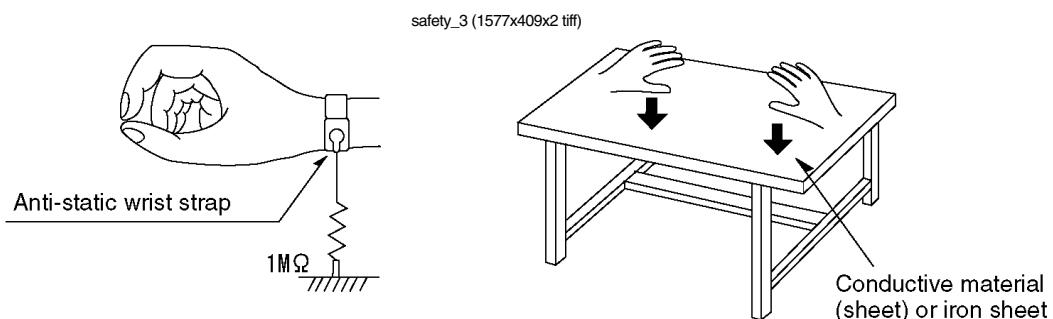
Some devices such as the DVD player use the optical pickup(laser diode)and the optical pickup will be damaged by static electricity in the working environment.Proceed servicing works under the working environment where grounding works is completed.

5.1.1. Worktable grounding

1.Put a conductive material(sheet)or iron sheet on the area where the optical pickup is placed, and ground the sheet.

5.1.2.Human body grounding

1 Use the anti-static wrist strap to discharge the static electricity from your body.



5.1.3.Handing of optical pickup

1.To keep the good quality of the optical pickup maintenance parts during transportation and before installation, the both ends of the laser diode are short-circuited. After replacing the parts with new ones, remove the short circuit according to the correct procedure.(See this Technical Guide).

2.Do not use a tester to check the laser diode for the optical pickup .Failure to do so will damage the laser diode due to the power supply in the tester.

5.2.Handing precautions for Traverse Unit (Optical Pickup)

1.Do not give a considerable shock to the traverse unit(optical pickup)as it has an extremely high-precise structure.

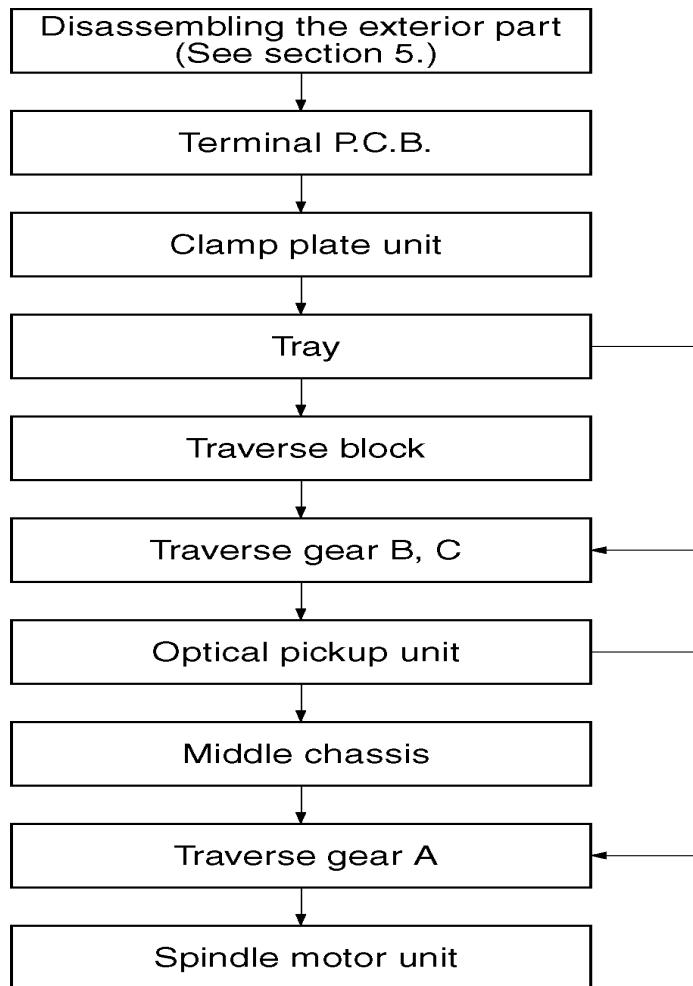
2.When replacing the optical pickup, install the flexible cable and cut it short land with a nipper.See the optical pickup replacement procedure in this Technical Guide.Before replacing the traverse unit, remove the short pin for preventing static electricity and install a new unit.Connect the connector as short times as possible.

3.The flexible cable may be cut off if an excessive force is applied to it.Use caution when handling the cable.

4.The half-fixed resistor for laser power adjustment cannot be adjusted.Do not turn the resistor.

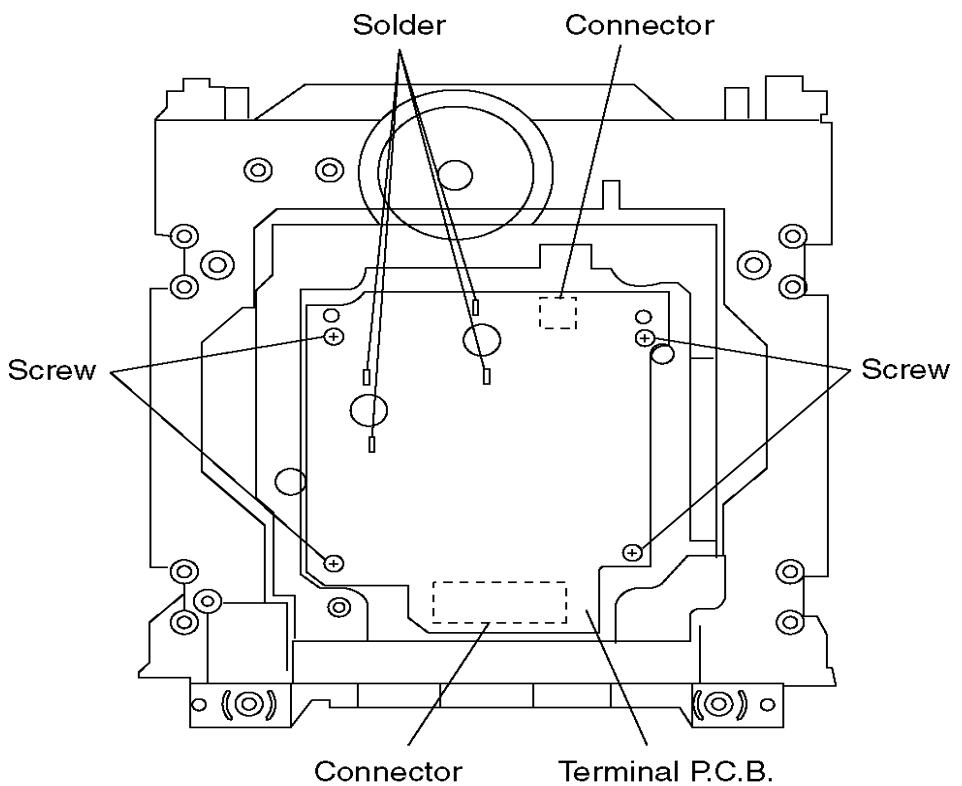
6.ASSEMBLING AND DISASSEMBLING THE MECHANISM UNIT

6.1 Disassembly Procedure



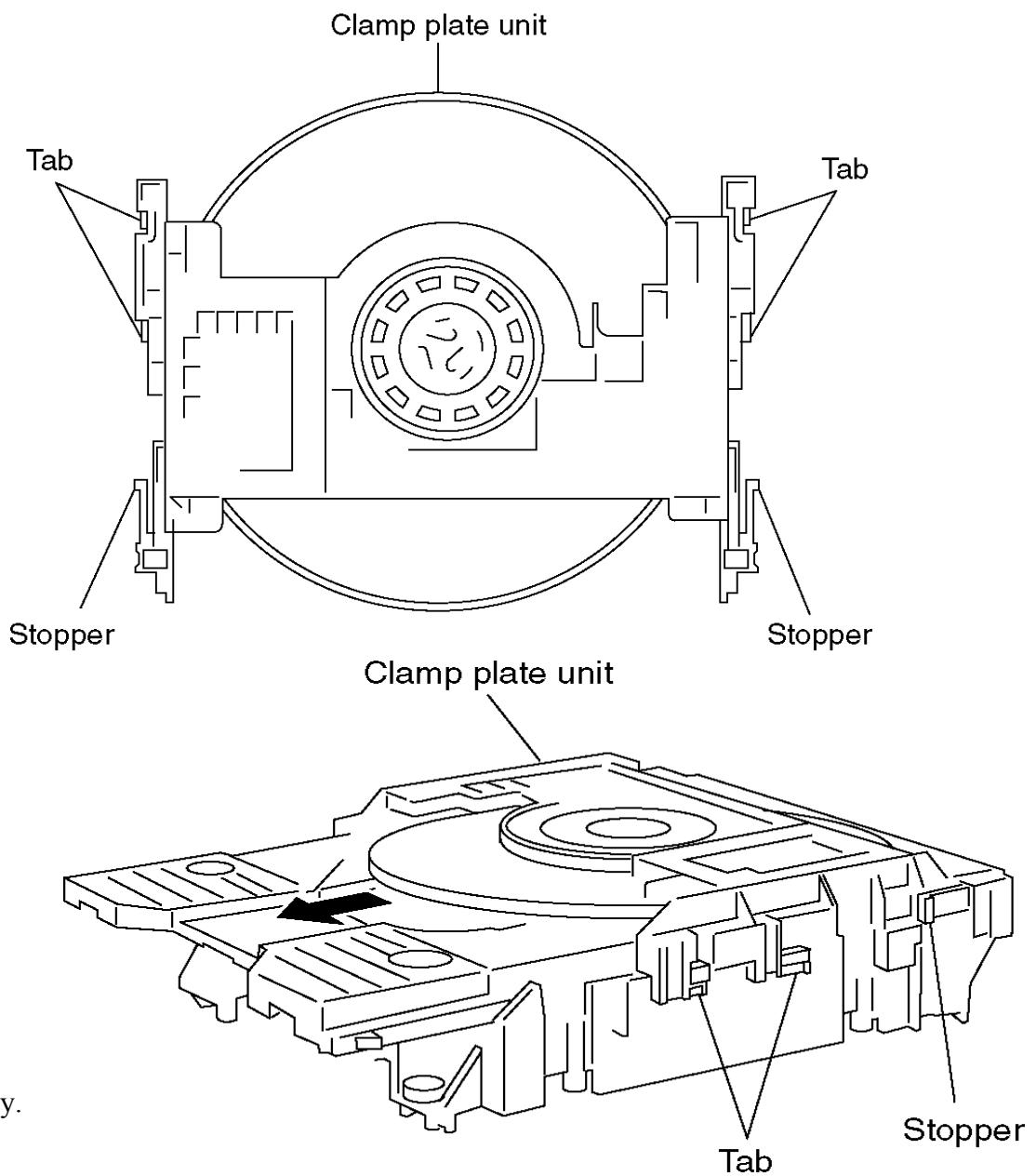
6.2 Terminal P.C.B.

- 1.Unscrew the screws.
- 2.Remove the solders.
- 3.Remove the connectors



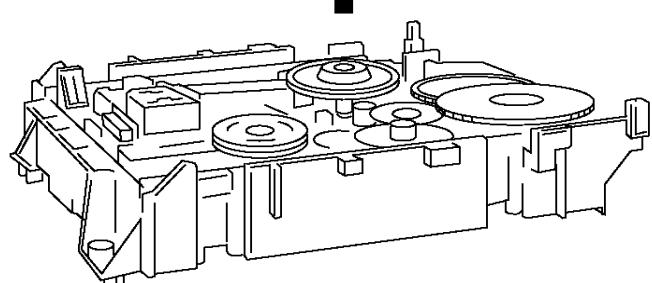
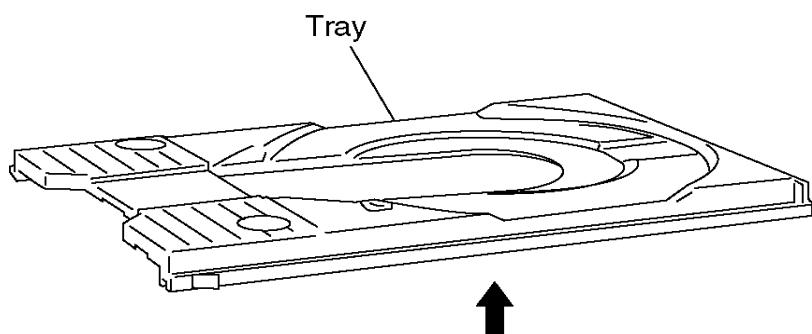
6.3 Clamp Plate Unit

1. Spread the stopper with hand to slide the tabs and remove the clamp plate unit.



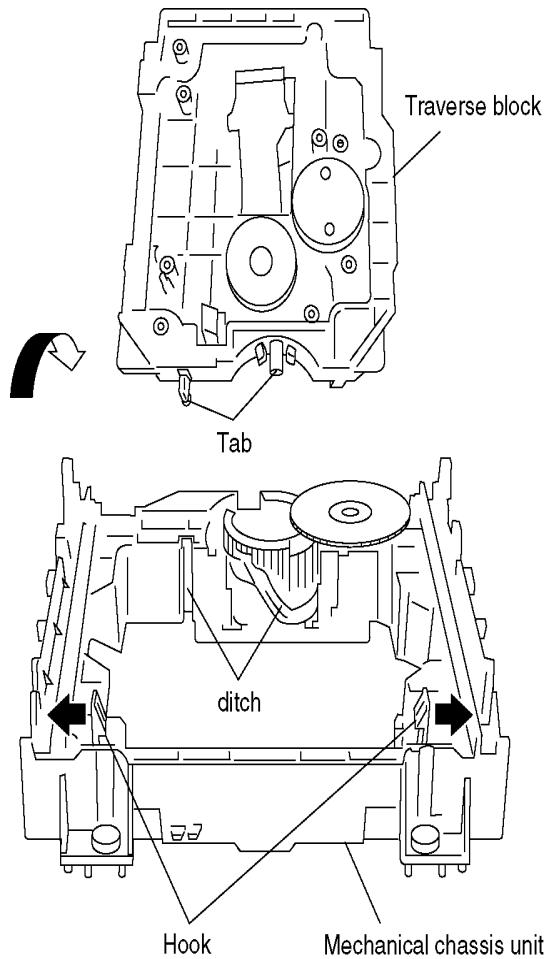
6.4 Tray

1. Lift the tray.



6.5 Traverse Block

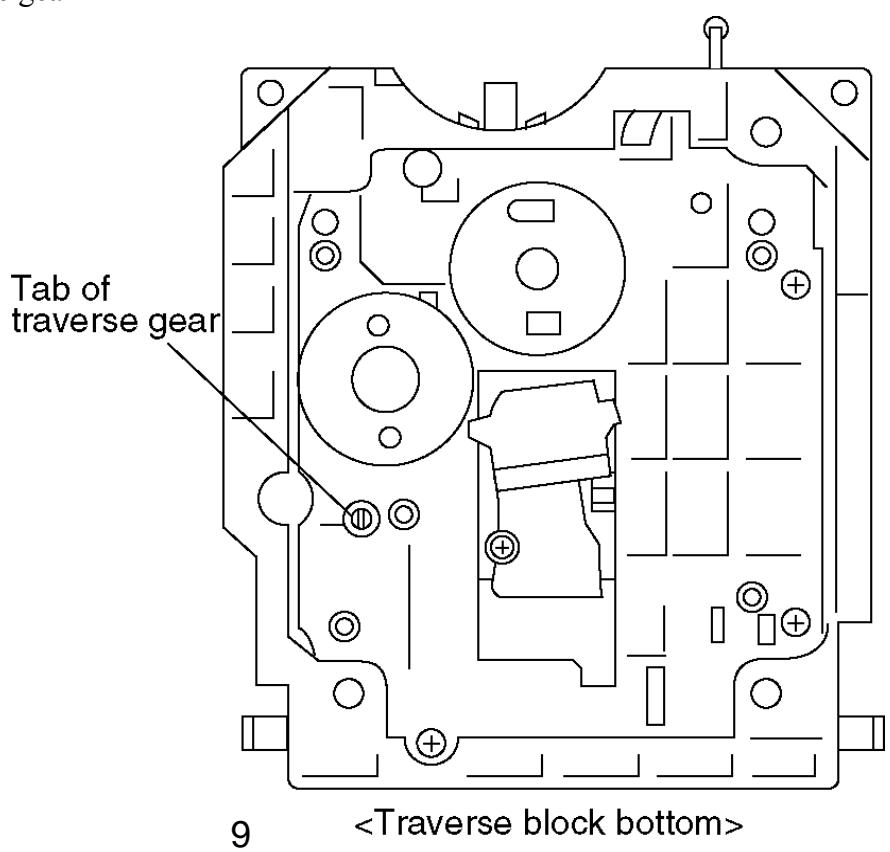
- 1.Lift the traverse block while spreading the hook of the mechanical chassis chassis unit.
- 2.Disengage the tabs from the holes of the mechanical chassis unit.

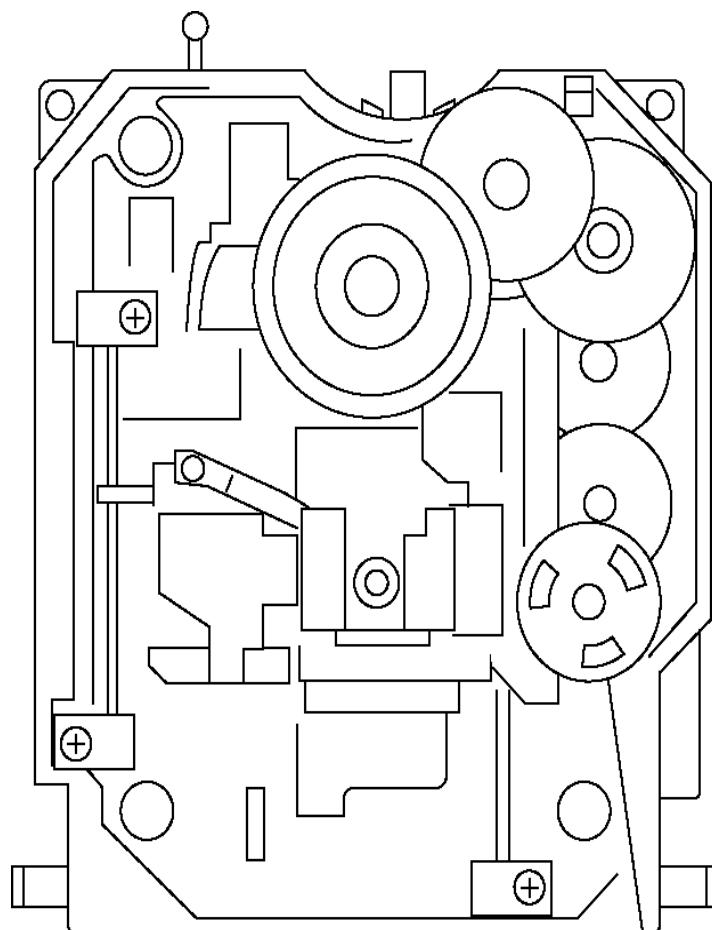


6.6. Traverse Gear

- 1.Disengage the tabs from the traverse gear

- 2.Remove the traverse gears B and C.

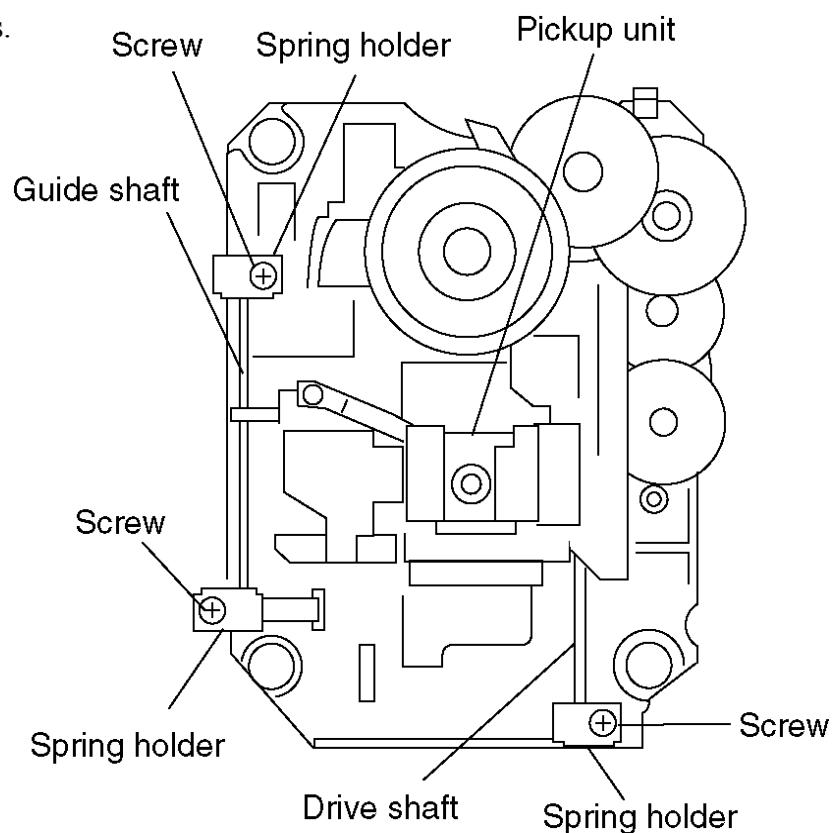




Traverse gears B and C

6.7 Optical Pickup Unit

1. Unscrew the screws.
2. Remove the spring holders and the springs.
3. Pull out of the drive shaft and guide shaft.



6.7.1. Precautions in optical pickup replacement

when working around the optical pickup.(Refer to the related page in this Manual about the countermeasures.

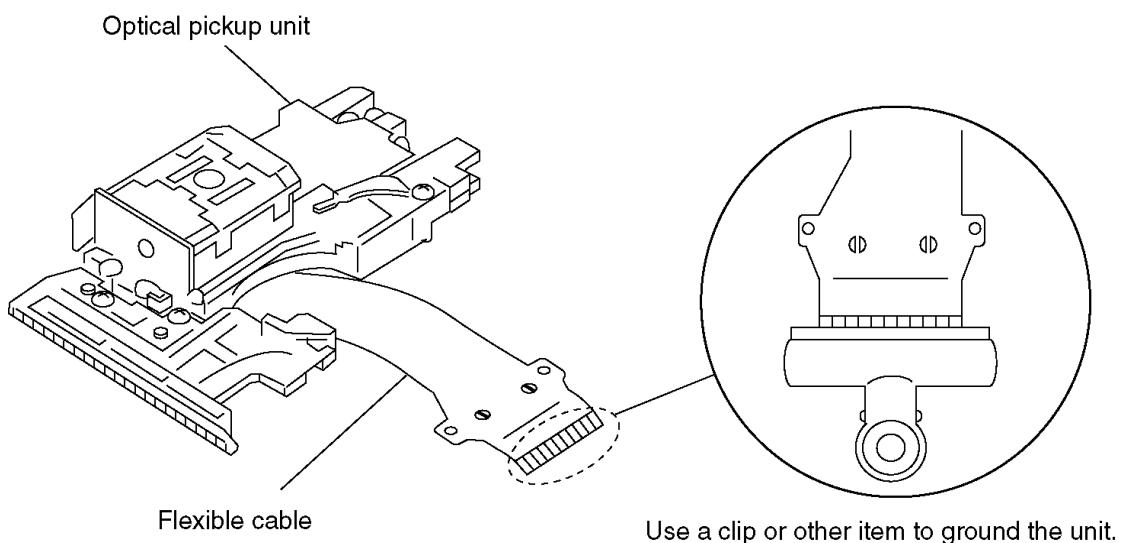
1.Do not touch laser diode,actuator and their peripheries.

2.Do not use tester to check laser diode.(Laser diode can be damaged easily.)

removing it.

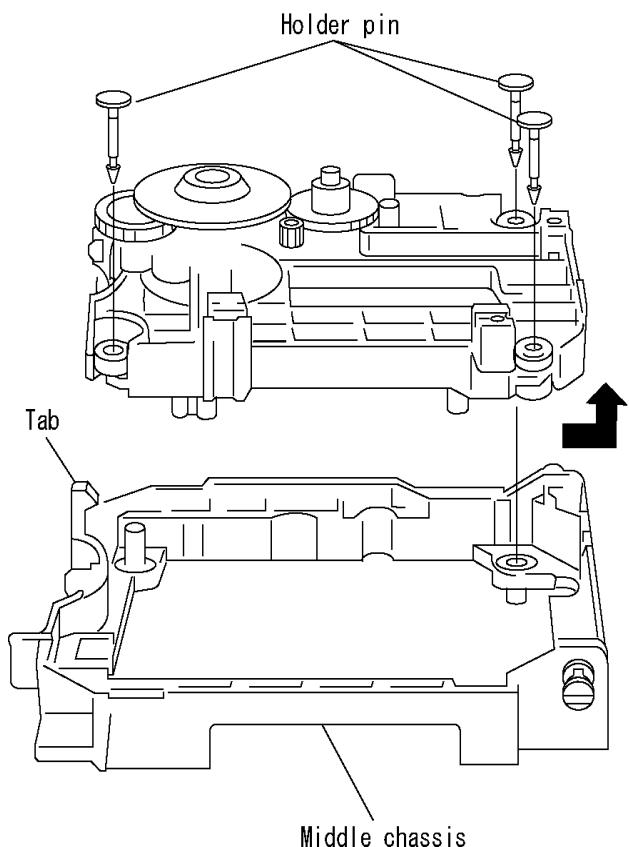
4.Solder the land on flexible cable of optical pickup unit.

-When using the soldering iron without anti-static feature,short-circuit the flexible cable terminal with a clip befo



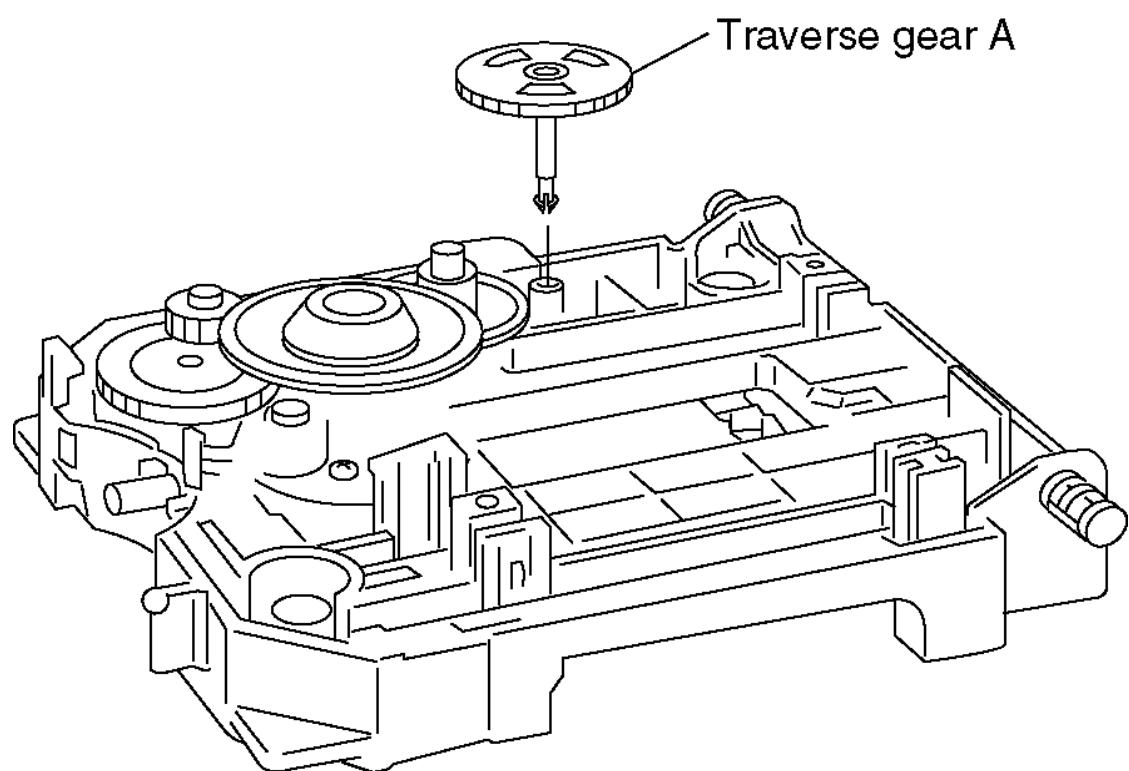
6.8. Disassembling the Middle Chassis

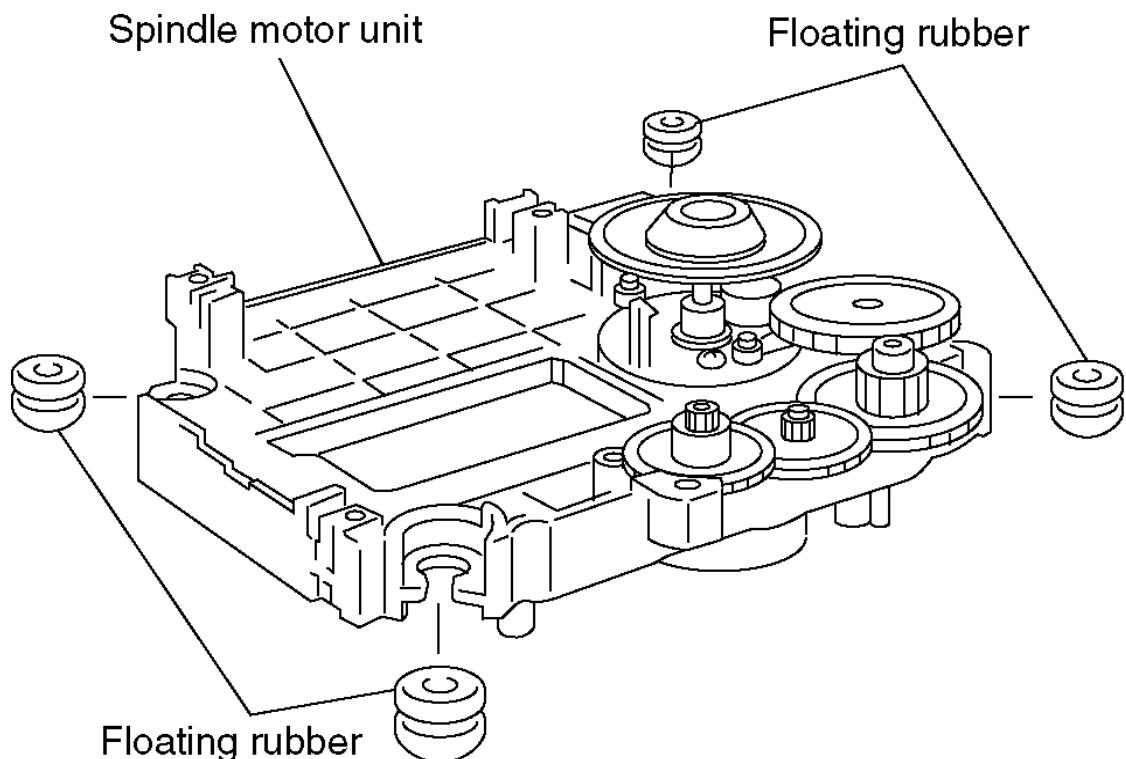
- 1.Remove the holders pins.
- 2.Remove the tab.
- 3.It lifts while pulling it in the direction of the arrow.



6.9. Disassembling the Traverse Gear A

- 1.Remove the traverse gear A.





7. Electrical Confirmation

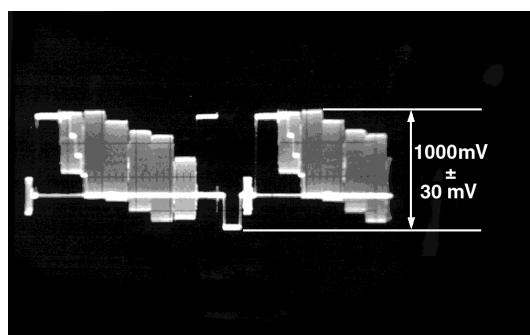
7.1. Video Output (Luminance Signal) Confirmation

DO this confirmation after replacing a P.C.B.

Measurement point	Mode	Disc
Video output terminal	Color bar 75% PLAY(Title 46):DVDT-S15 PLAY(Title 12):DVDT-S01	DVDT-S15 or DVDT-S01
Measuring equipment/tools	Confirmation value	
200mV/dir,10 μ sec/dir	1000mVp-p \pm 30mV	

Purpose: To maintain video signal output compatibility.

1. Connect the oscilloscope to the video output terminal and terminate at 75 ohms.
2. Confirm that luminance signal(Y+S)level is 1000mVp-p \pm 30mV



7.2. Video Output (Chrominance Signal) Confirmation

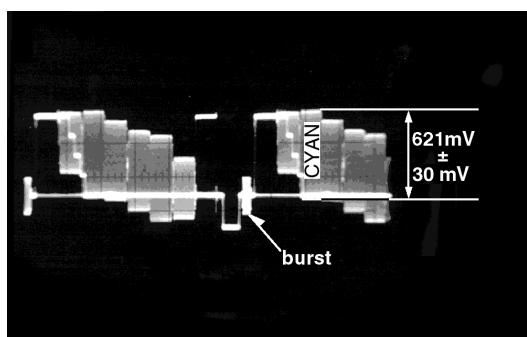
Do the confirmation after replacing P.C.B.

Measurement point	Mode	Disc
Video output terminal	Color bar 75% PLAY(Title 46):DVDT-S15 PLAY(Title 12):DVDT-S01	DVDT-S15 or DVDT-S01
Measuring equipment,tools	Confirmation value	
Screwdriver,Oscilloscope 200mV/dir,10 μ sec/dir	621mVp-p \pm 30mV	

Purpose: To maintain video signal output compatibility.

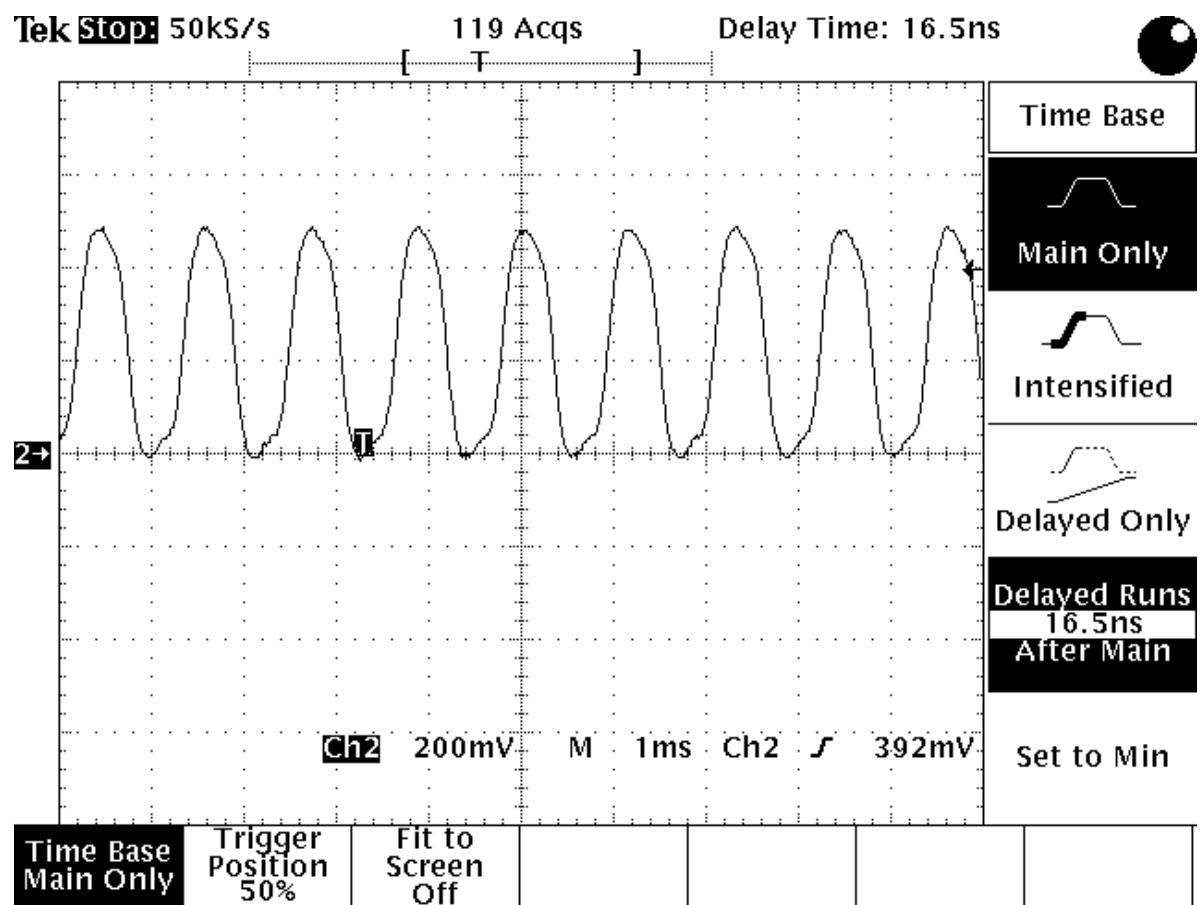
1. Connect the oscilloscope to the video output terminal and terminate at 75 ohme.

2. Confirm that the chrominance signal(C)level is 621 mVp-p \pm 30mV

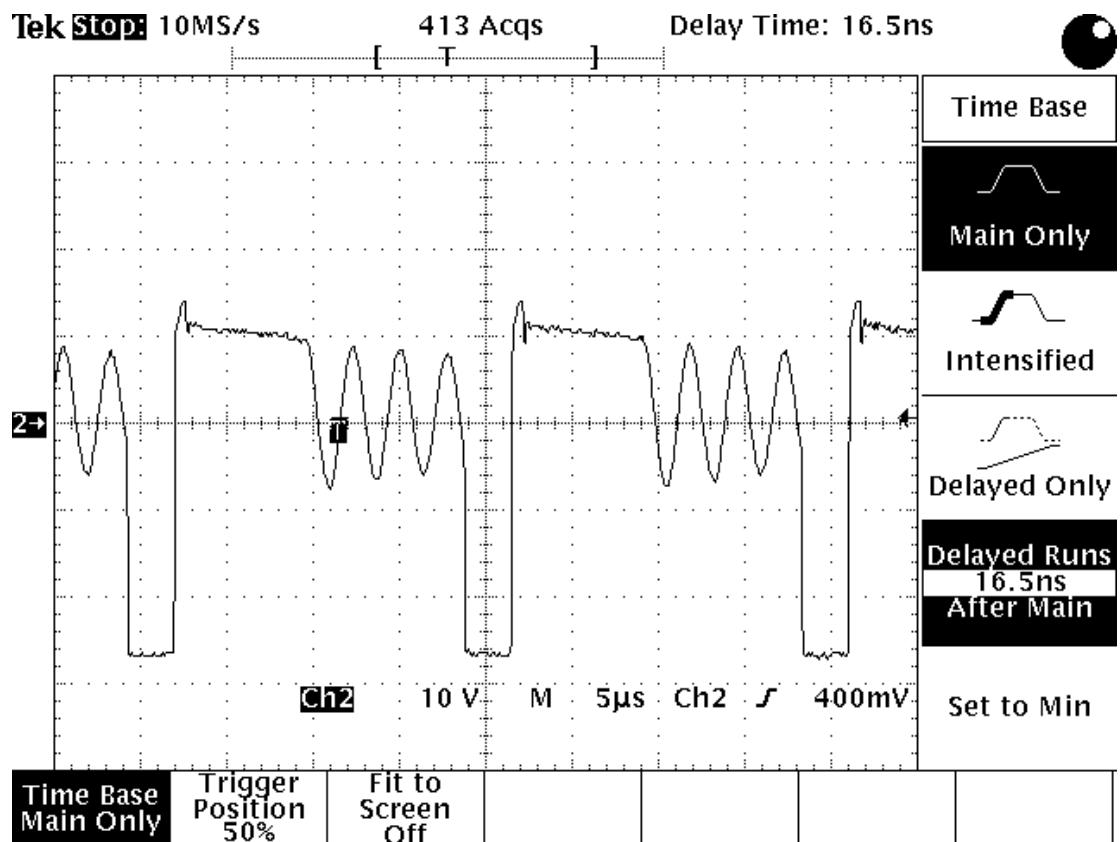


8.MPEG BOARD CHECK WAVEFORM

1. 27MHz WAVEFORM DIAGRAM



2. IC5L0380R PIN.2 WAVEFORM DIAGRAM



ES60X8 PINOUT DIAGRAM

The identical device pinouts for the ES6008, ES6018, ES6028 and ES6038 are shown in Figure 2.

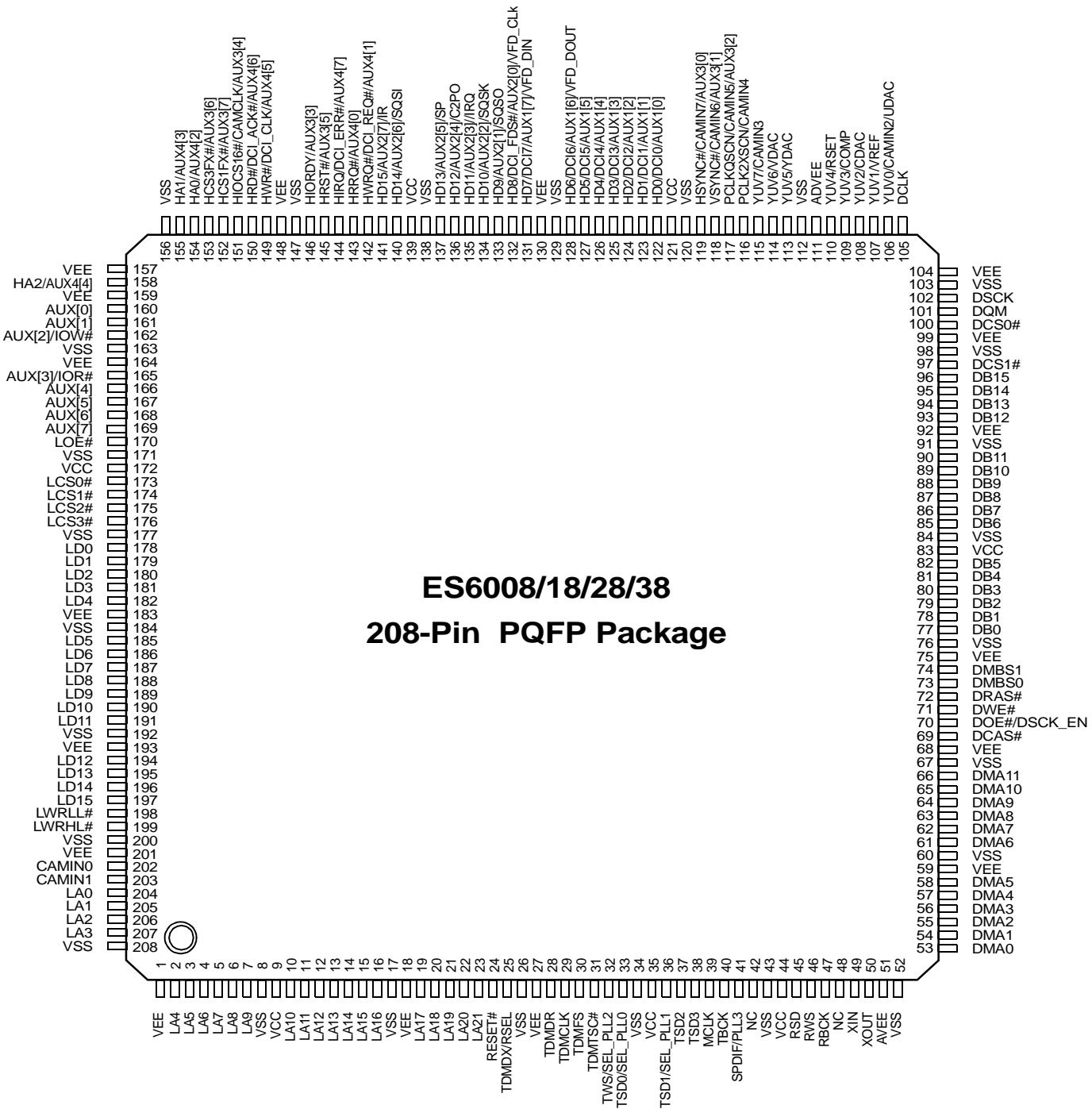


Figure 2 ES60x8 Pinout

ES60X8 PIN DESCRIPTION

Table 1 lists the identical pin descriptions for the ES6008, ES6018, ES6028 and ES6038.

Table 1 ES60x8 Pin Description

Name	Number	I/O	Definition																																				
VEE	1, 18, 27, 59, 68, 75, 92, 99, 104, 130, 148, 157, 159, 164, 183, 193, 201	I	I/O power supply.																																				
VSS	8, 17, 26, 34, 43, 52, 60, 67, 76, 84, 91, 98, 103, 112, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208	I	Ground.																																				
LA[21:0]	23:19, 16:10, 7:2, 207:204	O	Device address output.																																				
VCC	9, 35, 44, 83, 121, 139, 172	I	Core power supply.																																				
RESET#	24	I	Reset input, active low.																																				
TDMDX		O	TDM transmit data.																																				
RSEL	25	I	ROM Select. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>RSEL</th> <th>Selection</th> </tr> <tr> <td>0</td> <td>16-bit ROM</td> </tr> <tr> <td>1</td> <td>8-bit ROM</td> </tr> </table>	RSEL	Selection	0	16-bit ROM	1	8-bit ROM																														
RSEL	Selection																																						
0	16-bit ROM																																						
1	8-bit ROM																																						
TDMDR	28	I	TDM receive data.																																				
TDMCLK	29	I	TDM clock input.																																				
TDMFS	30	I	TDM frame sync.																																				
TDMTSC#	31	O	TDM output enable.																																				
TWS		O	Audio transmit frame sync.																																				
SEL_PLL2	32	I	System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>SEL_PLL2</th> <th>SEL_PLL1</th> <th>SEL_PLL0</th> <th>Clock Type</th> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>VCO off.</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>DCLK</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Bypass mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>DCLK x 2</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>DCLK x 4.5</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>DCLK x 3</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>DCLK x 3.5z</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>DCLK x 4</td> </tr> </table>	SEL_PLL2	SEL_PLL1	SEL_PLL0	Clock Type	0	0	0	VCO off.	0	0	1	DCLK	0	1	0	Bypass mode	0	1	1	DCLK x 2	1	0	0	DCLK x 4.5	1	0	1	DCLK x 3	1	1	0	DCLK x 3.5z	1	1	1	DCLK x 4
SEL_PLL2	SEL_PLL1	SEL_PLL0	Clock Type																																				
0	0	0	VCO off.																																				
0	0	1	DCLK																																				
0	1	0	Bypass mode																																				
0	1	1	DCLK x 2																																				
1	0	0	DCLK x 4.5																																				
1	0	1	DCLK x 3																																				
1	1	0	DCLK x 3.5z																																				
1	1	1	DCLK x 4																																				
TSD0		O	Audio transmit serial data port 0.																																				
SEL_PLL0	33	I	Refer to the description and matrix for SEL_PLL2 pin 32.																																				
TSD1		O	Audio transmit serial data port 1.																																				
SEL_PLL1	36	I	Refer to the description and matrix for SEL_PLL2 pin 32.																																				
TSD[2]	37	O	Audio transmit serial data output 2.																																				
TSD[3]	38	O	Audio transmit serial data output 3.																																				

Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition																								
MCLK	39	I/O	Audio master clock for audio DAC.																								
TBCK	40	O	Audio transmit bit clock.																								
SPDIF	41	O	S/PDIF output.																								
SEL_PLL3		I	Clock source select. <table border="1" style="margin-left: 20px;"> <tr> <th>SEL_PLL3</th> <th>Clock Source</th> </tr> <tr> <td>0</td> <td>Crystal oscillator</td> </tr> <tr> <td>1</td> <td>DCLK input</td> </tr> </table>	SEL_PLL3	Clock Source	0	Crystal oscillator	1	DCLK input																		
SEL_PLL3	Clock Source																										
0	Crystal oscillator																										
1	DCLK input																										
NC	42, 48		No connect pins. Leave open.																								
RSD	45	I	Audio receive serial data.																								
RWS	46	I	Audio receive frame sync.																								
RBCK	47	I	Audio receive bit clock.																								
XIN	49	I	Crystal input.																								
XOUT	50	O	Crystal output.																								
AVEE	51	I	Analog power for PLL.																								
DMA[11:0]	66:61, 58:53	O	DRAM address bus [11:0].																								
DCAS#	69	O	DRAM column address strobe.																								
DOE#	70	O	DRAM output enable.																								
DSCK_EN		O	DRAM clock enable.																								
DWE#	71	O	DRAM write enable.																								
DRAS#	72	O	DRAM row address strobe.																								
DMBS0	73	O	SDRAM bank select 0.																								
DMBS1	74	O	SDRAM bank select 1.																								
DB[15:0]	96:93, 90:85, 82:77	I/O	DRAM data bus [15:0].																								
DCS[1:0]#	97,100	O	SDRAM chip select [1:0].																								
DQM	101	O	Data input/output mask.																								
DSCK	102	O	Output clock to SDRAM.																								
DCLK	105	I	27 MHz clock input to PLL.																								
YUV0	106	O	YUV0 pixel output data.																								
CAMIN2		I	Camera input 2.																								
UDAC		O	Video DAC output. <table border="1" style="margin-left: 20px;"> <tr> <th>Mode</th> <th>YDAC</th> <th>UDAC</th> <th>VDAC</th> <th>CDAC</th> </tr> <tr> <td>A</td> <td>Y</td> <td>C</td> <td>Composite</td> <td>C</td> </tr> <tr> <td>B</td> <td>Y</td> <td>Composite</td> <td>Composite</td> <td>C</td> </tr> <tr> <td>C</td> <td>Y</td> <td>U</td> <td>Composite</td> <td>V</td> </tr> <tr> <td>D</td> <td>Y</td> <td>U</td> <td>C</td> <td>V</td> </tr> </table> <p>Y: Luma component for YUV and Y/C processing. C: Chrominance signal for Y/C processing. U: Chrominance component signal for YUV mode. V: Chrominance component signal for YUV mode.</p>	Mode	YDAC	UDAC	VDAC	CDAC	A	Y	C	Composite	C	B	Y	Composite	Composite	C	C	Y	U	Composite	V	D	Y	U	C
Mode	YDAC	UDAC	VDAC	CDAC																							
A	Y	C	Composite	C																							
B	Y	Composite	Composite	C																							
C	Y	U	Composite	V																							
D	Y	U	C	V																							

Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition
YUV1	107	O	YUV1 pixel output data.
VREF		I	Internal voltage reference to video DAC. Bypass to ground with 0.1 μ F capacitor.
YUV2	108	O	YUV2 pixel output data.
CDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV3	109	O	YUV3 pixel output data.
COMP		I	Compensation input. Bypass to ADVEE with 0.1 μ F capacitor.
YUV4	110	O	YUV4 pixel output data.
RSET		I	DAC current adjustment resistor input.
ADVEE	111	I	Analog power for video DAC.
YUV5	113	O	YUV5 pixel output data.
YDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV6	114	O	YUV6 pixel output data.
VDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV7	115	O	YUV7 pixel output data.
CAMIN3		I	Camera YUV 3.
PCLK2XSCN	116	I/O	27-MHz video output pixel clock.
CAMIN4		I	Camera YUV 4.
PCLKQSCN	117	O	13.5-MHz video output pixel clock.
CAMIN5		I	Camera YUV 5.
VSYNC#	118	I/O	Vertical sync, active low.
CAMIN6		I	Camera YUV 6.
HSYNC#	119	I/O	Horizontal sync, active low.
CAMIN7		I	Camera YUV 7.
HD[5:0]	127:122	I/O	Host data I/O [5:0].
DCI[5:0]		I/O	DVD channel data I/O [5:0].
AUX1[5:0]		I/O	Aux1 data I/O [5:0].
HD[6]	128	I/O	Host data I/O [6].
DCI[6]		I/O	DVD channel data I/O [6].
AUX1[6]		I/O	Aux1 data I/O [6].
VFD_DOUT		I	VFD data output.
HD[7]	131	I/O	Host data I/O [7].
DCI[7]		I/O	DVD channel data I/O [7].
AUX1[7]		I/O	Aux1 data I/O [7:0].
VFD_DIN		I	VFD data input.
HD[8]	132	I/O	Host data bus 8.
DCI_FDS#		I/O	DVD input sector start.
AUX2[0]		I/O	Aux2 data I/O 0.
VFD_CLK		I	VFD clock input.
HD[9]	133	I/O	Host data bus line 9.
AUX2[1]		I/O	Aux2 data I/O [1] when selected.
SQSQ		I	Subcode-Q data.
HD[10]	134	I/O	Host data bus line10.
AUX2[2]		I/O	Aux2 data I/O [2] when selected.
SQSK		I	Subcode-Q clock.

Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition
HD[11]	135	I/O	Host data bus line11.
AUX2[3]		I/O	Aux2 data I/O [3] when selected.
IRQ		O	IRQ output.
HD[12]	136	I/O	Host data bus line12.
AUX2[4]		I/O	Aux2 data I/O [4] when selected.
C2PO		I	C2PO error correction flag from CD-ROM.
HD[13]	137	I/O	Host data bus line13.
AUX2[5]		I/O	Aux2 data I/O [5] when selected.
SP		I	16550 UART serial port input.
HD[14]	140	I/O	Host data bus line14.
AUX2[6]		I/O	Aux2 data I/O [6] when selected.
SQSI		I	Subcode-Q sync.
HD[15]	141	I/O	Host data bus line15.
AUX2[7]		I/O	Aux2 data I/O [7] when selected.
IR		I	IR remote control input.
HWRQ#	142	O	Host write request.
DCI_REQ#		O	DVD control interface request.
AUX4[1]		I/O	Aux4 data I/O 1.
HRRQ#	143	O	Host read request.
AUX4[0]		I/O	Aux4 data I/O 0.
HIRQ	144	I/O	Host interrupt.
DCI_ERR#		I/O	DVD channel data error.
AUX4[7]		I/O	Aux4 data I/O 7.
HRST#	145	O	Host reset.
AUX3[5]		I/O	Aux3 data I/O 5.
HIORDY	146	I	Host I/O ready.
AUX3[3]		I/O	Aux3 data I/O 3.
HWR#	149	I/O	Host write.
DCI_CLK		I/O	DVD channel data clock.
AUX4[5]		I/O	Aux4 data I/O 5.
HRD#	150	O	Host read.
DCI_ACK#		O	DVD channel data valid.
AUX4[6]		I/O	Aux4 data I/O 6.
HIOCS16#	151	I	Device 16-bit data transfer.
CAMCLK		I	Camera port pixel clock input.
AUX3[4]		I/O	Aux3 data I/O 4.
HCS1FX#	152	O	Host select 1.
AUX3[7]		I/O	Aux3 data I/O 7.
HCS3FX#	153	O	Host select 3.
AUX3[6]		I/O	Aux3 data I/O 6.
HA[2:0]	158, 155:154	I/O	Host address bus.
AUX4[4:2]		I/O	Aux4 data I/Os [4:2].
AUX[1:0]	160	I/O	Auxiliary ports 1:0.

Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition
AUX[2]	162	I/O	Auxiliary port 2.
IOW#		O	I/O Write strobe.
AUX[3]	165	I/O	Auxiliary port 3.
IOR#		O	I/O Read strobe.
AUX[7:3]	169:166	I/O	Auxiliary ports 7:3.
LOE#	170	O	Device output enable.
LCS[3:0]#	176:173	O	Chip select [3:0].
LD[15:0]	197:194, 191:185, 182:178	I/O	EPROM device data bus.
LWRLL#	198	O	Device low-byte write enable.
LWRHL#	199	O	Device high-byte write enable.
CAMINO	202	I	Camera YUV 0.
CAMIN1	203	I	Camera YUV 1.

LICENSING REQUIREMENTS

Dolby Digital Licensing

Dolby Digital audio enabling software is provided with the Vibratto series of DVD processors. Dolby is a trademark of the Dolby Laboratories. Supply of this implementation of Dolby Technology does not convey a license or imply a right under any patent, or any other Industrial or Intellectual Property Right of Dolby Laboratories, to use this implementation in any end-user or ready-to-use final product. Companies planning to use this implementation in products must obtain a license from Dolby Laboratories Licensing Corporation before designing such products. Additional per-chip royalties may be required and are to be paid by the purchaser to Dolby Laboratories, Inc. Details of the OEM Dolby Digital license may be obtained by writing to:

Dolby Laboratories Inc.
 Dolby Laboratories Licensing Corporation
 Attn.: Intellectual Property Manager
 100 Potrero Avenue
 San Francisco, CA 94103-4813

Macrovision Licensing

Macrovision Copy Protection is supported in the Vibratto series of DVD processors. The use of Macrovision's Copy Protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision.

Reverse engineering or disassembly is prohibited. A valid Macrovision license must be in effect between the Vibratto purchaser and Macrovision Corporation. Additional per-chip royalties may be required and are to be paid by the purchaser to Macrovision Corporation. Details of the Macrovision license may be obtained by writing to:

Macrovision Corporation
 1341 Orleans Avenue
 Sunnyvale, CA 94089

FUNCTIONAL DESCRIPTION

Figure 3 shows the internal block diagram for the basic Vibratto DVD processor.

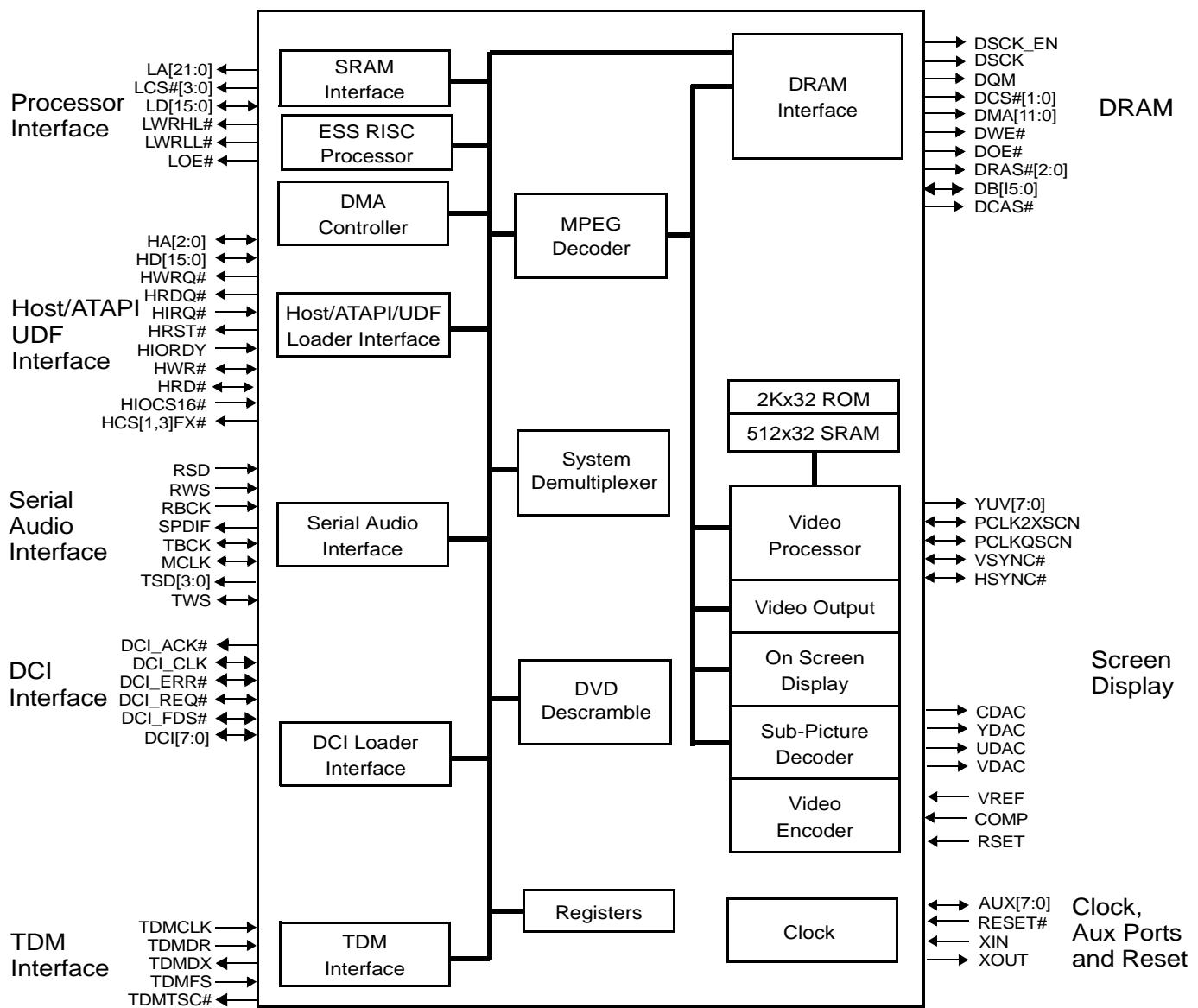


Figure 3 Vibratto Block Diagram

Vibratto Device Architecture

The Vibratto device architecture includes a RISC processor, CRT controller, transport mechanism, video encoder, memory controller, on-screen display (OSD) controller and video processor.

ESS RISC Processor

Embedded in the Vibratto is a 32-bit data pipelined RISC processor, with a combined 16 kb instruction and data cache subsystem. Programming of the RISC processor is

done mostly in C. For applications involving an external host processor the communication between a host processor and the Vibratto is handled by a host interface module. The host interface can also be used for high speed data input and output.

The ESS RISC processor instruction and data cache subsystem is organized as a two-way set associative. On a cache load-miss and write-miss, the cache lines are allocated into the cache memory.

IC BLOCK DIAGRAM & DESCRIPTION

IC U214 Am29F002B/Am29F002NB

2 Megabit (256 K x 8-Bit) CMOS 5.0 Volt-only Boot Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
 - 5.0 Volt-only operation for read, erase, and program operations
 - Minimizes system level requirements
- **Manufactured on 0.32 µm process technology**
 - Compatible with 0.5 µm Am29F002 device
- **High performance**
 - Access times as fast as 55 ns
- **Low power consumption (typical values at 5 MHz)**
 - 1 µA standby mode current
 - 20 mA read current
 - 30 mA program/erase current
- **Flexible sector architecture**
 - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and three 64 Kbyte sectors
 - Supports full chip erase
 - Sector Protection features:
 - A hardware method of locking a sector to prevent any program or erase operations within that sector
 - Sectors can be locked via programming equipment
 - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
 - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
 - Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write cycle guarantee per sector**
- **20-year data retention at 125°C**
 - Reliable operation for the life of the system
- **Package option**
 - 32-pin PDIP
 - 32-pin TSOP
 - 32-pin PLCC
- **Compatibility with JEDEC standards**
 - Pinout and software compatible with single-power supply Flash
 - Superior inadvertent write protection
- **Data# Polling and toggle bits**
 - Provides a software method of detecting program or erase operation completion
- **Erase Suspend/Erase Resume**
 - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
 - Hardware method to reset the device to reading array data (not available on Am29F002NB)

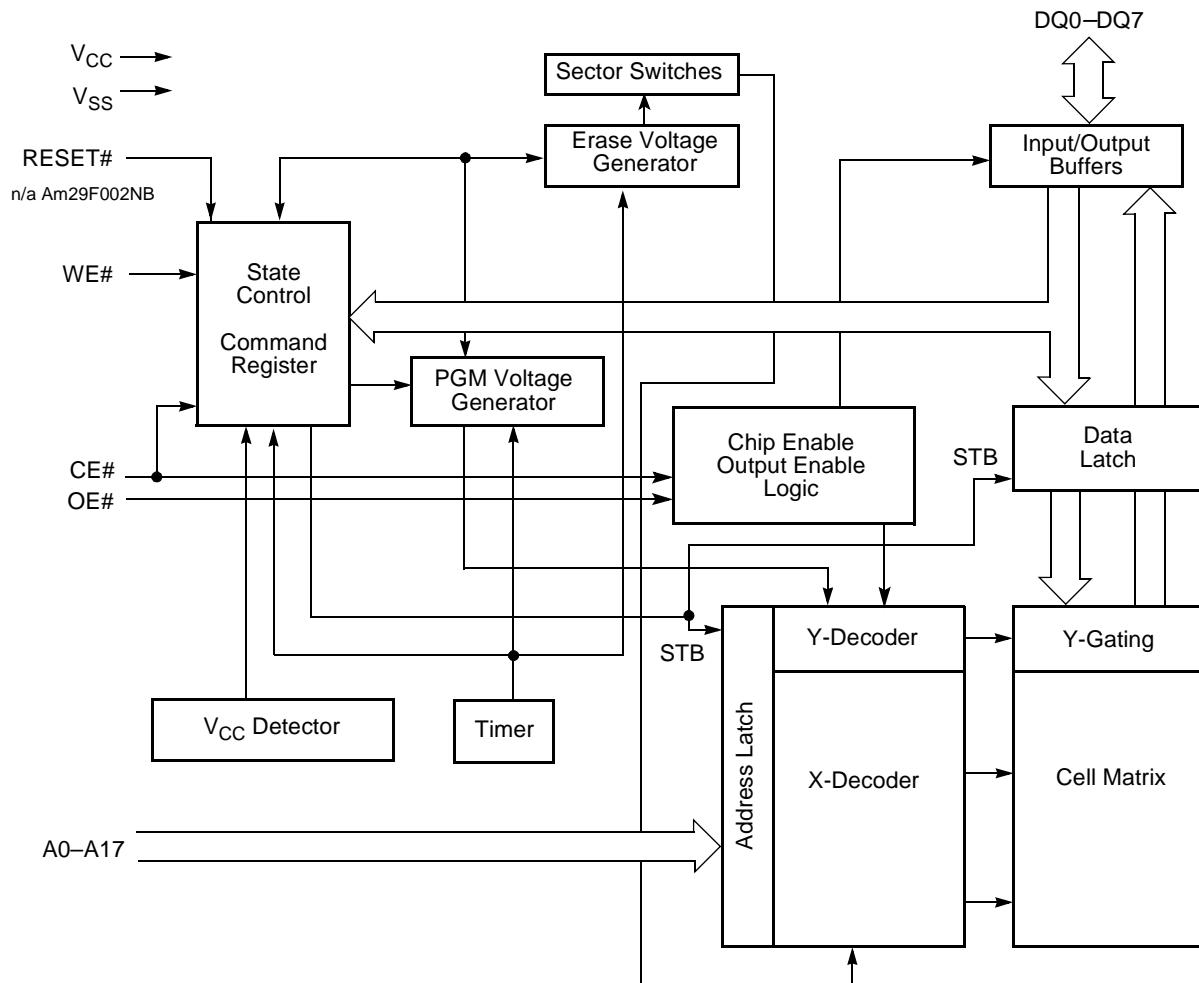
IC BLOCK DIAGRAM & DESCRIPTION

PRODUCT SELECTOR GUIDE

Family Part Number		Am29F002B/Am29F002NB			
Speed Option	V _{CC} = 5.0 V ± 5%	-55			
	V _{CC} = 5.0 V ± 10%		-70	-90	-120
Max access time, ns (t _{ACC})		55	70	90	120
Max CE# access time, ns (t _{CE})		55	70	90	120
Max OE# access time, ns (t _{OE})		30	30	35	50

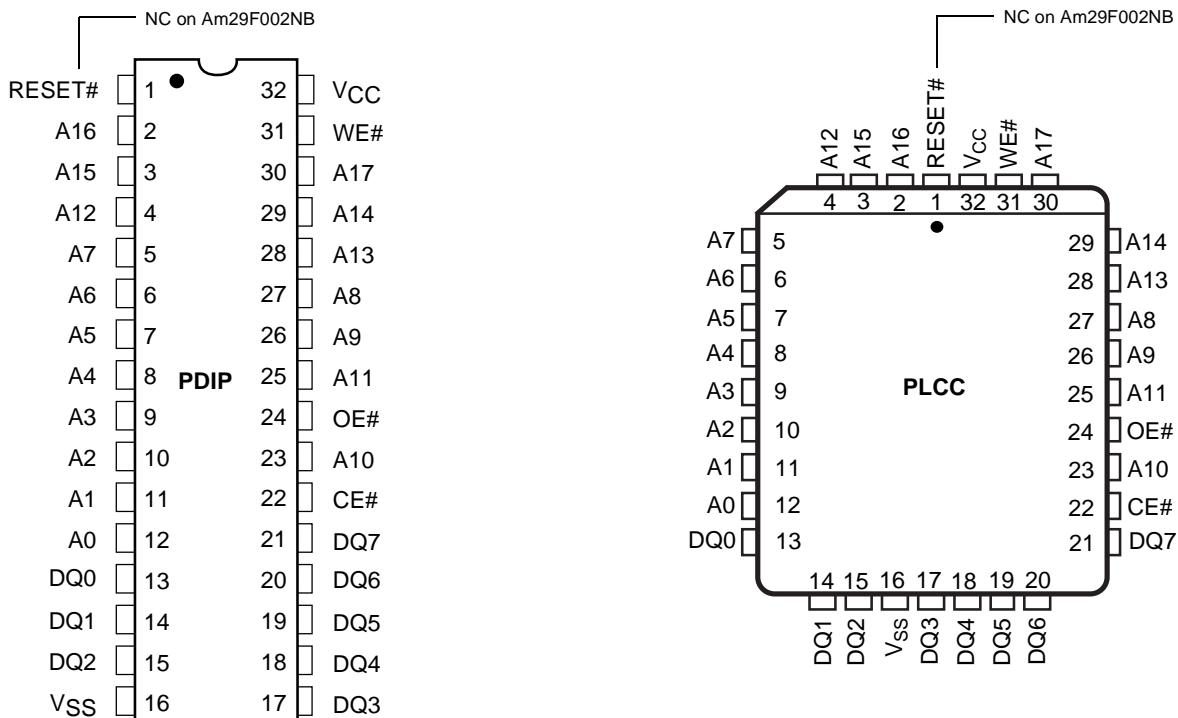
Note: See "AC Characteristics" for full specifications.

BLOCK DIAGRAM



IC BLOCK DIAGRAM & DESCRIPTION

CONNECTION DIAGRAMS

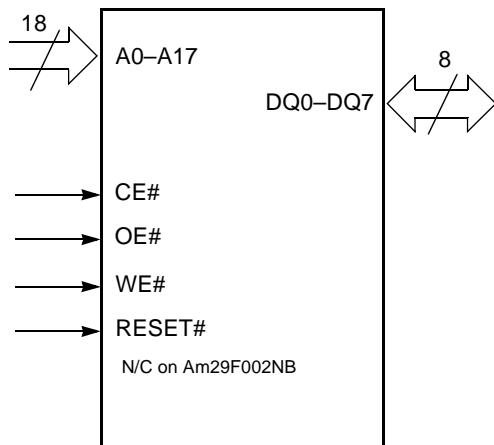


IC BLOCK DIAGRAM & DESCRIPTION

PIN CONFIGURATION

A0–A17 = 18 addresses
DQ0–DQ7 = 8 data inputs/outputs
CE# = Chip enable
OE# = Output enable
WE# = Write enable
RESET# = Hardware reset pin, active low
(not available on Am29F002NB)
V_{CC} = +5.0 V single power supply
(see Product Selector Guide for
device speed ratings and voltage
supply tolerances)
V_{SS} = Device ground
NC = Pin not connected internally

LOGIC SYMBOL



IC BLOCK DIAGRAM & DESCRIPTION

IC U206 SDRAM-HY57V65162B

4 Banks x 1M x 16Bit Synchronous DRAM

DESCRIPTION

The Hyundai HY57V651620B is a 67,108,864-bit CMOS Synchronous DRAM, ideally suited for the Mobile applications which require low power consumption and extended temperature range. HY57V651620B is organized as 4banks of 1,048,576x16.

HY57V651620B is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or Full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

FEATURES

- Single 3.3V ± 10% power supply
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 54pin TSOP-II with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM or LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
 - 1, 2, 4, 8 or Full page for Sequential Burst
 - 1, 2, 4 or 8 for Interleave Burst
- Programmable CAS Latency ; 2, 3 Clocks

ORDERING INFORMATION

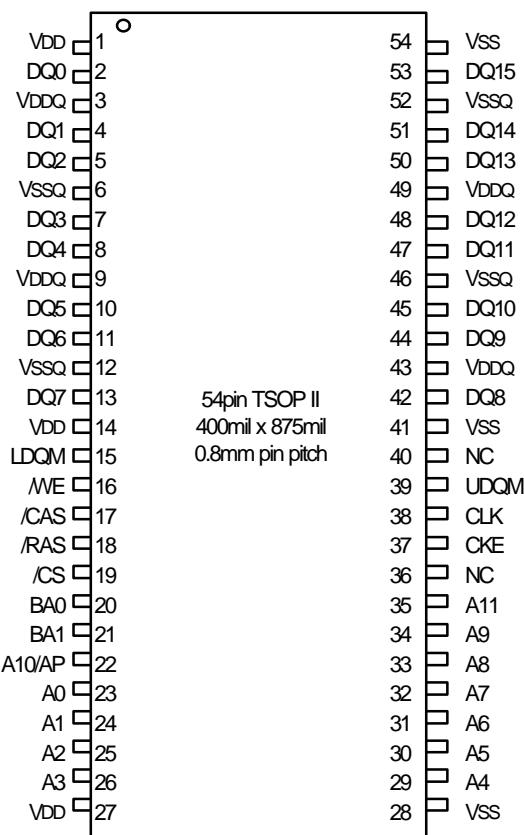
Part No.	Clock Frequency	Power	Organization	Interface	Package			
HY57V651620BTC-7I	143MHz	Normal power	4Banks x 1Mbits x16	LVTTL	400mil 54pin TSOP II			
HY57V651620BTC-75I	133MHz							
HY57V651620BTC-10SI	100MHz							
HY57V651620BLTC-7I	143MHz	Lower Power						
HY57V651620BLTC-75I	133MHz							
HY57V651620BLTC-10SI	100Mhz							

This document is a general product description and is subject to change without notice. Hyundai Electronics does not assume any responsibility for use of circuits described. No patent licenses are implied.

Rev. 0.4/Nov.00

IC BLOCK DIAGRAM & DESCRIPTION

PIN CONFIGURATION



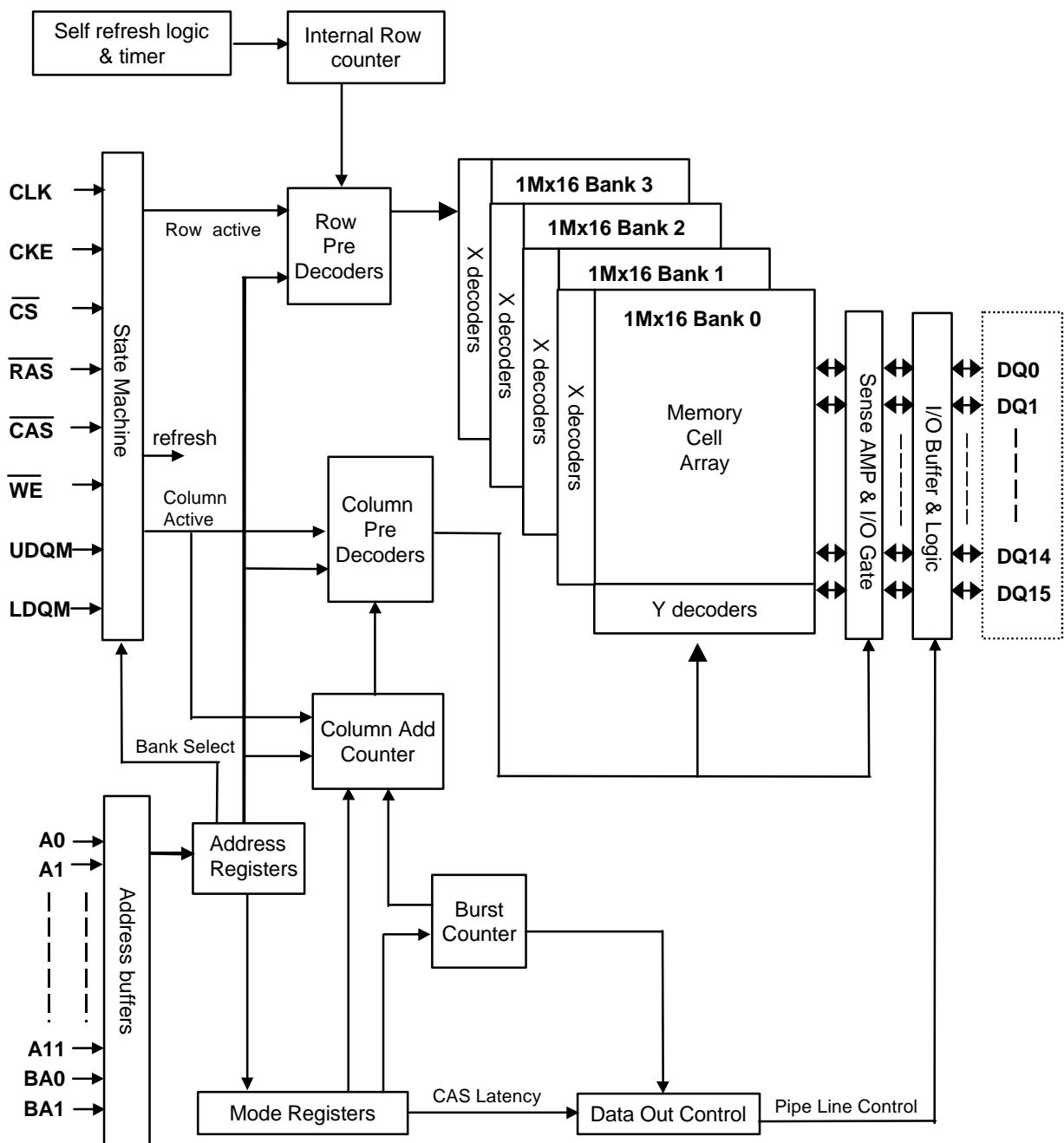
PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
CS	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0,BA1	Bank Address	Selects bank to be activated during RAS activity Selects bank to be read/written during CAS activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
RAS, CAS, WE	Row Address Strobe, Column Address Strobe, Write Enable	RAS, CAS and WE define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

IC BLOCK DIAGRAM & DESCRIPTION

FUNCTIONAL BLOCK DIAGRAM

1Mbit x 4banks x 16 I/O Synchronous DRAM



IC BLOCK DIAGRAM & DESCRIPTION

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	-40 ~ 85	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITION (TA= -40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High Voltage	VIH	2.0	3.0	VDDQ + 2.0	V	1,2
Input Low Voltage	VIL	VSSQ - 2.0	0	0.8	V	1,3

Note :

1. All voltages are referenced to VSS = 0V
2. VIH (max) is acceptable 4.7V AC pulse width with ≤3ns of duration
3. VIL (min) is acceptable -2.0V AC pulse width with ≤3ns of duration

AC OPERATING CONDITION (TA= -40 to 85°C, VDD=3.3V ± 0.3V, VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

Note :

1. Output load to measure access time is equivalent to two TTL gates and one capacitor (50pF)
For details, refer to AC/DC output circuit

IC BLOCK DIAGRAM & DESCRIPTION

IC WS7805

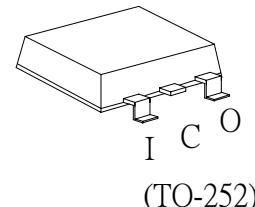
POSITIVE-VOLTAGE REGULATORS

- 3-Terminal Regulators
- Output Current Up to 1.5 A
- No External Components
- Internal Thermal Overload Protection
- High Power Dissipation Capability
- Internal Shot-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

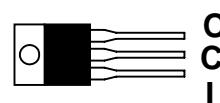
DESCRIPTION

This series of fixed-voltage monolithic integrated-circuit voltage regulators designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 amperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload.

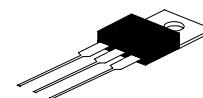
TO-252
WS7805DP



(TO-252)



TO-220
WS7805CV



ABSOLUTE MAXIMUM RATINGS OVER OPERATING TEMPERATURE RANGE (UNLESS OTHERWISE NOTE)

WS7805	PARAMETER	UNIT
Input voltage, V_I	35	V
Continuous total dissipation at 25°C free-air temperature	2	W
Lead temperature 1.6mm (1/16 inch) from case 10 seconds	260	°C
Storage temperature range, T_{stg}	-65 to 150	°C

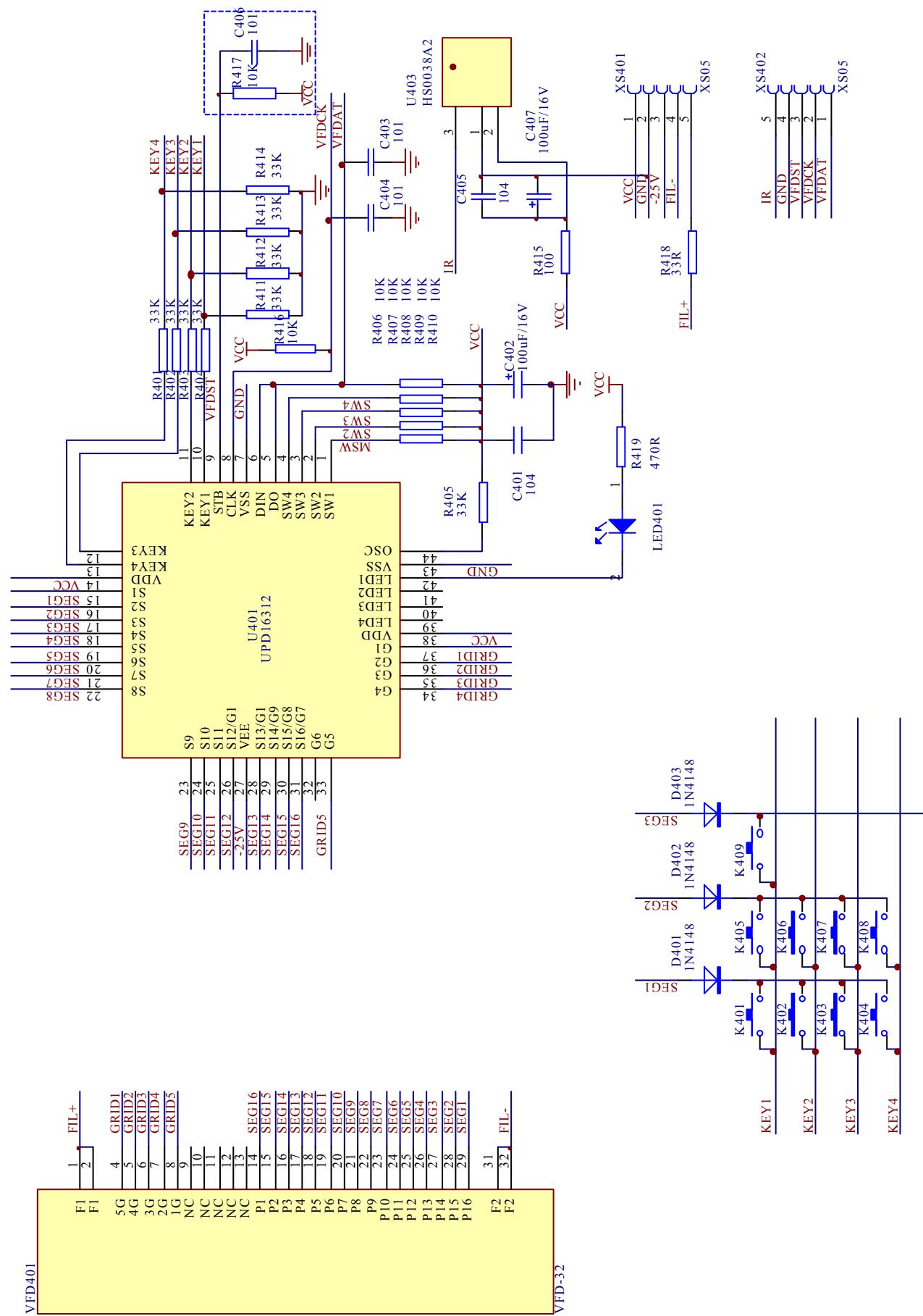
RECOMMENDED OPERATING CONDITIONS

MIN MAX UNIT

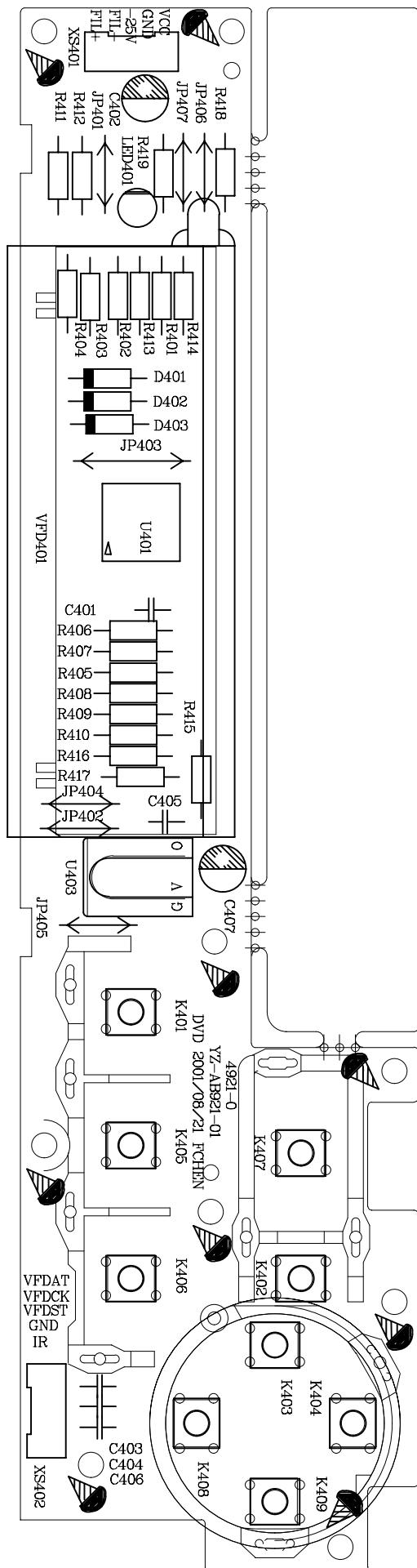
Input voltage, V_I	7	25	V
Output current, I_O		1.5	A
Operating virtual junction temperature, T_J	0	70	°C

10. SCHEMATIC & P.C.B WIRING DIAGRAM

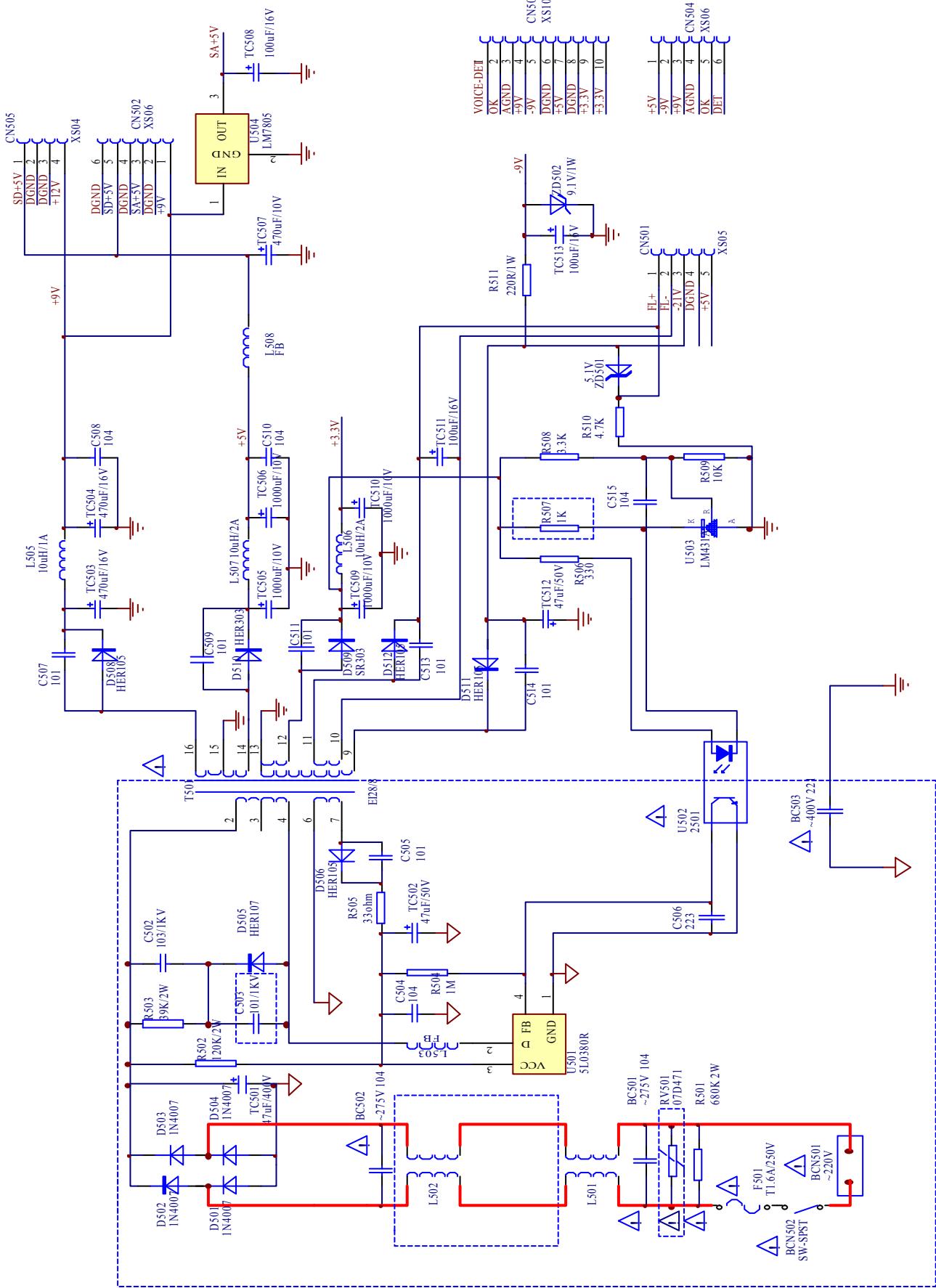
FRONT SCHEMATIC DIAGRAM



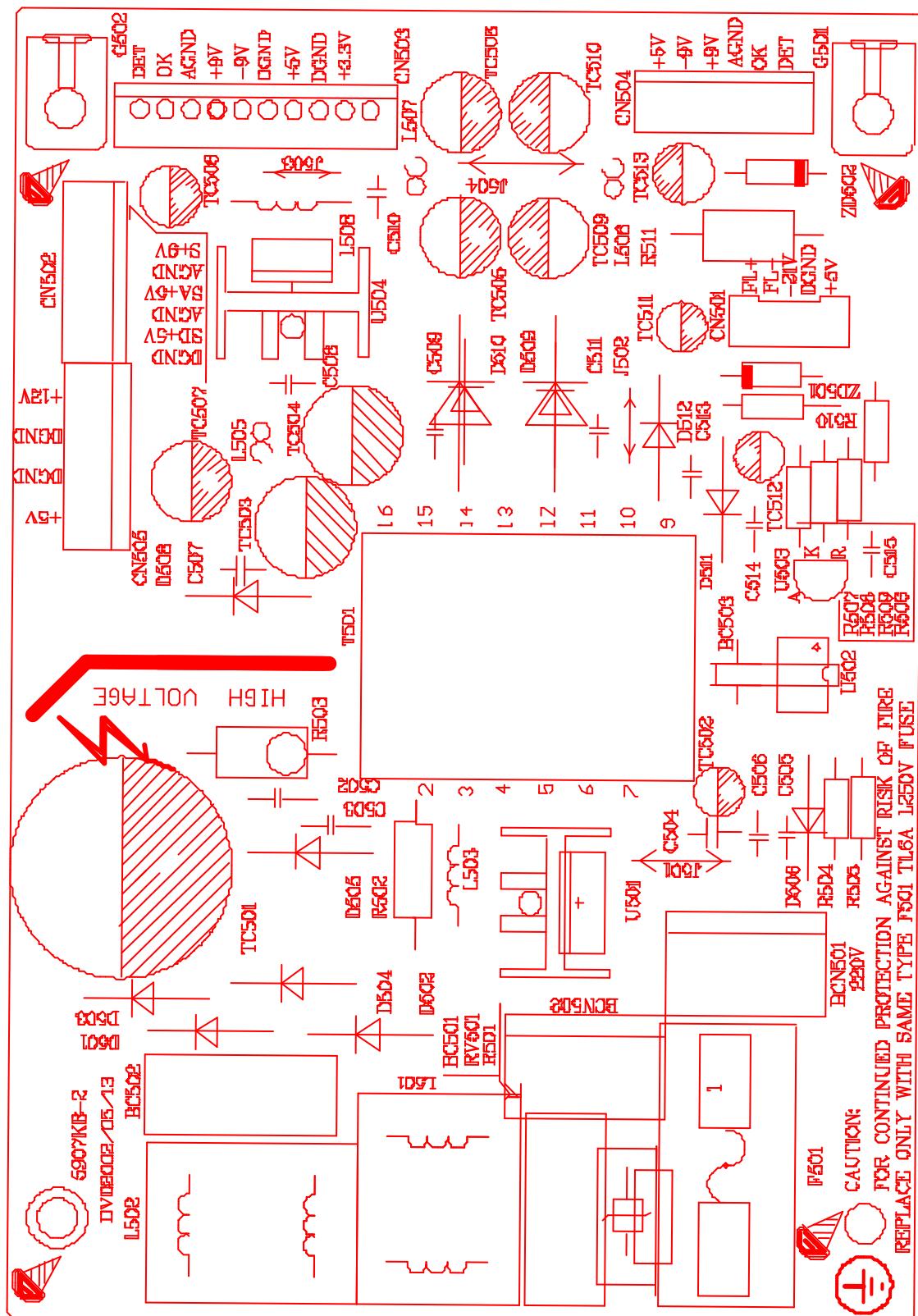
FRONT SCHEMATIC DIAGRAM



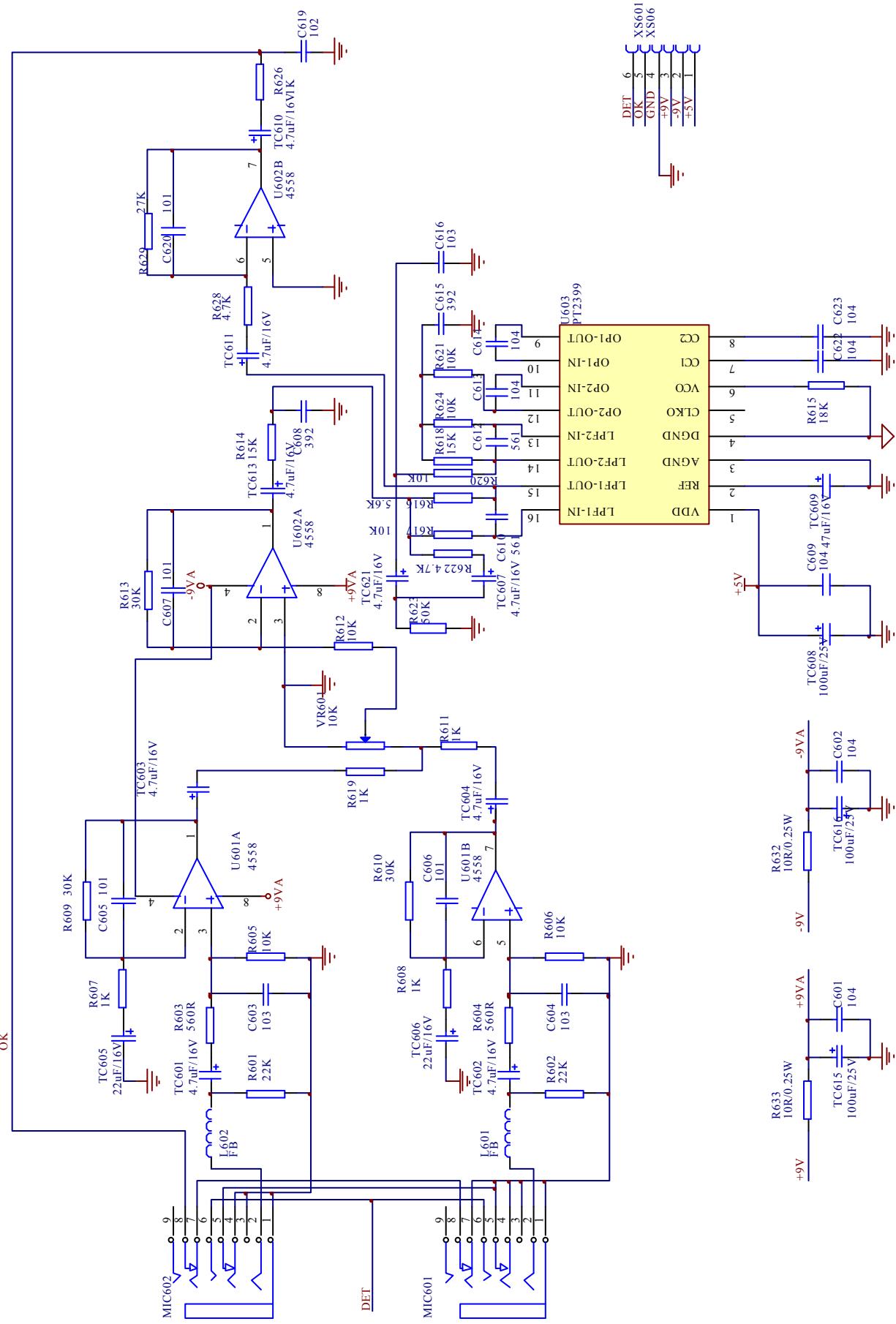
POWER BOARD SCHEMATIC DIAGRAM



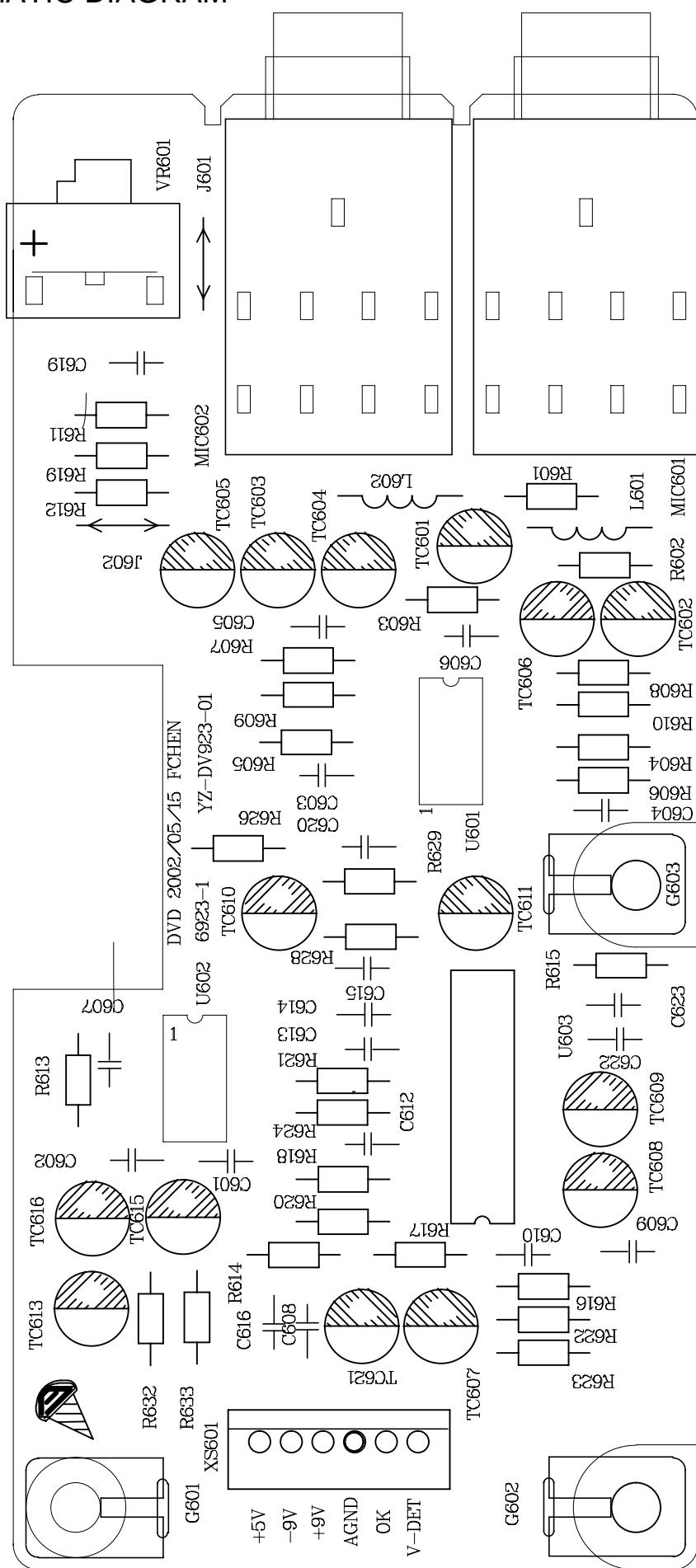
POWER BOARD SCHEMATIC DIAGRAM



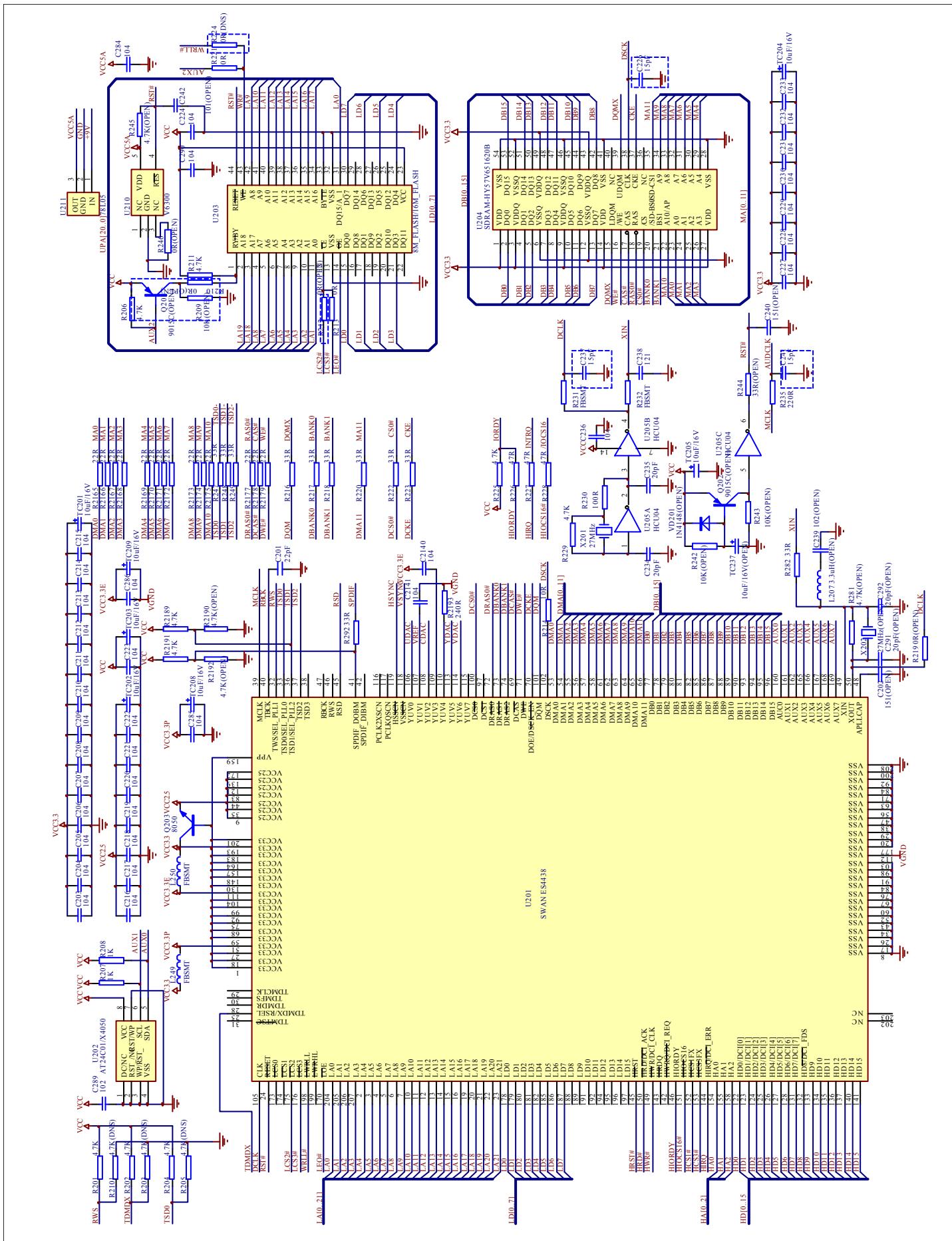
OK SCHEMATIC DIAGRAM



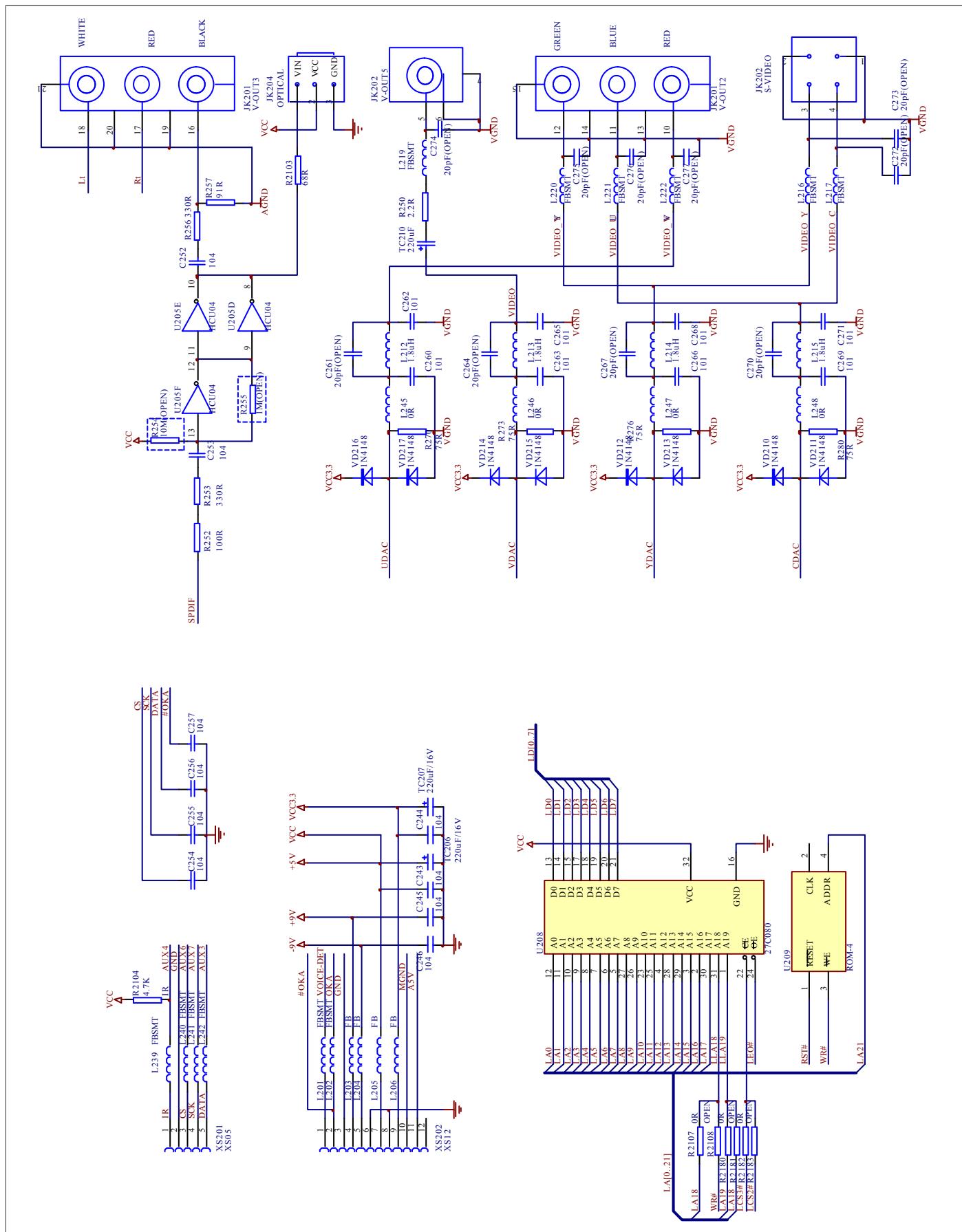
OK SCHEMATIC DIAGRAM



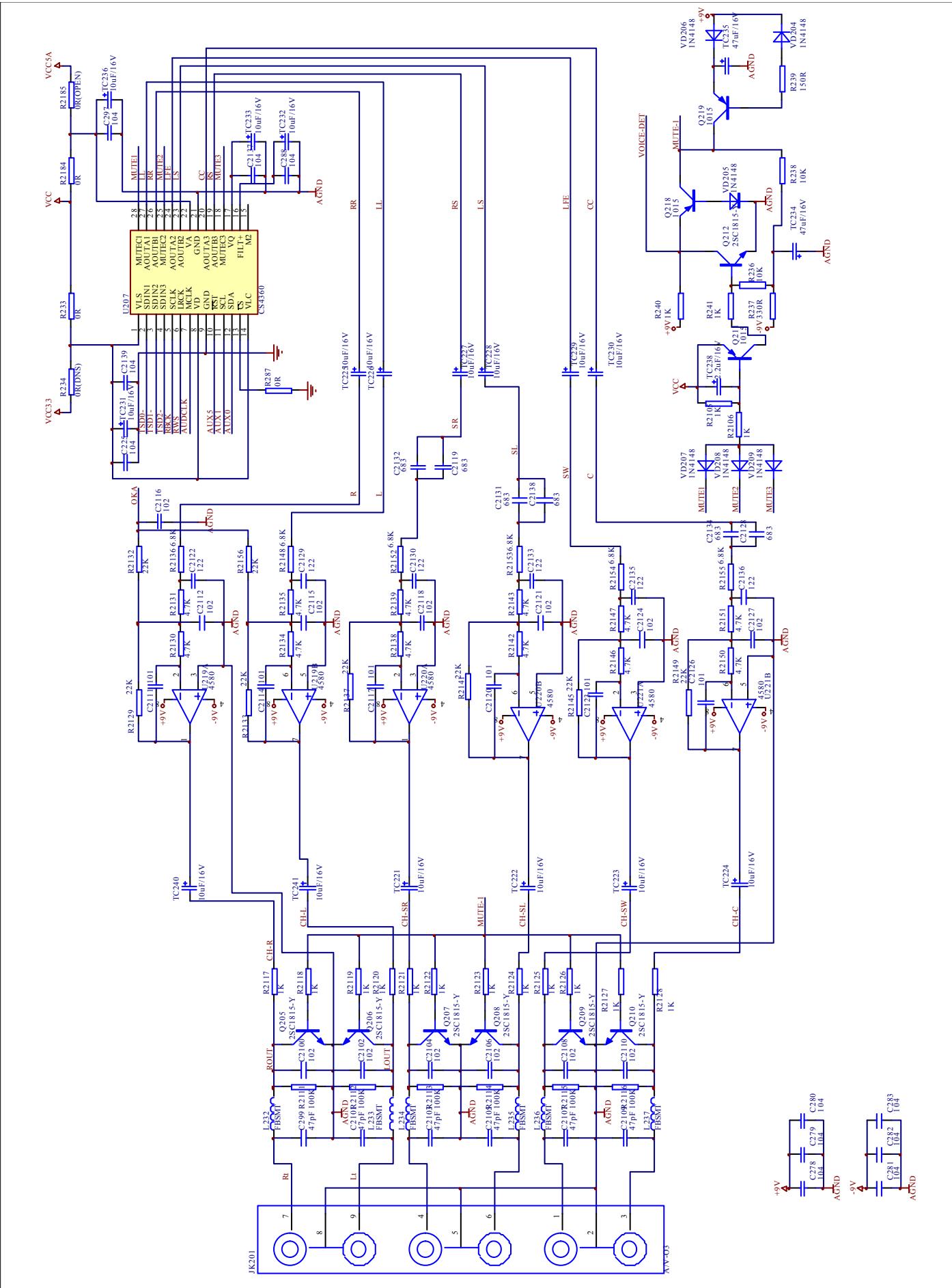
MIAN SCHEMATIC DIAGRAM



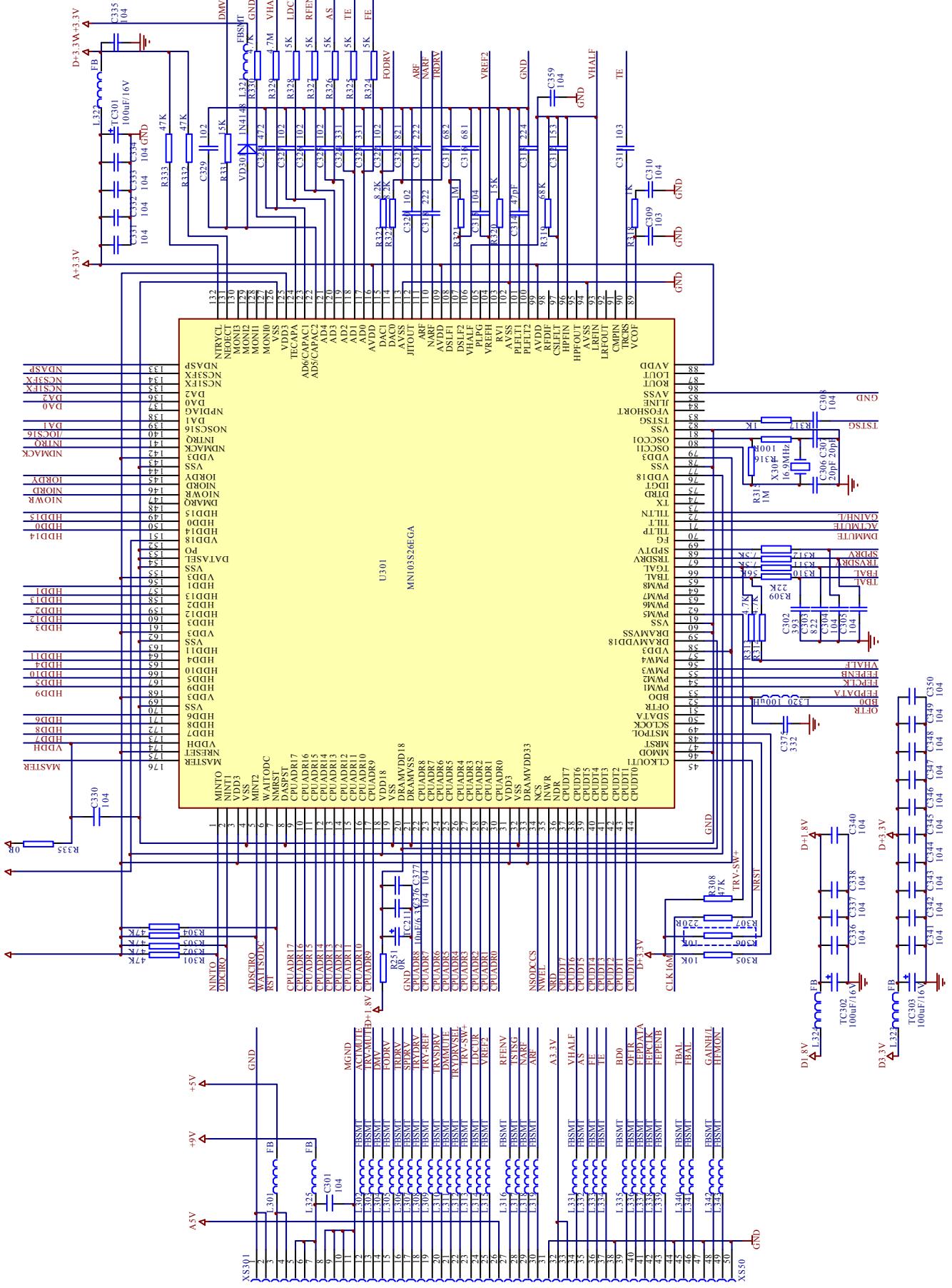
MIAN SCHEMATIC DIAGRAM



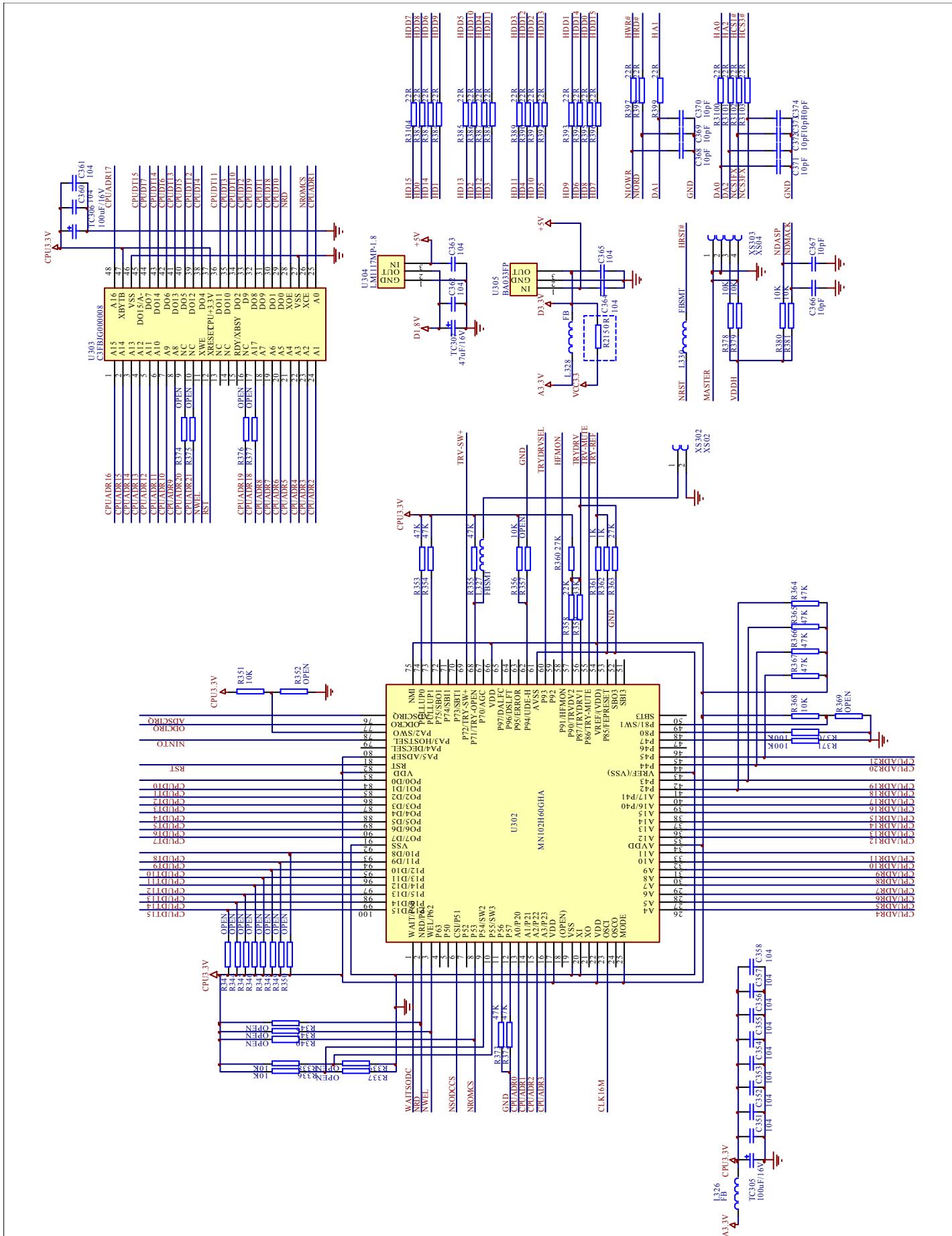
MIAN SCHEMATIC DIAGRAM



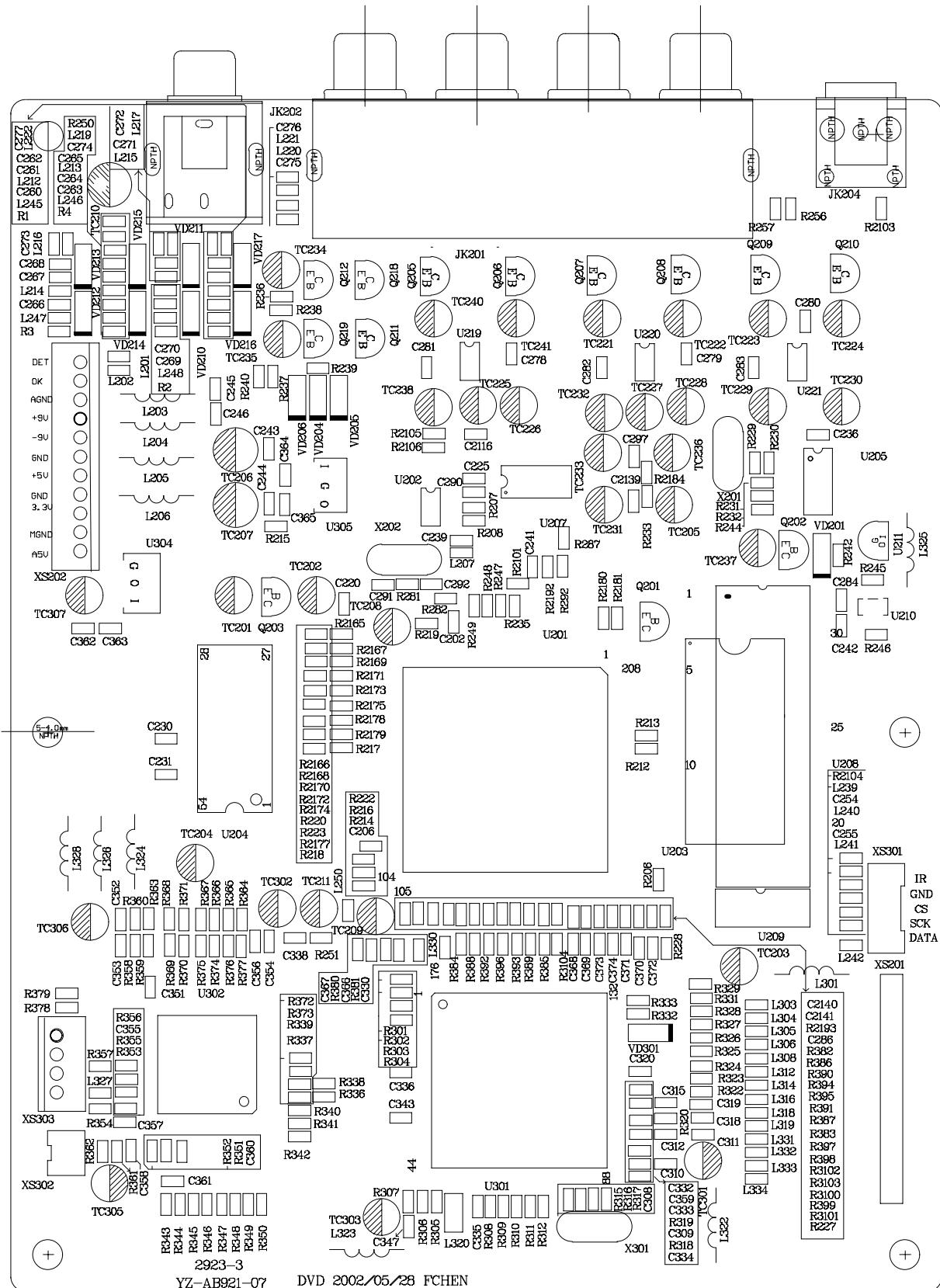
MIAN SCHEMATIC DIAGRAM



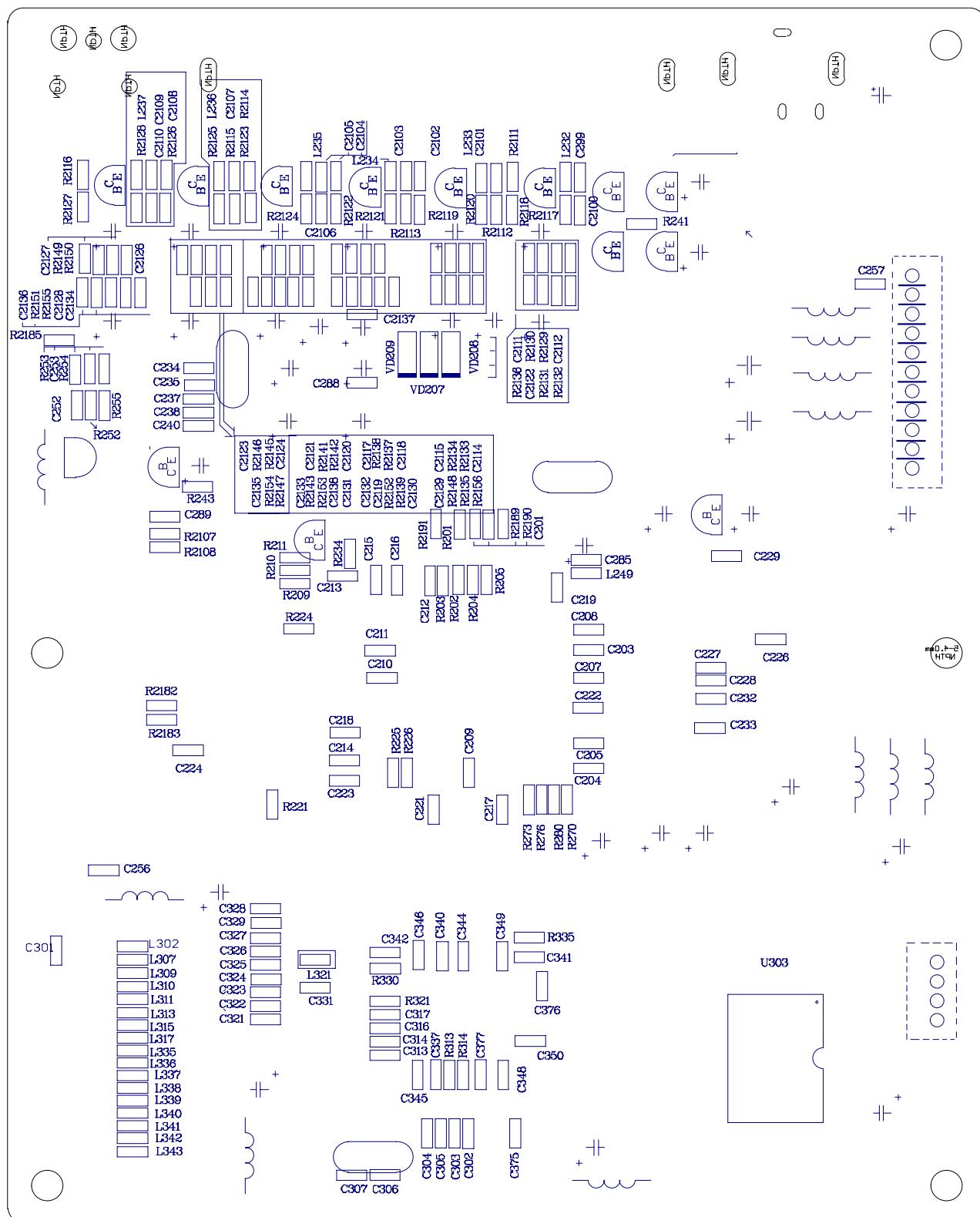
MIAN SCHEMATIC DIAGRAM



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11. SPARE PARTS LIST

BBK921D (RU) MATERIAL LIST

1. DECODE BOARD

NO	MATERIAL	SPECIFICATIONS/PART NUMBER	QUANTITY	LOCATION
1	CHIP RESISTOR	1/16W 0Ω ±5%	12	R213,R335,R287,R2184,L245~L248,R221,L320,R233,R251
2	CHIP RESISTOR	1/16W 2.2Ω ±5%	1	R250
3	CHIP RESISTOR	1/16W 10Ω ±5%	1	R214
4	CHIP RESISTOR	1/16W 22Ω ±5%	37	R382~R399,R2165~R2175,R2177~R2179,R3100~R3104
5	CHIP RESISTOR	1/16W 33Ω ±5%	10	R216~R218,R220,R222,R223,R247~R249,R292
6	CHIP RESISTOR	1/16W 47Ω ±5%	3	R226,R227,R228
7	CHIP RESISTOR	1/16W 68Ω ±5%	1	R2103
8	CHIP RESISTOR	1/16W 75Ω ±5%	4	R270,R273,R276,R280
9	CHIP RESISTOR	1/16W 91Ω ±5%	1	R257
10	CHIP RESISTOR	1/16W 100Ω ±5%	2	R252,R316
11	CHIP RESISTOR	1/16W 150Ω ±5%	1	R239
12	CHIP RESISTOR	1/16W 220Ω ±5%	2	R235,R307
13	CHIP RESISTOR	1/16W 270Ω ±5%	1	R2193
14	CHIP RESISTOR	1/16W 330Ω ±5%	3	R237,R253,R256
15	CHIP RESISTOR	1/16W 1K ±5%	22	R207,R208,R240,R241,R317,R318,R361,R362,R2105,R2106,R2117~R2128
16	CHIP RESISTOR	1/16W 4.7K ±5%	24	R201,R202,R204,R211,R225,R206,R313,R314,R330,R2104,R2130,R2131,R2134,R2135,R2138,R2139,R2142,R2143,R2146,R2147,R2150,R2151,R2189,R2192
17	CHIP RESISTOR	1/16W 6.8K ±5%	6	R2136,R2148,R2152,R2153,R2154,R2155
18	CHIP RESISTOR	1/16W 7.5K ±5%	2	R311,R312
19	CHIP RESISTOR	1/16W 8.2K ±5%	2	R322,R323
20	CHIP RESISTOR	1/16W 10K ±5%	13	R236,R238,R305,R306,R336,R338,R351,R357,R368,R378~R381
21	CHIP RESISTOR	1/16W 15K ±5%	7	R320,R324~R328,R331
22	CHIP RESISTOR	1/16W 20K ±5%	8	R2129,R2132,R2133,R2137,R2141,R2145,R2149,R2156
23	CHIP RESISTOR	1/16W 22K ±5%	2	R309,R358
24	CHIP RESISTOR	1/16W 27K ±5%	2	R360,R363
25	CHIP RESISTOR	1/16W 33K ±5%	1	R359
26	CHIP RESISTOR	1/16W 47K ±5%	16	R301~R304,R308,R332,R333,R353~R355,R364~R367,R372,R373
27	CHIP RESISTOR	1/16W 56K ±5%	1	R310
28	CHIP RESISTOR	1/16W 68K ±5%	1	R319
29	CHIP RESISTOR	1/16W 100K ±5%	9	R370,R371,R2111~R2116,R281
30	CHIP RESISTOR	1/16W 1MΩ ±5%	2	R315,R321
31	CHIP RESISTOR	1/16W 4.7MΩ ±5%	1	R329
32	CD	CD11 50V2.2U±20%5×11 2	3	TC232,TC233,TC238
33	CD	CD11 16V10U±20%5×11 2	15	TC208,TC209,TC221~TC230,TC240,TC241,T211
34	CD	CD11C 16V47U±20%5×7 2	15	TC205,TC231,TC234~TC236,TC301~TC303,TC305~TC307 TC201~TC204
35	CD	CD11 16V220U±20%6×12 2.5	3	TC206,TC207,TC210
36	CHIP CAPACITOR	50V 10P ±5% NPO 0603	9	C366~C374
37	CHIP CAPACITOR	50V 20P ±5% NPO 0603	2	C306,C307

38		CHIP CAPACITOR	50V 22P ±5% NPO 0603	1	C201
39		CHIP CAPACITOR	50V 47P ±5% NPO 0603	8	C299,C314,C2101,C2103,C2105,C2107,C2109,C291
40		CHIP CAPACITOR	50V 101 ±5% NPO 0603	14	C260,C262,C263,C265,C266,C268,C269,C271,C2111,C2114,C2117,C2120,C2123,C2126
41		CHIP CAPACITOR	50V 331 ±5% NPO 0603	2	C323,C324
42		CHIP CAPACITOR	50V 681 ±5% NPO 0603	1	C316
42.1		CHIP CAPACITOR	50V 681 ±10% 0603	1	C316
43		CHIP CAPACITOR	50V 821 ±10% 0603	1	C321
44		CHIP CAPACITOR	50V 102 ±10% 0603	21	C289,C320,C322,C325,C326,C327,C329,C2100,C2102,C2104,C2106,C2108,C2110,C2112,C2115,C2116,C2118,C2121,C2124,C2127,C239
45		CHIP CAPACITOR	50V 122 ±10% 0603	6	C2122,C2129,C2130,C2133,C2135,C2136
46		CHIP CAPACITOR	50V 222 ±10% 0603	2	C318,C319
47		CHIP CAPACITOR	50V 332 ±10% 0603	1	C375
48		CHIP CAPACITOR	50V 472 ±10% 0603	1	C328
49		CHIP CAPACITOR	50V 682 ±10% 0603	1	C317
50		CHIP CAPACITOR	50V 822 ±10% 0603	1	C303
51		CHIP CAPACITOR	50V 103 ±10% 0603	2	C309,C311
52		CHIP CAPACITOR	50V 153 ±10% 0603	1	C312
53		CHIP CAPACITOR	16V 393 ±10% 0603	1	C302
54		CHIP CAPACITOR	16V 683 ±10% 0603	6	C2119,C2128,C2131,C2132,C2134,C2138
55		CHIP CAPACITOR	50V 104 +80%-20% 0603	96	C203~C225,C227~C233,C236,C243~C246,C252,C253,C278~C286,C288,C290,C297,C301,C304,C305,C308,C310,C315,C330~C338,C340~C365,C2137,C2139,C2140,C2141,C376~C377
	55.1	CHIP CAPACITOR	25V 104 +80%-20% 0603	96	C203~C225,C227~C233,C236,C243~C246,C252,C253,C278~C286,C288,C290,C297,C301,C304,C305,C308,C310,C315,C330~C338,C340~C365,C2137,C2139,C2140,C2141,C376~C377
56		CHIP CAPACITOR	16V 224 +80%-20% 0603	1	C313
57		CHIP CAPACITOR	50V 27P ±5% NPO 0603	1	C292
58	CHIP	INDUCTANCE	1.8uH ±10% 1608	4	L212~L215
59	CHIP	INDUCTANCE	RH354708	11	L203~L206,L301,L322~L326,L328
60	CHIP	INDUCTANCE	3.3uH ±10% 1608	1	L207
61		CHIP MAGNETIC BEADS	FCM1608K-221T05	55	L201,L202,L216,L217,L219~L222,L232~L237,L239~L242,L249,L250,L302~L319,L321,L327,L330~L343,R219
62		CHIP DIODE	1N4148	15	VD204~VD217,VD301
	62.1	CHIP DIODE	LS4148	15	VD204~VD217,VD301
	62.2	CHIP DIODE	LL4148	15	VD204~VD217,VD301
63		TRIODE	S8050D	1	Q203
64		TRIODE	C1815Y	7	Q205~Q210,Q212
65		TRIODE	2SA1015	3	Q211,Q218,Q219
66		IC	HA178L05PA TO-92M	1	U211
67		IC	NJM4558M SOP	3	U219,U220,U221
	67.1	IC	4580 SOP	3	U219,U220,U221
	67.2	IC	4558 SOP	3	U219,U220,U221
68		IC	MM74HCU04M SOP	1	U205

	68.1	IC	HCU04 SOP	1	U205
69		IC	MT48LC4M16A2-75C SOP	1	U204
	69.1	IC	D4564163G5-A80 SOP	1	U204
	69.2	IC	HY57V641620HGT-H TSOP	1	U204
70		IC	CS4360 SSOP	1	U207
71		IC	AT24C01A SOP	1	U202
72		电光转换器	GP1F32T	1	JK204
	72.1	电光转换器	TX178A	1	JK204
73		IC	ES6018F QFP	1	U201
74		IC	MN102H60GHC LQFP	1	U302
75		IC	MN103S26EGA LQFP	1	U301
76		IC	BA033FP TO252-3	1	U305
77		IC	LM1117MP-1.8 SOT-223	1	U304
78		IC	V6300F SOT-23 5L	1	U210
79		SOFTWARE PROGRAM FLASH	ROM921DS-0A(8M)	1	
80		SOFTWARE PROGRAM FLASH	220 (2M)	1	
81		CRYSTAL OSCILLATOR	16.9344MHZ 49-U	1	X301
82		CRYSTAL OSCILLATOR	27.00MHz 49-U	1	X202
83		PCB	2923-3	1	
84		TERMINAL SOCKET	AV12-8.4-2G	1	JK201
85		TERMINAL SOCKET	CS-09	1	JK202
86		SOCKET	5 PIN 2.0mm	1	XS201
87		SOCKET	2 PIN 2.0mm	1	XS302
88		SOCKET	11 PIN 2.5mm	1	XS202
89		CABLE SOCKET	50 PIN 0.5mm CHIP WITHOUT CLASP	1	XS301

2、POWER BOARD

NO	MATERIAL	SPECIFICATIONS/PART NUMBER	QUANTITY	LOCATION
1	CARBON-FILM RESISTOR	1/4W33Ω±5% SHAPED 10	1	R505
2	CARBON-FILM RESISTOR	1/4W330Ω±5% SHAPED 10	1	R506
3	CARBON-FILM RESISTOR	1/4W10K±5% SHAPED 10	1	R507
4	CARBON-FILM RESISTOR	1/4W4.7K±5% SHAPED 10	1	R510
5	CARBON-FILM RESISTOR	1/4W1MΩ±5% SHAPED 10	1	R504
6	METAL FILM RESISTOR	1/4W4.7K±1%	1	R508
7	METAL FILM RESISTOR	1/4W12K±1% SHAPED 10	1	R509
8	METAL OXIDE FILM RESISTOR	1W330Ω±5% R-SHAPED 15×8	1	R511
9	METAL OXIDE FILM RESISTOR	2W39K±5% FLAT- SHAPED 15×9	1	R503
10	METAL OXIDE FILM RESISTOR	2W120K±5% SHAPED 15	1	R502

11	HIGH VOLTAGE RESISTOR	1/2W680K±5%	1	R501
12	PORCELAIN CAPACITOR	50V 100P ±10% 5mm	6	C505,C507,C509,C511,C513,C514
13	PORCELAIN CAPACITOR	50V 104 ±20% 5mm	4	C504,C508,C510,C515
14	PORCELAIN CAPACITOR	1000V 101 +80%-20% 7.5mm	1	C503
14.1	PORCELAIN CAPACITOR	1000V 101 ±10% 7.5mm	1	C503
15	PORCELAIN CAPACITOR	1000V 103 +80%-20% 7.5mm	1	C502
16	CERAMIC CAPACITOR	CT81 400V 221±20% 10mm	1	BC503
16.1	CERAMIC CAPACITOR	CT81 400V221±10% 10mm	1	BC503
17	TERYLENE CAPACITOR	100V 223 ±10% 5mm	1	C506
18	TERYLENE CAPACITOR	275V 104 ±20% 15mm	1	BC501
18.1	TERYLENE CAPACITOR	275V 104 ±10% 15mm	1	BC501
19	CD	GZ16V100U±20%6×12 2.5	3	TC508,TC511,TC513
19.1	CD	CD11 16V100U±20%6×12 2.5	3	TC508,TC511,TC513
19.2	CD	CD110 16V100U±20%6×12 2.5	3	TC508,TC511,TC513
19.3	CD	CD11C 16V100U+20%-15%6×7 2.5	3	TC508,TC511,TC513
19.4	CD	CD11C 16V100U±20%6×7 2.5	3	TC508,TC511,TC513
20	CD	CD11 16V470U±20%8×123.5	2	TC503,TC504
21	CD	CD11 50V47U±20%6×12 2.5	2	TC502,TC512
22	CD	CD11 10V1000U±20%8×16 3.5	4	TC505,TC506,TC509,TC510
22.1	CD	CD11 10V1000U±20%8×14 3.5	4	TC505,TC506,TC509,TC510
22.2	CD	GS 10V1000U±20%8×16 3.5	4	TC505,TC506,TC509,TC510
22.3	CD	GS 10V1000U±20%8×14 3.5	4	TC505,TC506,TC509,TC510
23	CD	LS 400V47U±20%22×25 10	1	TC501
23.1	CD	LP3 400V47U±20%22×28 10	1	TC501
24	MAGNETIC BEADS INDUCTANCE	RH354708	1	L503
25	CHOKE COIL	VERTICAL 10UH 1A 5mm	1	L505
26	CHOKE COIL	VERTICAL 10UH 2A 5mm	2	L506,L507
27	SWITCH POWER TRANSFORMER	BCK-4025B-2876	1	T501
28	DIODE	HER105	4	D506,D508,D511,D512
29	DIODE	HER306	1	D510
30	SCHOTTKY DIODE	SR360	1	D509
31	DIODE	HER107	1	D505
32	VOLTAGE REGULATOR	5.1V 1/2W	1	ZD501
33	VOLTAGE REGULATOR	9.1V 1W	1	ZD502
34	DIODE	1N4007	4	D501~D504
35	IC	5L0380R YDTU	1	U501
36	IC	LM431ACZ TO-92	1	U503
36.1	IC	TL431C TO-226AA(LP)	1	U503
36.2	IC	431L TO-92	1	U503
36.3	IC	KA431AZ TO-92	1	U503

37	POWER GRID FILTER	UT-20 40mH ±20% 10×13	1	L502
38	PHOTOELECTRIC COUPLER	NEC2561	1	U502
38.1	PHOTOELECTRIC COUPLER	PC817	1	U502
38.2	PHOTOELECTRIC COUPLER	NEC2501	1	U502
38.3	PHOTOELECTRIC COUPLER	HS817	1	U502
38.4	PHOTOELECTRIC COUPLER	817D	1	U502
39	IC	LM7805 GOLD SEALED TO-220	1	U504
40	PCB	5907KB-2	1	
41	SOCKET	5 PIN 2.0mm	1	CN501
42	SOCKET	9 PIN 2.5mm	1	CN503
43	SOCKET	2 PIN 2.5mm	1	CN502
44	SOCKET	6 PIN 2.5mm	1	CN504
45	SOCKET	2 PIN 8.0mm 2#	2	BCN501,BCN502
46	CONNECTION CORDS	Φ0.6 SHAPED 7.5mm	2	J502,J503
47	CONNECTION CORDS	Φ0.6 SHAPED 10mm	3	L501,J501
48	CONNECTION CORDS	Φ0.6 SHAPED 12.5mm	1	J504
49	FUSE HOLDER	T1.6AL 250V	1	F501
50	FUSE HOLDER	BLX-2	1	USED FOR F501
51	RADIATOR BOARD	11×15×25 AB009K	2	U501,U504 FOR HEAT RADIATION
51.1	RADIATOR BOARD	11×15×25 WHITE AB905	2	U501,U504 FOR HEAT RADIATION
52	GROUND CHIP OF THE POWER BOARD	AB903	2	G501~G502
53	TAPPING SCREW	BT 3×8 BLACK	2	FIX THE RADIATOR BOARD

3. KARAOKE BOARD

NO	MATERIAL	SPECIFICATIONS/PART NUMBER	QUANTITY	LOCATION
1	CARBON-FILM RESISTOR	1/6W560Ω±5% SHAPED 7.5	2	R603,R604
2	CARBON-FILM RESISTOR	1/6W1K±5% SHAPED 7.5	5	R607,R608,R611,R619,R626
3	CARBON-FILM RESISTOR	1/6W4.7K±5% SHAPED 7.5	3	R622,R628,R623
4	CARBON-FILM RESISTOR	1/6W5.6K±5% SHAPED 7.5	1	R616
5	CARBON-FILM RESISTOR	1/6W10K±5% SHAPED 7.5	7	R605,R606,R612,R617,R620,R621,R624
6	CARBON-FILM RESISTOR	1/6W22K±5% SHAPED 7.5	2	R601,R602
7	CARBON-FILM RESISTOR	1/6W10Ω±5% SHAPED 7.5	2	R632,R633
8	CARBON-FILM RESISTOR	1/6W15K±5% SHAPED 7.5	2	R614,R618
9	CARBON-FILM RESISTOR	1/6W18K±5% SHAPED 7.5	1	R615
10	CARBON-FILM RESISTOR	1/6W27K±5% SHAPED 7.5	1	R629

11	CARBON-FILM RESISTOR	1/6W30K±5% SHAPED 7.5	3	R613,R609,R610
12	VOLTAGE REGULATOR POTENTIOMETER	R0901N-BA1-B10K	1	VR601
13	PORCELAIN CAPACITOR	50V 100P ±10% 5mm	4	C607,C620,C605,C606
14	PORCELAIN CAPACITOR	50V 561 ±10% 5mm	2	C610,C612
15	PORCELAIN CAPACITOR	50V 103 ±10% 5mm	4	C603,C604,C616,C619
16	PORCELAIN CAPACITOR	50V 104 ±20% 5mm	7	C601,C602,C609,C622,C623,C613,C614
17	PORCELAIN CAPACITOR	50V 392 ±10% 5mm	2	C608,C615
18	CD	CD11 16V22U±20%5×11 2	2	TC605,TC606
19	CD	CD11 10V47U±20%5×7 2	1	TC609
19.1	CD	CD11C 16V47U±20%5×7 2	1	TC609
20	CD	CD11 25V100U±20%6×12 2.5	3	TC615,TC616,TC608
21	CD	CD11 16V4.7U±20%5×11 2	9	TC601~TC604,TC610,TC611,TC613,TC621,TC607
22	MAGNETIC BEADS INDUCTANCE	RH354708	2	L601,L602
23	IC	NJM4558D DIP	2	U601,U602
24	IC	PT2399 DIP	1	U603
25	PCB	6923-1	1	
26	RAFT CORDS	6P120 2.5 2 PLUG WITH NEEDLES SAME DIRECTION	1	xs601
27	MIC SOCKET	CK3-6.35-106	2	MIC601,MIC602
28	CONNECTION CORDS	Φ0.6 SHAPED 7.5mm	2	J602,J601
29	GROUND CHIP THE POWER BOARD	AB903	3	G601~G603

4、MAIN FRONT PANEL

NO	MATERIAL	SPECIFICATIONS/PART NUMBER	QUANTITY	LOCATION
1	SOFT SPONGE SPACER	15×7×3.5 DOUBLE SIDED TAPE	3	CONNECT VFD DISPLAY WITH THE FRONT PANEL'S PCB
2	SOFT SPONGE SPACER	10×10×9 DOUBLE SIDED TAPE	1	CONNECT THE INFRARED SENSOR WITH PCB
3	CARBON FILM RESISTOR	1/4W2.2Ω±5% SHAPED 10	1	R418
4	CARBON FILM RESISTOR	1/4W100Ω±5%	1	R415
4.1	CARBON FILM RESISTOR	1/4W100Ω±5% SHAPED 10	1	R415
5	CARBON FILM RESISTOR	1/4W10K±5%	7	R406~R410,R416,R417
5.1	CARBON FILM RESISTOR	1/4W10K±5% SHAPED 10	7	R406~R410,R416,R417
6	CARBON FILM RESISTOR	1/4W33K±5%	9	R401~R405,R411~R414
6.1	CARBON FILM RESISTOR	1/4W33K±5% SHAPED 10	9	R401~R405,R411~R414
7	PORCELAIN CAPACITOR	50V 100P ±10% 5mm	3	C403,C404,C406

8		PORCELAIN CAPACITOR	50V 103 +80%-20% 2.5mm	2	C401,C405
	8.1	PORCELAIN CAPACITOR	50V 103 ±20% 2.5mm	2	C401,C405
9		CD	CD11C 10V100U±20%5×7 2	2	C402,C407
10		DIODE	1N4148	3	D401~D403
11		IC	D16312GB QFP	1	U401
	11.1	IC	PT6312LQ QFP	1	U401
12		VFD	HNV-05SS32	1	U402
13		LIGHT TOUCH RESTORE SWITCH	VERTICAL 6×6×1	9	K401~K409
14		PCB	4921-0	1	
15		CONNECTION CORDS	Φ0.6 SHAPED 10mm	6	JP401,JP402,JP404~JP407
16		CONNECTION CORDS	Φ0.6 SHAPED 15mm	1	JP403
17		RAFT CORDS	5P240 2.0 2 PLUG WITH L NEEDLES, REVERSED	2	XS401,XS402
18		INFRARED SENSOR	HS0038A2	1	U403