PLL bringup:
1. VCTCXO starts up
2. FX3 brings up Catalina, sets CLKOUT to FPGA
3. FX3 programs FPGA
4. FPGA writes to PLL, initializes PLL
5. PLL locks to external ref if avail.
6. If no ref, PLL tristated via SPI

SMA External Reference

15dBm max. (3.5V into 50 ohms)

J100 142-0701-871

C100 0.1uF

R128 10K

D100

R126 10K

C104 0.1uF

R110 49.9

C111 0.1uF

DG4157DL U103

SN74LVC1G3157 works too

ref_sel

C150 0.1uF

C106 0.1uF

C107 0.1uF

ADF4001 U101

xo_to_pll

C151 0.1uF

C112 100pF

R111 4.7K

R120 1M

R124 100K

R118 DNP

auxdac1

R125 47.0K 1%

C137 180pF

C139 82pF

C138 2.2nF

R121 1M

vcxo_tune

pll_lock_filt

pll_sclk_filt

pll_mosi_filt

pll_ce_filt

Assume 400Hz/Volt
4kHz loop bandwidth
10MHz compare frequency
5mA CP current
reduce C139 by the load cap of trace + tune
Eff. Kv is adjusted based on the resistor div
formed by R124 and the impedance
of the VCTCXO input (~10K)

LAYOUT:
R110 and C150 Should be close to U101

GPSDO

L100 MI1206K601R-10

C101 0.1uF

C102 22uF X5R 6.3V

U100 M9107

R100 4.7K

J101 142-0701-871

gps_rxd

R106 100

R127 150

gps_lock

PPS_IN_INT

gps_txd_nmea

gps_txd

C108 47uF 6.3V X5R

GPS antenna

S100 JLEAD_SW

R108 150

LED100 GPSDO lock LED

Q100

R109 10K

External PPS input

5V max.

J104 142-0701-971

R103 1K

R102 49.9

C103 1000pF

R104 2K

U102 SN74AUP1T57

PPS_IN_EXT

C116 0.1uF

L107 MI1206K601R-10

VCTCXO X100

C105 10uF X5R 6.3V

C109 0.1uF

vcxo_tune

C119 470pF

R122 510K

R123 510K

C118 0.01uF

C117 0.1uF

Place at U106

U106 SN74LVC1G04

net=3.3V_CLK:5
net=GND:3
Self-biasing clock squarer

U104 CDLVC1103PWR

R113 47 xo_out To Catalina

R119 47 xo_to_pll To PLL RF in

U105 FIN1001

codec_main_clk_p Buffer to FPGA
codec_main_clk_n Place near U104

net=3.3V_CLK:1
net=GND:2

C110 10uF X5R 6.3V

C113 0.1uF

C114 0.1uF

Place at U105

R101 2.2K

R105 1K

R107 1K

R112 1K

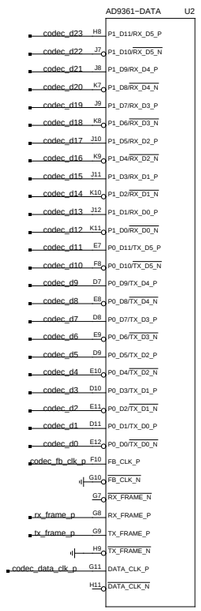
C115 470pF

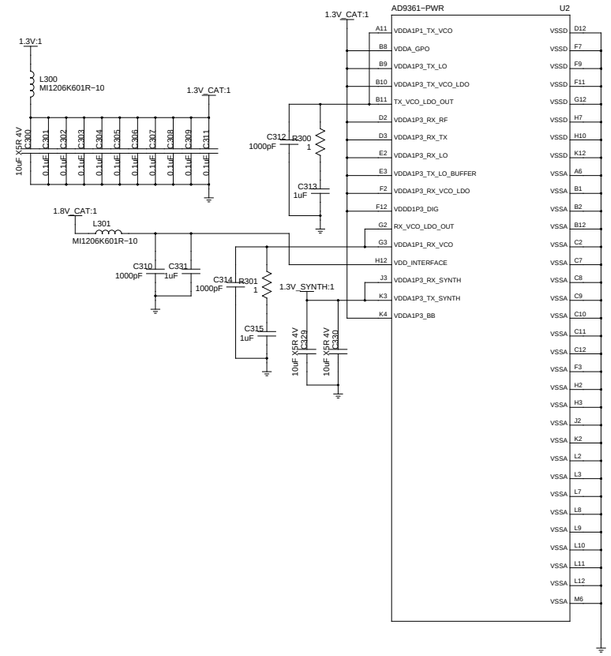
C120 470pF

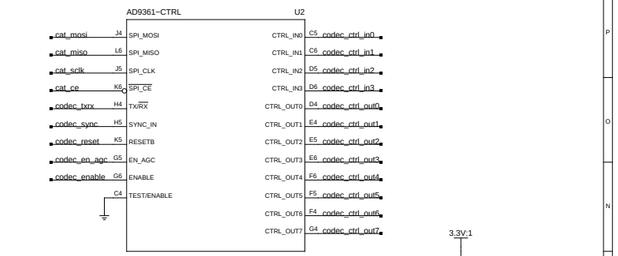
C121 470pF

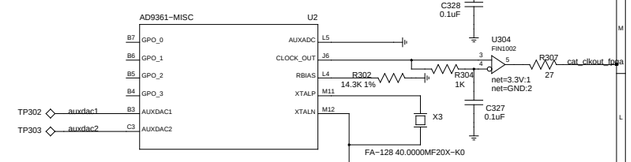
C122 470pF

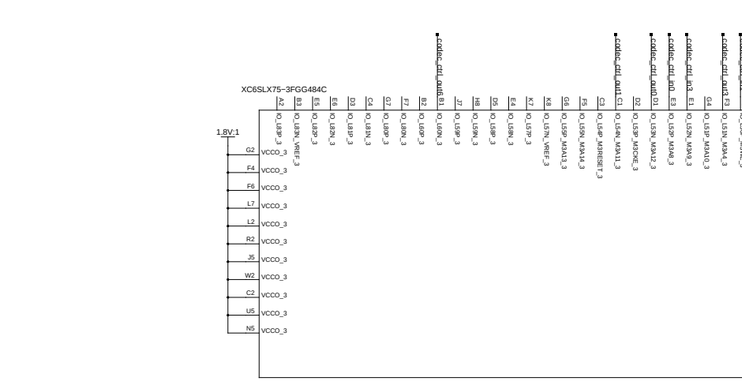
TITLE	B200 Clock
FILE: clock.sch	REVISION: 2
PAGE 1 OF 8	DRAWN BY: nick, matt





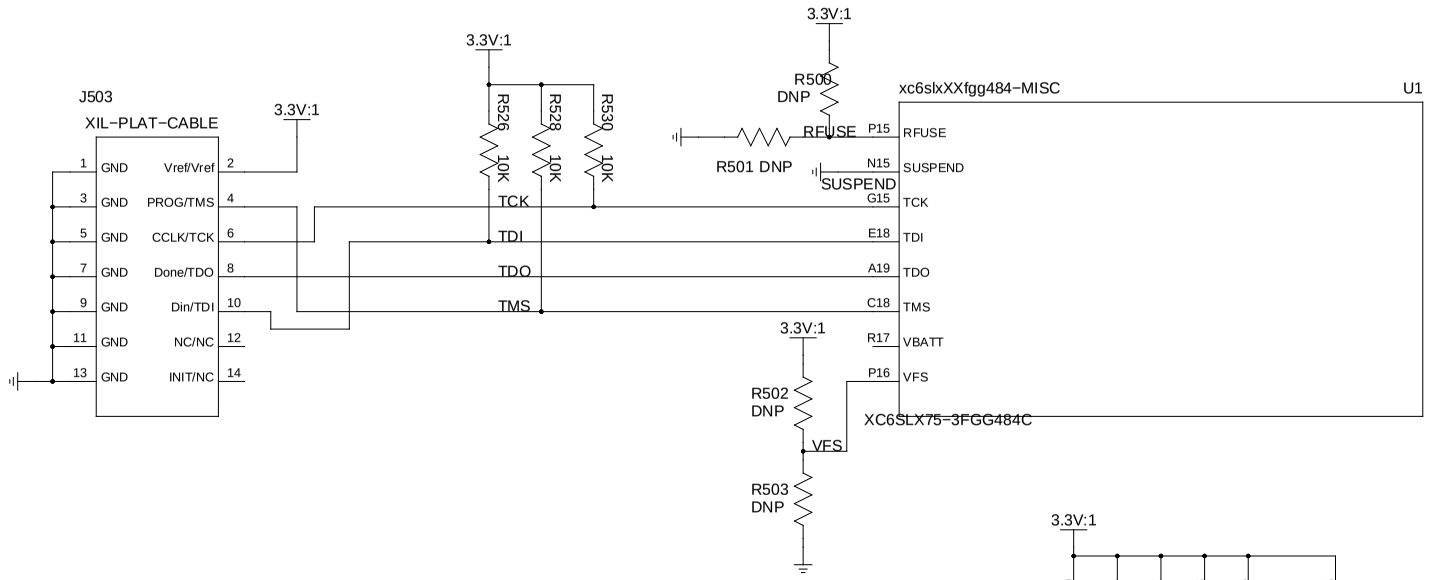


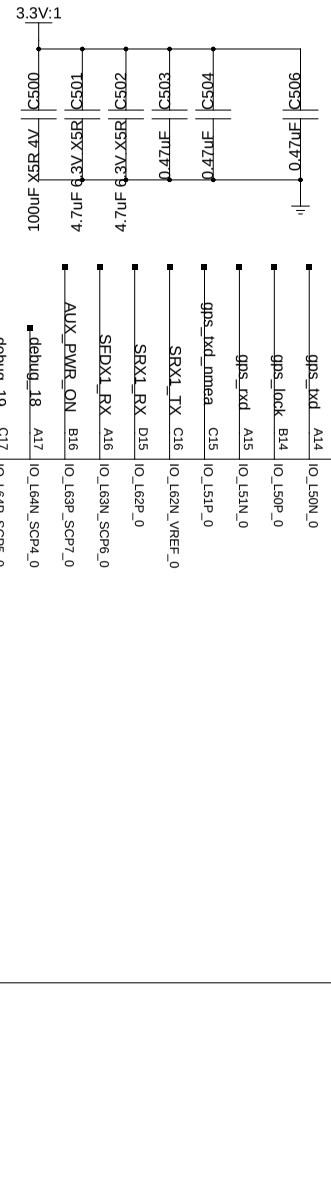


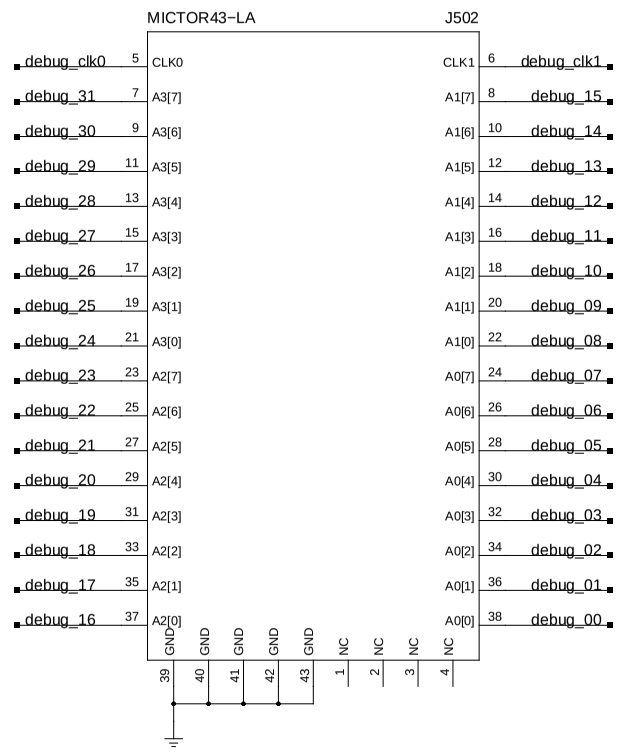


codec_main_clk is the main FPGA clock (for timestamps, serial timing, etc.)
codec_data_clock is the RX data clock (received from Catalina)
codec_fb_clk is the TX data clock (sent to Catalina,
just the data_clock turned back around)
GCLK24/25 and GCLK26/27 are both on the LT
clock bus. GCLK22 shares a BUFGMUX with
GCLK30, which is unused.

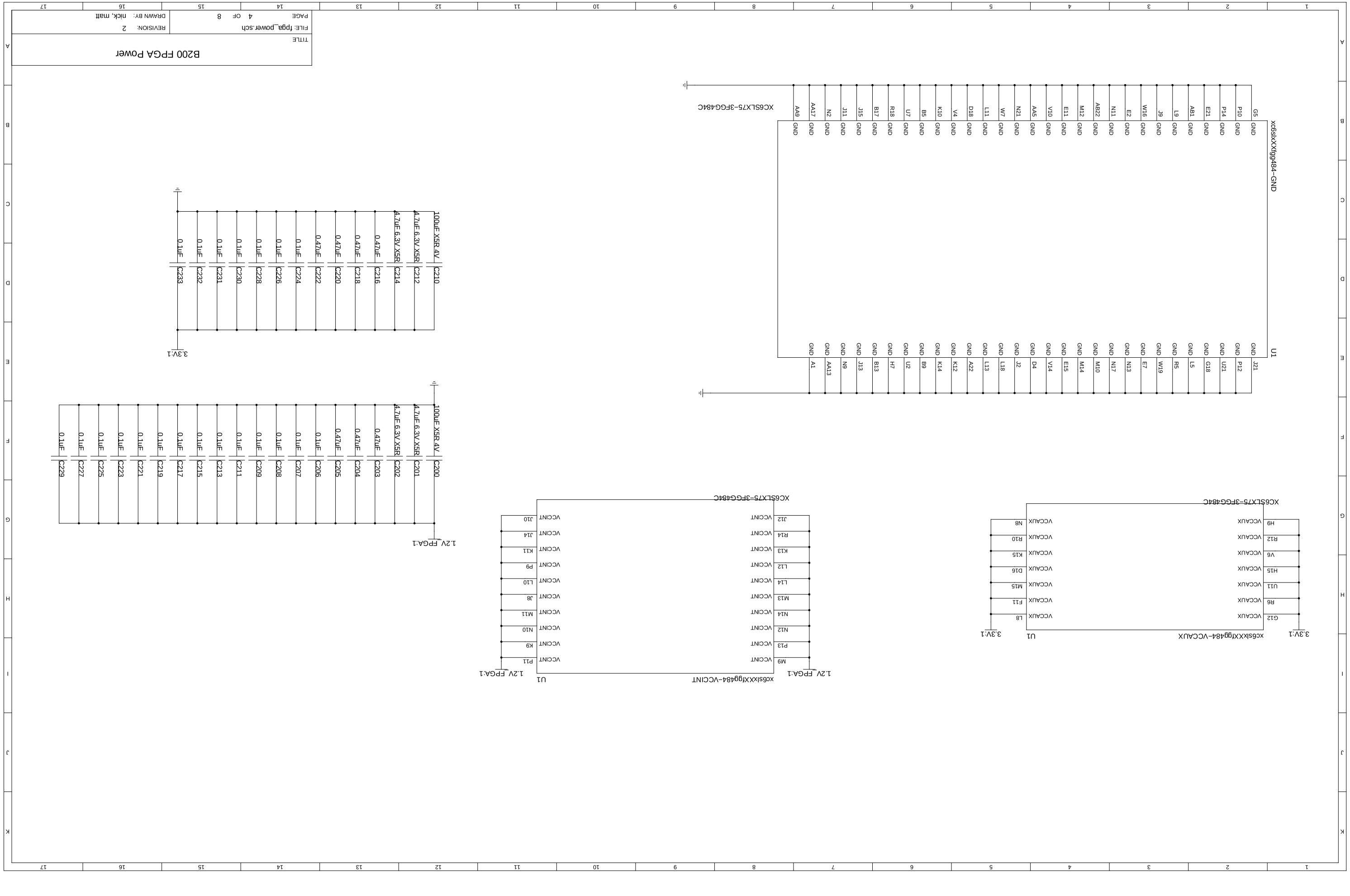
TITLE:	B200 AD9361-FPGA Interface
FILE: fpga_codec.sch	REVISION: 2
PAGE 2 OF 8	DRAWN BY: nick, matt

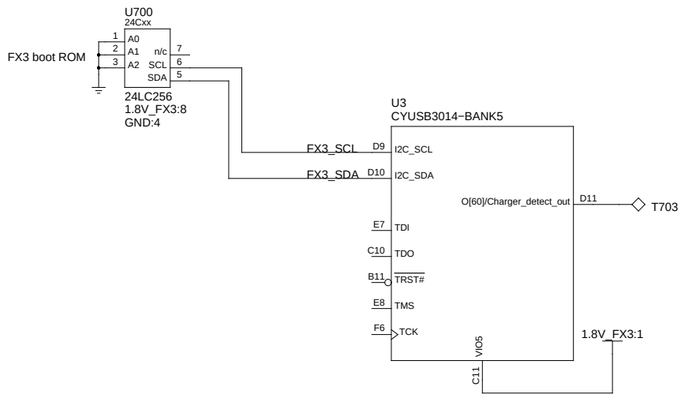


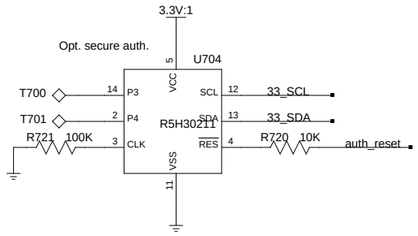


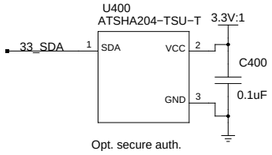


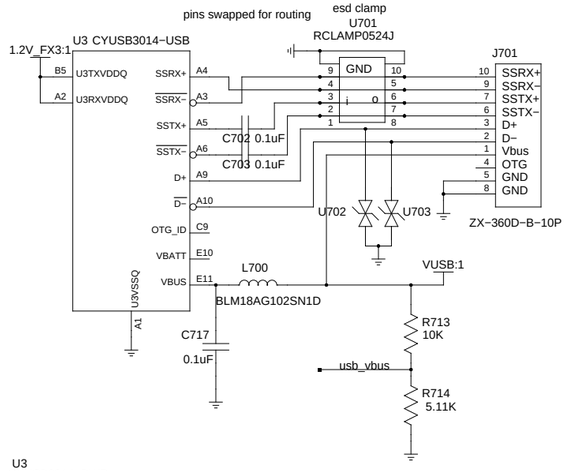
B200 debug and misc	
TITLE	
FILE: fpga_debug.sch	REVISION: 2
PAGE 3 OF 8	DRAWN BY: nick, matt

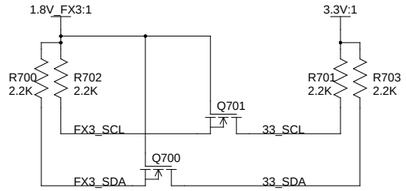

B200 FPGA Power
FILE: fpga_power.sch
REVISION: 2
DRAWN BY: nick, matt
PAGE 4 OF 8
xc6slxXfgg484-GND
U1
XC6SLX75-3FGG484C
GND
xc6slxXfgg484-VCCAUX
VCCAUX
3.3V_1
xc6slxXfgg484-VCCINT
VCCINT
1.2V_FPGA_1
100uF X5R 4V
4.7uF 6.3V X5R
0.47uF
0.1uF

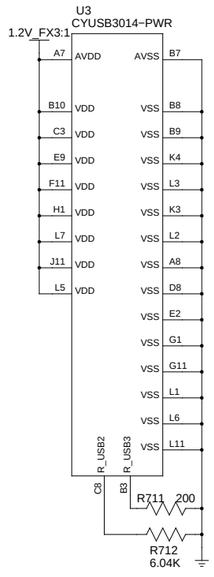


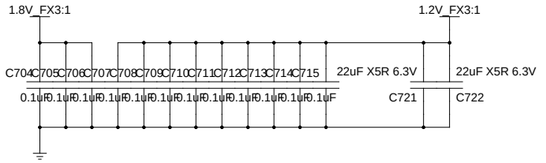




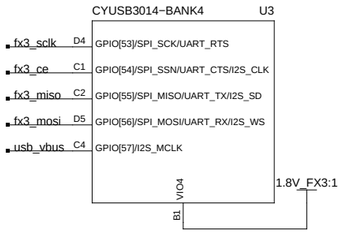


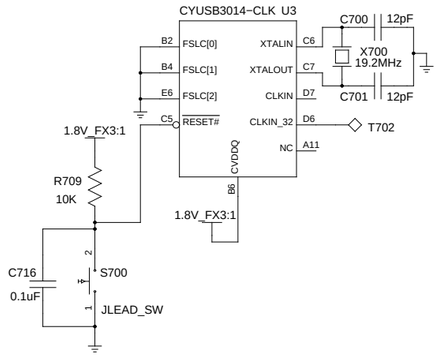




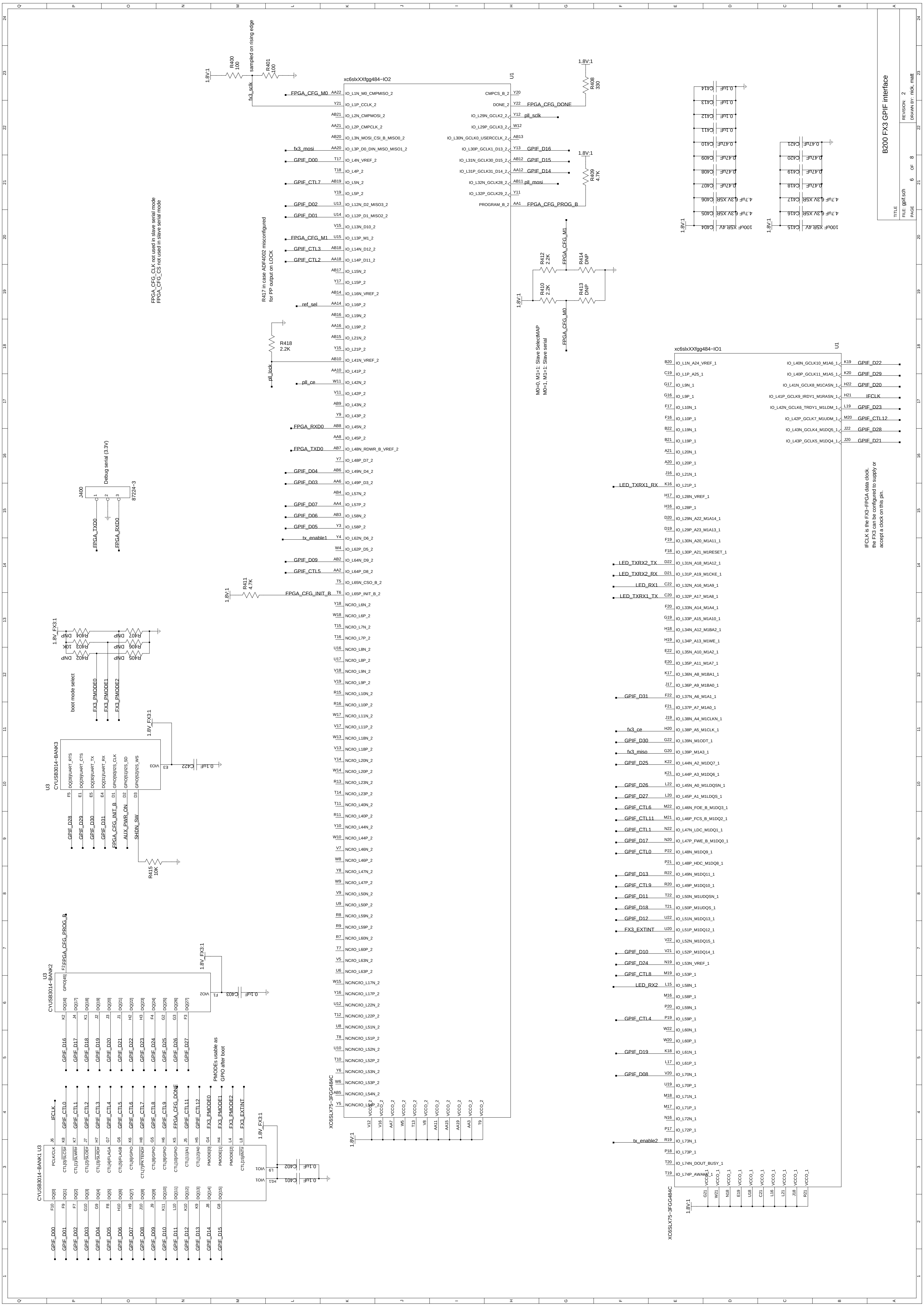


SPI is unusable in 32−bit GPIF mode.





TITLE	B200 FX3 interface
FILE: fx3.sch	REVISION: 2
PAGE 5 OF 8	DRAWN BY: nick, matt


B200 FX3 GPIF interface
TITLE
FILE: gpif.sch
PAGE 6 OF 8
REVISION: 2
DRAWN BY: nick, matt
xc6slxXXfgg484~IO2
U1
XC6SLX75~3FGG484C
xc6slxXXfgg484~IO1
sampled on rising edge
fx3_sclk
R400 100
R401 100
R408 330
R409 4.7K
R410 2.2K
R412 2.2K
R413 DNP
R414 DNP
R411 4.7K
R418 2.2K
R415 10K
R417 in case ADF4002 misconfigured for PP output on LOCK
FPGA_CFG_CLK not used in slave serial mode
FPGA_CFG_CS not used in slave serial mode
M0=0, M1=1: Slave SelectMAP
M0=1, M1=1: Slave serial
IFCLK is the FX3->FPGA data clock, the FX3 can be configured to supply or accept a clock on this pin.
J400
87224~3
Debug serial (3.3V)
FPGA_TXD0
FPGA_RXD0
boot mode select
FX3_PMODE0
FX3_PMODE1
FX3_PMODE2
U3
CYUSB3014~BANK3
CYUSB3014~BANK2
CYUSB3014~BANK1
PMODEs usable as GPIO after boot
100uF X5R 4V
4.7uF 6.3V X5R
0.47uF
0.1uF
1.8V:1
1.8V_FX3:1

Receive

U802 BD3150L50100A00 — 3000–6000 — 1:2
U801 SKY13317-373LF
AD9361-RX U2
U808 BD3150L50100A00 — 1:2
U810 SKY13317-373LF
RX1 — U800 — C800 470pF
rx_bandsel_a R822 1K
rx_bandsel_c R823 1K
rx_bandsel_b R824 1K
C830 470pF, C838 470pF, C858 470pF
C804 10pF, C802 470pF, C801 100pF
C880 10pF, C881 10pF
T800 1600–4000 1:1
T801 70–2200 1:1
C805 100pF, C806 470pF
C882 10pF, C883 10pF
T802 1:1, T803 1:1
C818 100pF, C821 470pF
C823 100pF, C820, C824 470pF 10pF
R831 1K rx_bandsel_b
R832 1K rx_bandsel_c
R833 1K rx_bandsel_a
C865 470pF, C866 470pF, C867 470pF
C831 470pF — U813 — RX2

3.3V:1 — R800 150 — LED800 — RX1 active LED — Q800
3.3V:1 — R801 150 — LED801 — TX1 mode LED — Q801
3.3V:1 — R802 150 — Q802
LED_TXRX1_RX
LED_TXRX1_TX
LED_RX1
R803 10K, R804 10K, R805 10K

C847 DNP, C849 DNP
U805 SKY13335-381LF
TX1 — C810 220pF — TXRX1 — C809 470pF — SFDX1_TX 1K R825 — SRX1_TX 1K R826 — C859 470pF — C860 470pF
J800 5432 142-0701-871

TXRX1
TXRX2

C852 DNP, C855 DNP
J801 142-0701-871
SKY13335-381LF U811
C826 470pF — RFC — OUT1 TXRX2 — OUT2 — C832 220pF TX2 — PAD VCTL1 R834 1K SRX2_TX — GND VCTL2 R836 1K SFDX2_TX — C869 470pF — C871 470pF
C834 470pF

3.3V:1 — R810 150 — LED802 — TX2 mode LED — Q804
3.3V:1 — R811 150 — Q805
3.3V:1 — R812 150 — LED803 — RX2 active LED — Q806
LED_TXRX2_RX
LED_TXRX2_TX
LED_RX2
R813 10K, R816 10K, R817 10K

RX1
U807SKY13335-381LF
C812 470pF — RFC — OUT1 — C819 470pF — OUT2
PAD VCTL1 R829 1K SFDX1_RX
GND VCTL2 R830 1K SRX1_RX
C861 470pF, C862 470pF
C848 DNP, C851 DNP
J802 5432 142-0701-871

RX1

RX2
J803 142-0701-871
SKY13335-381LFU814
C829 470pF — RFC — OUT1 — C833 470pF — RX2 — OUT2
SRX2_RX R835 1K — VCTL1 PAD
SFDX2_RX R837 1K — VCTL2 GND
C868 470pF, C870 470pF
C854 DNP, C856 DNP

SFDX1 | Result
0 | RX only on TXRX1 ant
1 | Full duplex operation

Transmit

U809 BD3150L50100A00 — 1:2
U815 BD3150L50100A00 — 1:2
U816 SKY13335-381LF
AD9361-TX U2
C890 1000pF, C825 1000pF, C822 10uF X5R 4V
L804 100nH, L805 100nH, R814 680, R815 680
L806 15nH, L807 15nH
C827 220pF, C828 220pF, C817 10pF, C884 10uF X5R 4V
T804 1:1
C835 1000pF, C891 1000pF, C836 10uF X5R 4V
R820 680, R821 680
L808 100nH, L809 100nH
L810 15nH, L811 15nH
C839 220pF, C841 220pF, C842 10pF, C885 10uF X5R 4V
T805 1:1

1.3V_TX:1
3.3V_TXAMP2:1

TX1 — SOT89 — U804 PGA-102+ — L801 15nH — R808 680 — L800 100nH — C807 0.01uF — C808 1000pF
C811 220pF — C816 22pF
tx_bandsel_a R827 1K
tx_bandsel_b R828 1K
C863 470pF, C864 470pF

TX2 — SOT89 — U817 PGA-102+ — L815 15nH — R809 680 — L814 100nH — C845 1000pF — C846 0.01uF
C843 22pF — C844 220pF
R838 1K tx_bandsel_b
R839 1K tx_bandsel_a
C872 470pF, C873 470pF

3.3V:1 — L802 2.2uH — C813 4.7uF 6.3V X5R — Q803 ZXTC2062E6 — R807 10K tx_enable1 — R806 1K
3.3V_TXAMP1:1

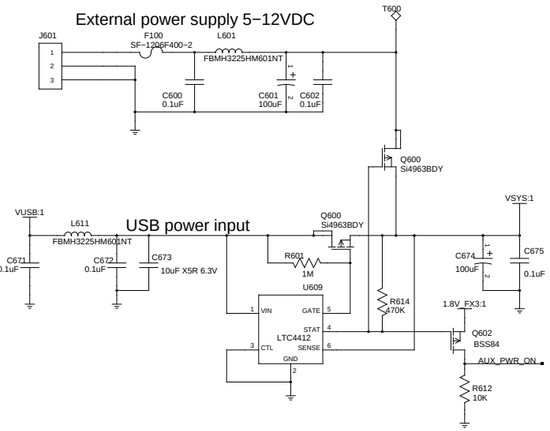
3.3V:1 — L812 2.2uH — C837 4.7uF 6.3V X5R — C840 4.7uF 6.3V X5R

3.3V:1 — L816 2.2uH — C857 4.7uF 6.3V X5R — Q807 ZXTC2062E6 — R818 10K tx_enable2 — R819 1K
3.3V_TXAMP2:1

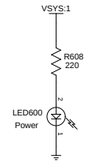
TX amp power

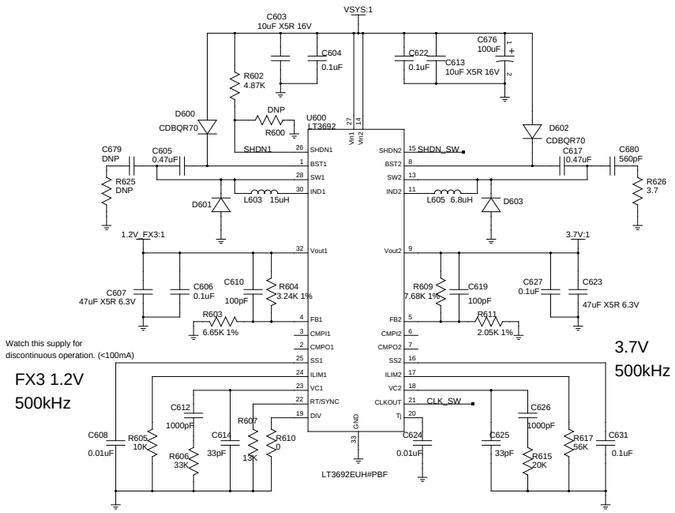
TITLE	B200 RF Interface
FILE: rf.sch	REVISION: 2
PAGE 8 OF 8	DRAWN BY: nick, matt

External power supply 5−12VDC



USB power input

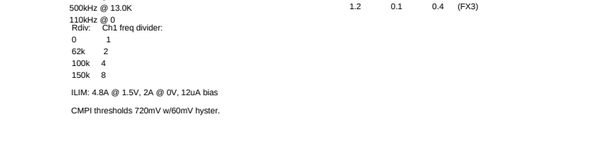




Watch this supply for discontinuous operation. (<100mA)

FX3 1.2V 500kHz

3.7V 500kHz



0.806V Vfb

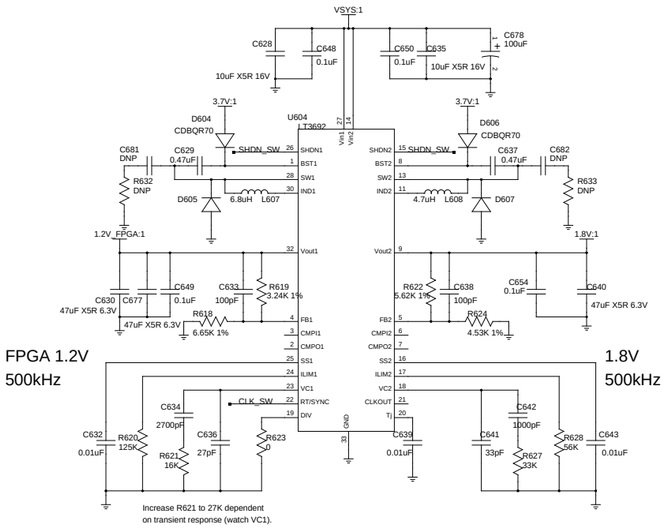
RT: 2.5MHz @ 950mV, 110kHz @ 0V, 12uA bias
1.5MHz @ 44.2K
1.0MHz @ 28.0K
500kHz @ 13.0K
110kHz @ 0

Rdiv:	Ch1 freq divider:
0	1
62k	2
100k	4
150k	8

ILIM: 4.8A @ 1.5V, 2A @ 0V, 12uA bias

CMPI thresholds 720mV w/60mV hyster.

Vout	Imin	Imax	
3.7	0.2	0.7	
1.8	0.6	1.5	
1.2	0.25	3.5	(FPGA)
1.2	0.1	0.4	(FX3)

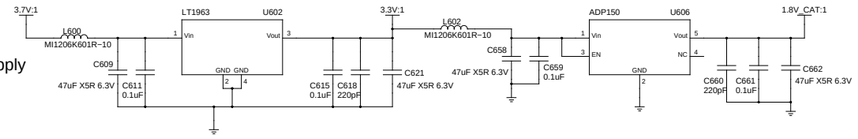


FPGA 1.2V 500kHz

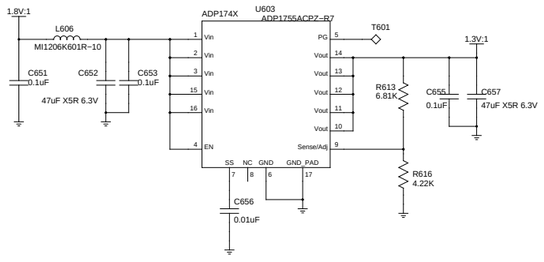
1.8V 500kHz

Increase R621 to 27K dependent on transient response (watch VC1).

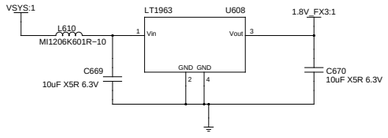
3.3V digital/TX amp supply



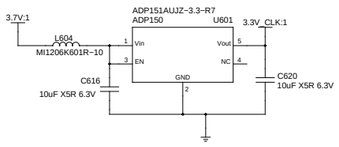
1.3V Catalina supply



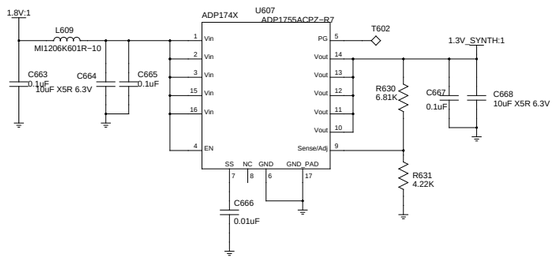
FX3 1.8V supply
For clocks, I/O

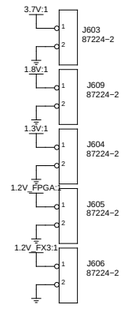


3.3V oscillator/clock supply



1.3V Catalina synth supply





TITLE	B200 Power
FILE: power.sch	REVISION: 2
PAGE 7 OF 8	DRAWN BY: nick, matt