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TECHNICAL DESCRIPTION: BASEBAND AND AUDIO CIRCUITS ON THE TRANSCEIVER BOARD

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1**GENERAL**

This document describes the baseband and the audio processing circuits, which are part of the transceiver board mounted in different digital pocket phones of GSM type.

The other part of the transceiver board that carries the radio circuits is described in the corresponding document starting with 1/1551 -.

One purpose of the baseband part is to control and monitor transmission and reception, to co-operate with the telephone exchanges of the mobile telephone system and to do the processing of audio signals to and from the mobile phone.

Chapter 2 contains information about document revisions.

In chapter 3 the data flow through the phone is described in both TX and RX direction.

In chapter 4 are several of the electrical functions and circuits described more in detail.

Chapter 5 describes the different memory types used in the phone.

In chapter 6 the layer structure of the PCB is briefly described.

1.1**Cross References****1.1.1****Names**

In most cases the different circuits in the phone are given names which are used during the development phase. These names are also used in this description.

The following list shows the used circuit names and the corresponding position numbers used in the schematics.

HERTA	N660
IRMA B	D900
IRMA FLASH	D910
MARTHA	D600
MARTHA FLASH	D610
VICTORIA 2+	N800



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1.1.2**Abbreviations**

Some common abbreviations are used in the text. These are explained below.

A/D	Analogue/Digital
CUI	Command User Interface
D/A	Digital/Analogue
DSP	Digital Signal Processor
HW	Hardware
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MS	Mobile Station
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
RTC	Real Time Clock
RX	Receive
SIM	Subscriber Identity Module
TAE	Terminal Adapter Equipment
TX	Transmit

2**CHANGES BETWEEN REVISIONS**

Rev A - the first revision.



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3

DATA FLOW

A general block diagram for the GSM phone is shown in the figure below. It shows the audio-data flow through the GSM phone. It also indicates the different hardware parts involved in the transmission.

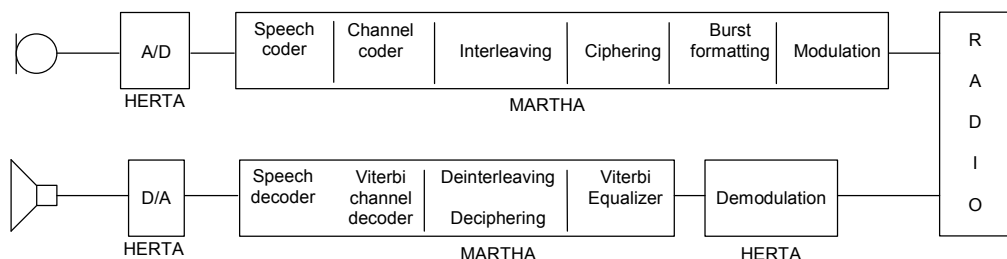


Figure 1 Block diagram for GSM phone.

All names below the boxes in figure 1 correspond to the actual circuit that performs the indicated task.

MARTHA controls the data flow. This is the central unit containing the AVR microprocessor, DSP, internal RAM and the interfaces to external circuits and units, external memories and the radio. It also performs a lot of the signal processing not done in the other circuits.

3.1

TX path

The speech signal from the microphone is amplified and digitized to a 16 bit-PCM signal in HERTA. It is then sliced into 20 ms pieces and thereafter speech coded in DSP to reduce the bit rate. Further data processing is carried out in MARTHA that includes channel coding, interleaving, ciphering and burst formatting. The data is then put through a wave form generator (IQ signal) before it is fed to the radio.

The interleaving causes a small delay. Ciphering is done with a relationship of 1:1 (input:output) and then the bits are formatted into eight half bursts (for every 20 ms of speech). These are then transmitted in the proper time slot at a rate of about 270 kbit/s.



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3.2 RX path

The receiver path works as follows. The signals IRA, IRB, QRA and QRB from the radio are hard limited phase modulated and differential signals that contain all the data received. A fast phase digitizer in HERTA demodulates these signals. The phase information is then fed to MARTHA.

The bursts received are then further processed in MARTHA mainly in the same way as in the TX path but in reversed order and with reversed functions, that is deciphering, deinterleaving and channel decoding.

The first step in MARTHA is however an equalizer that performs a Viterbi algorithm to create a channel model.

After all eight half bursts have been received and deciphered, they are reassembled into a 456 bit message. The sequence is decoded to detect and correct errors during the transmission. The decoder uses soft information (probability that a bit is true) from the equalizer to improve error correction.

Finally the bit stream is speech decoded in the DSP and then transformed back into analogue speech in HERTA.

3.3 TAE CIRCUITS

The TAE circuits handle the data communication related support. This means that it handles IrDA, RS232/USB cable interface and Bluetooth.

The IRMA B circuit provides an ARM processor, internal RAM, Bluetooth baseband controller, three UART blocks, four FIFOs, IrDA interface, interrupt controller, timers, watchdog and auto-baud functionality.

IRMA B uses one of the two clock outputs from MARTHA. The clock request system is entirely implemented in hardware in both IRMA B and MARTHA. IRMA B requests clock by setting SYSCLKEN high and the clock is stopped when IRMA B sets SYSCLKEN low. The clock is also supplied to the RAN BT radio circuit.

IRMA B communicates with MARTHA via a serial channel (IRMA B UART1 and MARTHA UART2). The second UART, UART2, is used for the IrDA and RS-232/USB cable communication. The third UART, UART3 is used for debug output and is only connected to testpoints.

The memories are connected to IRMA B as described in the memory section.

The IrDA logic consists of an IrDA compatible transceiver unit with its own regulator, powered from the VBAT supply. One I/O pin on IRMA B (UART2_IO1) is used to turn the regulator on which in turn turns on the IR current drive.

The cable interface is connected to UART2. It is the same UART block that handles IrDA and cable, but there is a switch inside IRMA B that can be set to



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select between the two serial ports. Also involved in the data cable interface are the two RS232 standard handshake signals CTS/RTS. There is a cable detect function inside IRMA B which requests clock and issues an interrupt when the UART2 receive signal has been high for a certain period of time. The time is programmable and up to 100ms.

The Bluetooth baseband controller can be set to wake up when the signal MCLWAKEUP from Martha goes high. This can be used to let MARTHA synchronise the GSM and Bluetooth paging periods. When MCLWAKEUP goes high only the Bluetooth block is running and the rest of IRMA B can be left in deepsleep to reduce the current consumption.

4 DESCRIPTION OF VARIOUS FUNCTIONS

4.1 ON/OFF circuitry

4.1.1 ON/OFF button

As long as the phone is turned off the enable inputs of VICTORIA 2+ are kept at high level by internal pull up resistors to VBATT. When the ON/OFF button is pressed, the signal ONSWa is connected to ground. This will cause VICTORIA 2+ to check the VBATT level. If VBATT is within limits VICTORIA 2+ will power up the buck regulator, the linear regulators and the serial interface. By doing this, the rest of the phone is powered up.

One of the first things the CPU has to do at power up is to set the regulators that shall be powered up. Sending a command from MARTHA to VICTORIA 2+ on the I²C interface does this. When this is done, the ON/OFF button can be released.

Pressing the ON/OFF button again turns off the MS, which will connect ONSWa to ground. This will not affect VICTORIA 2+ since the software in the phone will set VICTORIA 2+ to mask interrupts from ONSWa on the IRQ signal. The ONSWa signal is also linked a port input on Martha through a diode. MARTHA senses the signal and the program can turn off the regulators inside VICTORIA 2+ by using the serial I²C interface.



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4.1.2 **ONSRQ signal**

The phone can also be started from the system connector by pulling the CTS_ON signal to low level. This signal is connected to the ONSWb pin on VICTORIA 2+. When ONSWb is pulled to low level, VICTORIA 2+ will check the VBATT level and power up the regulators in the same way as when starting the phone with the ON/OFF button.

4.1.3 **Auto Turn On**

The CPU will automatically switch on, if a charger is connected. VICTORIA 2+ will sense the voltage difference between DCIO and VBATT created by the connected charger. If VBATT is within limits VICTORIA 2+ will power up the regulators. If VBATT is too low, a current generator inside VICTORIA 2+ will charge the battery with a small current, and when VBATT reaches the lower limit the regulators will power-up.

4.1.4 **Alarm**

The phone is switched on at Alarm from the RTC. DCON will then be generated directly from the RTC block with no influence from the CPU, which in this state has no power. DCON is connected to ONSWc on MARTHA. At alarm, the ONSWc signal will go high and the phone will be powered up in the same way as described in section 4.1.1. ONSWc is active high.

4.2 **POWER SUPPLY**

There are two ways for the mobile to get power. If battery is used, which is the common way, it is fed through the battery connector on the PCB then linked through the PCB to VICTORIA 2+, which contains the regulators for the baseband and radio part. The other way is through the system connector. A battery must always be attached to get the phone powered up.

The VBATT line is switched through the P-FET that acts as switch for the DCIO voltage and also as charge switch. The switch is controlled by VICTORIA 2+.

The different voltages are:

VDIG 2.75V, is used for MARTHA baseband pads and for the mixed mode circuit HERTA, the Anna AMR DSP and the I/O for graphics controller S1D13711.

VCORE 1.8V, is used to supply the MARTHA core and the memories, S1D13711 core and the synthesizer ML2860.

VMCL 2.75V, is used for IRMA and IrDA-module.

VMCLCORE 1.8V, is an LP2985 and used to supply IRMA core IRMA flash.



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VALLL 1.8V, used for the analogue supply to the ML2860 synthesizer.

VAMP 5V, LM2750 step-up regulator, used to supply the LM4980 audio amplifier.

VAMRCORE 1.8V, an LP2985 supply for the core of a DSP to be used for E-OTD.

VIRCAM 2.8V, an LP2985 for the supply to the camera and IR LED.

VRTC is used to supply the RTC block in MARTHA. The regulator for this voltage is always powered up when a battery is connected and cannot be switched off.

SIMVCC is generated from VICTORIA 2+. 5V SIMVCC is generated from a DC/DC converter that steps up the VDIG voltage to 5V for the SIM interface. 3V SIMVCC is generated by an LDO in VICTORIA 2+.

VBATT is the unregulated battery voltage.

An error flag output, PWRRST, which gives a low output voltage warning due to low battery voltage is generated by VICTORIA 2+. When VICTORIA 2+ detects a VBATT level out of limits, the signal PWRRST goes low. This will cause a HW reset to MARTHA. VICTORIA 2+ will turn off the regulators and power down the MS.

The signal PWRRST is also, as the name may indicate, the power reset to MARTHA at power up. PWRRST will be set to high, when the voltages from the regulators inside VICTORIA 2+ have stabilized.

4.3 AUDIO

Most of the audio processing is made in HERTA by the voice codec that converts between analogue speech signals and 16 bit linear PCM code in both RX and TX paths. HERTA also includes audio filters and amplifiers for microphone and earphone.

The microphone is connected differentially to HERTA. It is biased by a reference signal, CCO, from HERTA, which is properly filtered on the circuit board and inside HERTA. In the microphone path is also a high pass filter designed in that will cut frequencies below approximately 300 Hz.

HERTA communicates with MARTHA by means of the I²C interface. Settings, readings from the general purpose A/D converter, and control of HERTA are made on this interface. Data from A/D converter and phase digitizer is received on the signals QDAT and IDATA. Data to the D/A converter are sent from MARTHA on the DAC-signals.



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4.4 POLYPHONIC RING SIGNALS

Polyphonic ring signals are generated in a synthesiser, ML 2860 from OKI. This is a 32-voices midi synthesiser that is used for playing G-MIDI files. The clock to the synth is the 13MHz CLKOUT from Martha.

The synth is memory mapped and uses the data bus, the RAMCS signal and the ordinary WEn and OEn. The synth is power up and down using data commands.

The SYNT_IRQ signal tells Martha that the file that has been downloaded to the synth has almost finished playing and that the synth is ready for a new download.

The output from the synth is hooked up to speaker output of Herta to be played through the speaker. To be able to play polyphonic ring signals in the PHF the audio output to the PHF from Herta goes through the mixer part of the synth and is mixed in with the output of the synth.

4.5 RED INDICATOR

The red LED is controlled by MARTHA by sending I²C commands to VICTORIA 2+ that is connected directly to the LED. When the battery voltage is too low to power up the phone VICTORIA 2+ enters tricle charge mode when a charger is connected and turns on the red LED without involving MARTHA.

4.6 KEYBOARD SCANNING

The keyboard scanning is performed by 9 signals connected to the PORT block in MARTHA; KEYCOL 0-3 (open drain outputs) and KEYROW 0-4 (CMOS inputs with internal pull-ups). These signals are arranged in a matrix, each cross point can provide the functionality of one key button. In standby, when no scanning is performed, all the outputs are held low and all inputs are at high level due to the pull-ups.

Whenever a user presses any of the keys or moves the joystick, one of the inputs goes low. The software starts the key scanning procedure to determine which cross point was activated.

The maximum number of keys in a 4*5 matrix is 20. However it is possible to add more keys by connecting each of the inputs to ground.

4.7 KEYBOARD AND DISPLAY ILLUMINATION

The keyboard and the display are illuminated by LEDs. There are eight white LEDs for the keyboard and two white LEDs for the display. The keyboard LEDs are driven from a port on MARTHA through a transistor. The current through the LEDs are regulated to give a stable output. The display LEDs are driven from a switch capacitor circuit, LM2793 from National. This is



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controlled by a DAC signal from HERTA to adjust the brightness. The two white LEDs are built into the display package.

4.8 LCD CONTROLLER

The LCD is controlled by a graphics controller, S1D13711 from Epson. This is clocked by CLKOUT and also acts as a memory controller and camera interface.

4.9 E-OTD PROCESSOR

An external DSP takes care of the E-OTD if this is to be implemented.

4.10 REAL TIME CLOCK

The real time clock is a part of the MARTHA chip. A 32.768 kHz crystal is placed close to the inputs on MARTHA. A separate voltage, VRTC, which is generated by a regulator in VICTORIA 2+, powers the RTC block in MARTHA.

The RTC is always powered as long as the main battery is connected. On the output of the regulator is a backup capacitor connected. This capacitor will give power enough to keep the RTC alive at least 2 minutes after the main battery has been disconnected. The backup capacitor is a coin type rated 2.5V and 70mF.

4.11 IRDA-MODULE

4.11.1 Block diagram

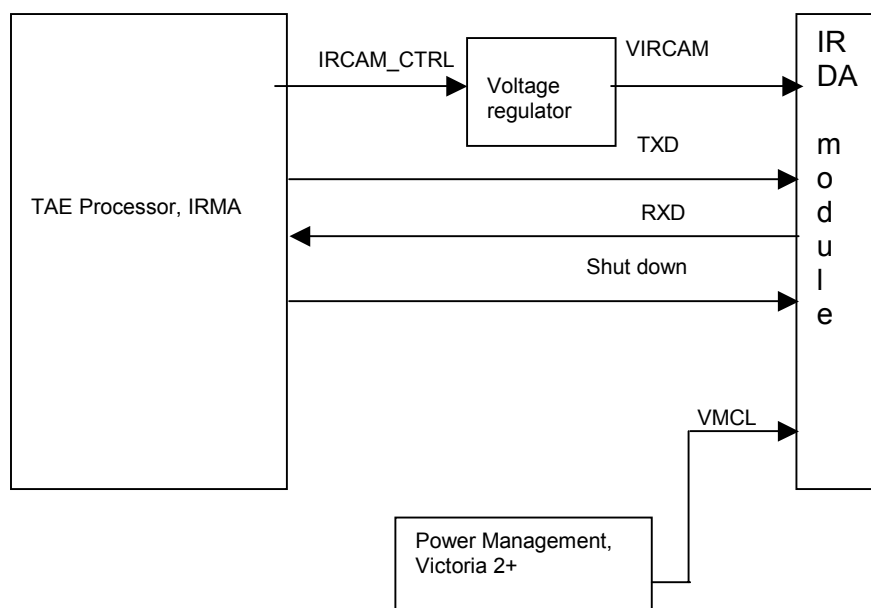


Fig.3

An overview of the IRDA block.



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The block is composed of Power Supply, Communication and Control signals.

4.11.2 Power supply

Two separate voltages power the IRDA module, the VIRCAM that powers the Infrared LED and the VMCL that powers the internal logic. The VIRCAM is a 2.8V regulated voltage from an external voltage regulator.

The IR current pulses are about 320mA for duration of 1.62us at 115.2kbps data rate. The current is drawn from the regulator, which is a 150mA low dropout voltage regulator. The regulator is still able to deliver the 320mA since it has a short circuit current of 450mA for some seconds.

There are two control signals from IRMA to the IR module interface, the IRCAM_CTRL and the Shut Down signals.

The IRCAM_CTRL signal is used to switch the voltage regulator to enable/disable current flow to the IRLED.

The Shut Down signal is used to cut the current consumption of the module to typically 10nA. The shut down mode disables the transmitter input and tri-states the receiver output with typical 500kΩ pull-up.

5 MEMORIES

Two different memories are used on the transceiver board. They are flash memories, one with two stacked flashes and one with stacked SRAM.

5.1 MEMORY CONFIGURATION

5.1.1 MARTHA memory

MARTHA FLASH memory holds the signalling software and non-volatile parameters.

The MARTHA FLASH is a stacked flash memory with one 64 MBit and one 32 MBit in the same package. It is organized as 4096x16 and 2058x16 respectively. Each memory is divided into separately erasable blocks.

A part of the memory is used as an emulated EEPROM area, this is called the NVM (Non Volatile Memory) area.

The MARTHA FLASH memory is connected to the common address and data bus. For control, the signals WEn, OEn and ROMCSn are used.

Communicating with the internal CUI performs program and erase operation. An internal write state-machine automatically executes the algorithms and timings necessary for program and erase operations.



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The VPPFLASH is connected to pin VPP on the device. To speed up the erase and programming time 12V can be applied to this pin. However this is not necessary.

5.1.2 **IRMA FLASH**

This memory is a flash memory with a SRAM stacked on top of the flash chip, all mounted in the same package. The flash is organized as 2048k*16 and the SRAM as 256k*16. This SRAM is used for temporary data storage during execution. No program code can be executed in this memory.

The SRAM memory is connected to the common address and data bus. For control, the signals WEn, OEn and RAMCSn are used.

5.1.3 **Programming**

The flash memories enables on board programming. The erasing and programming of the flash is then completely software controlled. The software communicates with external equipment through a serial link. During erasing and programming the software runs in RAM.

To decrease the programming time VPP 12V can be supplied. VPP is applied to the system connector on the terminal VPPFLASH. This pin is also used to disable the watchdog function in MARTHA.

The procedure to load a program for the first time in the production line is as follows:

When the phone is powered up and the signal PWRRST is released the software starts to read the first instruction in the flash memory (after a short delay). Now, if the SERVICEI signal is activated, the very first instruction is read from an internal ROM in MARTHA. This is a small ROM containing a very simple "boot strap loader". The purpose of this code is to listen to a specific code on the serial link, CTMS. This indicates that the user wishes to download a program called the "hexloader" to the RAM. If this code is not received within 2 seconds the execution is automatically switched over to continue in the MARTHA FLASH.

If the "hexloader" is successfully loaded into RAM the execution starts in RAM. With help of the "hexloader" it is now possible to execute the algorithm to download and program any code received on CTMS. It is also possible to erase the FLASH or to read the manufactures device code of that particular flash memory.

6 **PRINTED CIRCUIT BOARD**

The printed circuit board is an 8-layer board. The layers 3, 4 and 5 carry mosat of the power supply voltages.



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The layer structure is listed below:

Layer 1	Components, baseband signals (Primary side)
Layer 2	Baseband signals
Layer 3	Baseband signals
Layer 4	Baseband signals
Layer 5	Baseband signals
Layer 6	Ground
Layer 7	Baseband signals
Layer 8	Components, baseband signals (Secondary side)