Version change history

version number	date	description
V0.2	2013 year 1 month 25 day	EG8030 Data Sheet internal test version. This version is for internal use test!

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EG8030 Chip Data Sheet

1. Feature

- Single 5V supply
- External 16MHz crystal oscillator
- Pin Configuration four operating modes
  - Open loop phase synchronous regulator
  - Three-phase synchronous closed loop regulator
  - Three-phase independent open-loop regulator
  - Independent closed loop three-phase voltage regulator
- Voltage, current, temperature feedback real-time processing
- Overvoltage, undervoltage, overcurrent, short circuit, an overheat protection function
- 3S soft-start pins
- Phase sequence inversion function
- Phase clear function
- The way status indication LED and buzzer alarm
- Roadbed along a sinusoidal frequency output and the analog signal output
- All the way fan control output
- Pins provided two kinds of three-phase pure sine wave output frequency:
  - Pure sine wave 50Hz fixed frequency
  - Pure sine wave 60Hz fixed frequency
- PWM carrier frequency can be set
  - Carrier frequency 20KHz
  - Carrier frequency 10KHz
  - 5 KHz carrier frequency
  - 2.5KHz carrier frequency
- Comes with dead-time control pin is set four kinds of dead time:
  - 300nS dead time
  - 500nS dead time
  - 1.0uS dead time
  - 2.0uS dead time
- Modify the functions or parameters according to the customer applications provided by Yi Microelectronics

2. description

EG8030 is a digital, full-featured four kinds of work that comes with dead-time control of three-phase pure sine wave inverter generator chip, configurable Operation mode can be applied to DC-DC-AC two-stage power conversion architecture, or a single-stage DC-AC step-up transformer frequency transform architecture. External 16MHz crystal oscillator Device, can produce high precision, very small harmonic distortion and phase signal SPWM. And have the perfect sampling mechanism, capable of acquiring a current signal, temperature Of the signal, a phase voltage signal, the implementation process, and to realize the protection function, output voltage regulation. Chip using CMOS technology, the internal integration SPWM Sine generator, dead time control circuit, the amplitude of the multiplier factor, a soft start circuit.

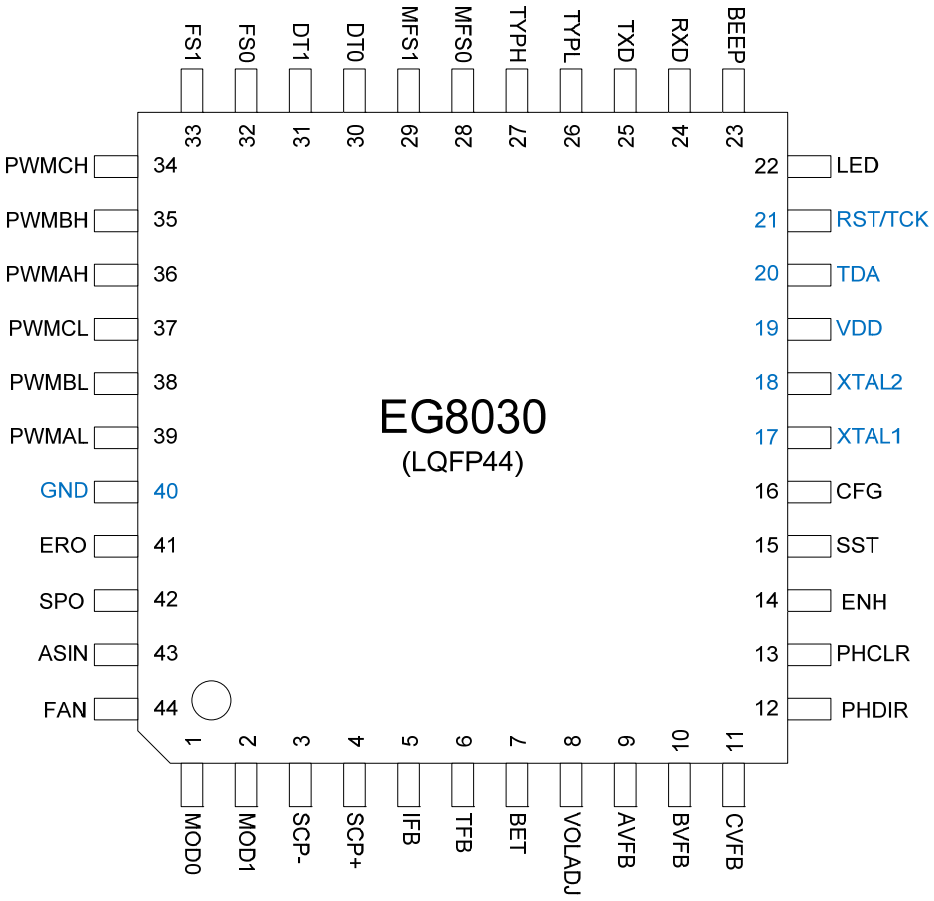
3. Applications

- Three-phase pure sine wave inverter

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4. Pin

4.1. Pin definitions



Map 4-1. EG8030 Pin definitions

Description:

1 , All chip configuration pins (DI) Are weak pull-up input port, an internal pull-up resistor value 30K [Omega], in the case of external pins floating,

The pin is high, i.e., the chip read word configuration " 1 "; If you need to configure" 0 "Can lead directly to ground.

2 , Chip feedback signal input pin (AI) Analog signal input port, a high-impedance mode, the external floating pin is undefined, the chip

ADC Read AD Value is undefined.

3 , All chip digital output pin (DO) Are push-pull output port, pull current capability 5mA , Sink current capability 20mA .

4 , Chip signal output sine wave (AO) Pin is the analog signal output port, to use only a small signal, no current capability.

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4.2. Pin Description

Pin Number	Pin Name	Port mode	description
1	MOD0	DI	MOD1, MOD0 operation mode is set in the three-phase inverter, "11" is a three-phase synchronous regulator open loop mode, i.e. to provide an analog signal for controlling the three-phase modulation depth SPWM by external VOLADJ foot, 0-5V 0% -100% can be set modulation depth; "10" is a three- phase synchronous loop regulator mode, the chip collecting three-phase output voltage phase, the PI regulation, modulation depth is calculated automatically, then the output is three-phase synchronous output, three-phase SPWM modulation depth that is the same; "01" is a three-phase independent open loop the pressure regulating mode, i.e. by AVFB \ BVFB \ CVFB external analog signals sampled three groups, independently controlling the depth of modulation of ABC three-phase; "00" is a three-phase independent closed loop mode regulation, the three-phase output voltage feedback directly to the treated AVFB \ BVFB \ CVFB pin chip PI regulator, are determined independently of ABC three-phase modulation depth. **Note: Modulation depth This is the maximum amplitude of the modulated carrier wave maximum amplitude and the minimum** amplitude and a ratio, expressed as a percentage of the difference between the minimum amplitude. The inverter, the DC bus at the same load and input conditions, the depth of amplitude modulation of the output sine wave SPWM substantially proportional relationship.
2	MOD1	DI	
3	NC	AI	Retention
4	NC	AI	Retention
5	I FB	AI	Load current feedback input
6	T FB	AI	Temperature feedback input
7	BET	AI	Battery voltage monitoring port, the overvoltage and undervoltage protection
8	FRQADJ	AI	Phase sine wave voltage feedback threshold, as a three-phase synchronous terminal regulator
9	V FB A	AI	A phase sine wave output voltage feedback input terminal
10	V FB B	AI	B-phase sine wave output voltage feedback input terminal
11	V FB C	AI	C-phase sine wave output voltage feedback input terminal
12	PHDIR	DI	Reverse phase sequence control pin "0" is set for the three-phase output phase sequence current ACB "1" to set the current three-phase output phase sequence ABC
13	PHCLR	DI	Clear port phase sequence, the falling edge of the trigger signal, the phase of A sinusoidal phase was adjusted to 0 °
14	ENH	DI	SPWM three-phase output enable pin "0" to close the three-phase signal SPWM outputs "1" on the three-phase output signal SPWM
15	SST	DI	Soft-start pin is set to "0" Soft starter off "1" soft start for 3 seconds each time you restart SPWM output, linearly increasing the amplitude of the sine wave period.
16	CFG	DI	SPWM configuration options Pin EG8030 SPWM output frequency of the modulation frequency, the size of the dead zone, the output level, the operation mode, soft start, three-phase sequence in two configurations, usually single chip while the external pin configuration work, by setting the FS \ MFS \ DT \ TYP \ MOD \ SST \ PHDIR foot implemented; when using serial communication, the pin can be provided to select the internal configuration registers, on the internal serial communication registers and setting, see **** "0" to select the internal configuration registers, used for selection of the external pin configuration, the chip work independently "1" when the serial communication

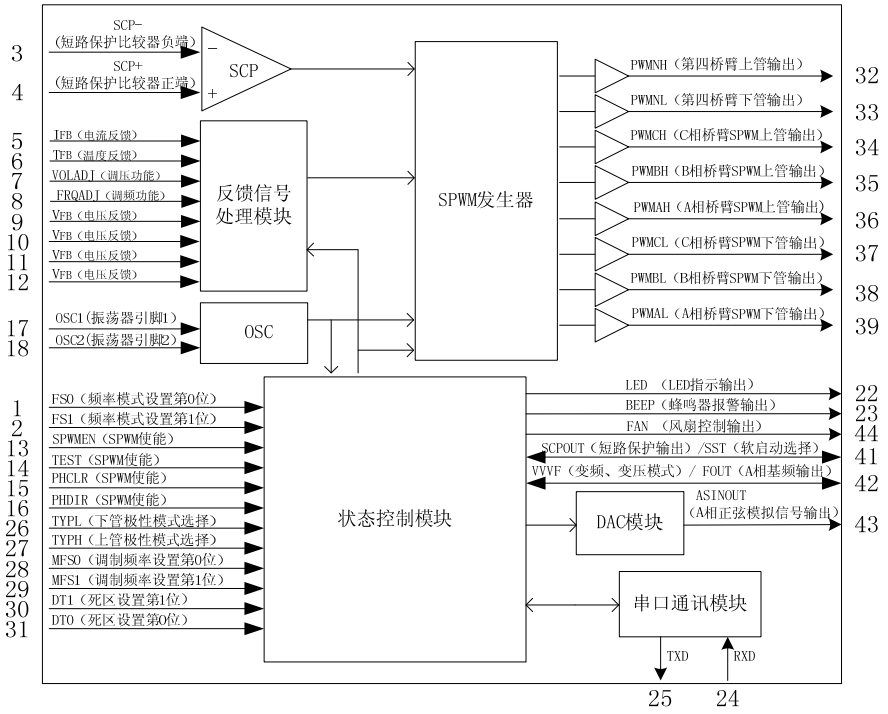
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Pin Number	Pin Name	Port mode	description
17	XTAL1		16M crystal oscillator input pin 1, a 22pF capacitor must be connected to ground
18	XTAL2		16M crystal oscillator input pin 2, a 22pF capacitor must be connected to ground
19	VCC	VCC	+ 5V working power supply terminal of the chip
20 , twenty one	NC		**Retention pin system, must be left open!**
twenty two	led	DO	External LED alarm output, outputs a low level "0" when a failure occurs normally lit LED: long bright OFF: 1 flicker, off for 2 seconds, the cycle has been Overcurrent: flicker 2, 2 seconds off, until the cycle; Brown: 4 under flashing off for 2 seconds, the cycle has been Overvoltage: blinking 3, 2 seconds off, until the cycle; overtemperature: 5 under flashing, off 2 second, has been circulating
twenty three	BEEP	DO	Buzzer alarm function: Normal: do not call Shutdown: call at 1, 2 seconds, until the cycle; Overcurrent: the name 2, 2 seconds, has cycles; overtemperature: 5 under the name,, 2 seconds, has cycles; Overvoltage: 3 under the name,, 2 seconds, has cycles; Brown: called 4, the stop 2 seconds, has cycles;
twenty four	RXD	DI	Serial communication function pin, 2400 baud, 8 data bits, 1 stop bit, no parity CFG pin is often necessary to use
25	TXD	DO	serial communication configuration is "0"
26	TYPH	DI	TYPH, TYPL is the PWM, the output type selected tube "00" is the low output power tube open tube, open at low output power Tubing; "01" is the low output power tube open tube, open at high output power Tubing; "10 "is the output high power tube open tube, the tube power output low open tube;" 11 "is open tube output high power tube, open output high power tube down tube; **Design in Application typical application circuit, according to the driving state of the pin means arranged reasonably, otherwise cause inconsistencies on a power MOS transistor is turned on while the phenomenon**
27	TYPL	DI	
28	MFS0	DI	MFS1, MFS0 output is provided SPWM modulation frequency wave "00" is the modulation frequency 2.5KHz output; "01" is output 5KHz modulation frequency; "10" is output 10KHz modulation frequency; "11" is output 20KHz modulation frequency;
29	MFS1	DI	
30	DT0	DI	DT1, DT0 is disposed on the PWM output, the dead time MOS transistor: "00" is 1.5uS dead time; "01" is 1.0uS dead time; "10" is 0.5uS dead time; "11" is 0.3uS dead time
31	DT1	DI	
32	FS1	DI	Output sine wave frequency setting pin "00" reservations "01" reservations "10", to output sine wave frequency is 60Hz "11" to set the output frequency of 50Hz sine wave
33	FS0	DI	
34	SPWMCH	DO	C-phase output bridge arm tube SPWM
35	SPWMBH	DO	B-phase output bridge arm tube SPWM
36	SPWMAH	DO	A phase output bridge arm tube SPWM

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Pin Number	Pin Name	Port mode	description
37	SPWMCL	DO	The C-phase output SPWM tube arm
37	SPWMCL	DO	The C-phase output SPWM tube arm
38	SPWMBL	DO	The B-phase output SPWM tube arm
39	SPWMAL	DO	A tube SPWM output lower phase arm
40	GND	GND	Chip ground terminal
41	ERO	DO	Fault signal output pin "0" normal operation outputs "1" when the chip is protected output off state
42	SPO	DO	Output pin voltage sampling Outputs a high level voltage during the sampling, not sampled low
43	ASIN	AO	An analog sine wave signal output pin A frequency and phase output are the same and the A-phase sine wave signal SPWM, see voltage feedback 9.1
44	FANCTR	DO	External fan control, when T FB Pin is detected when the temperature is higher than 45 ℃, outputs a high level "1" so that the fan is running, when the temperature falls below 40 ℃, it outputs a low level "0" stops the fan

5. Structure diagram

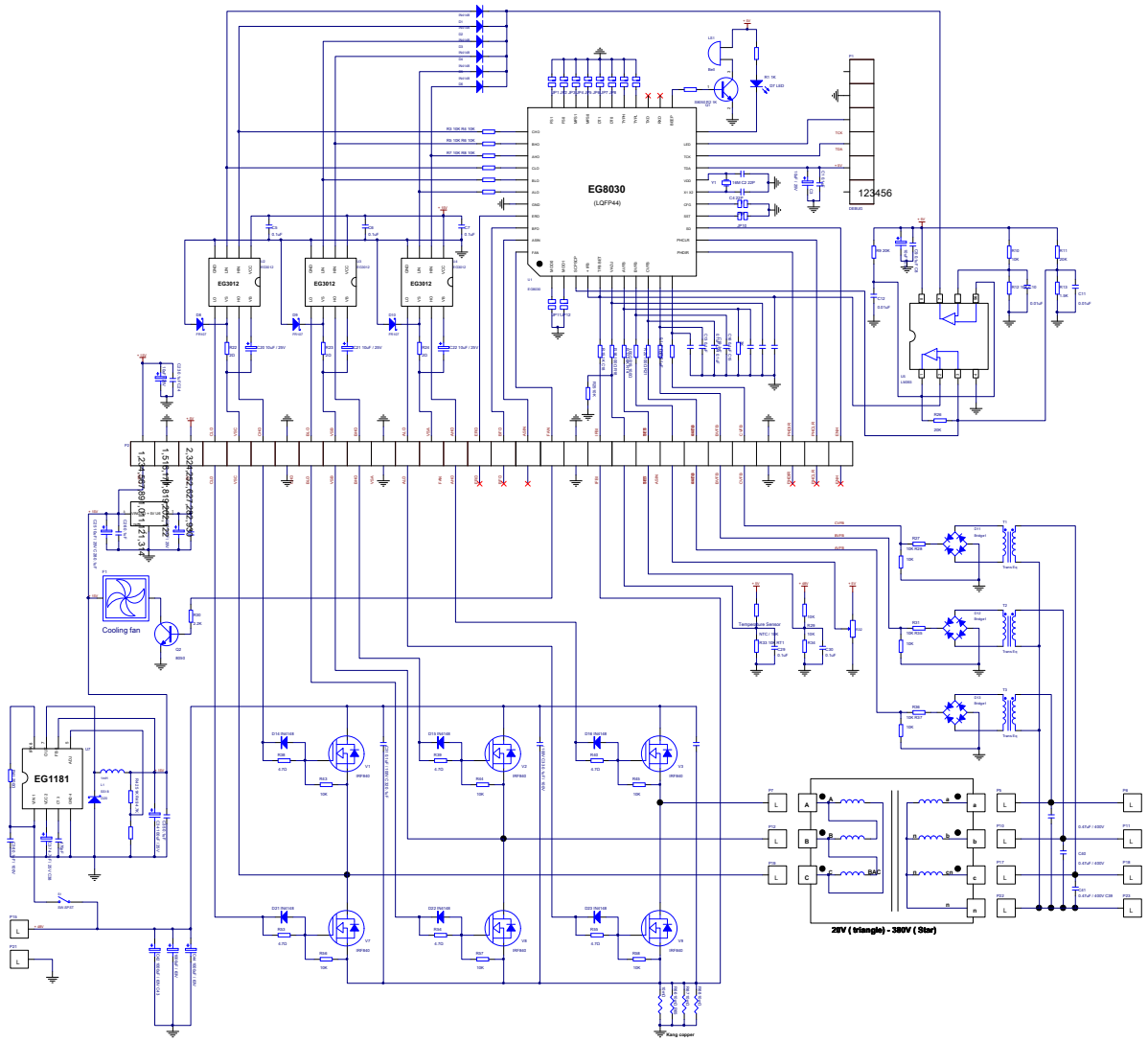


Map 5-1. EG8030 Structure diagram

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6. Typical application circuit

6.1 Regulators phase synchronous loop mode - DC-AC-AC Frequency transformer Δ- Y Boost structure (recommended)



EG8030 + EG3012 + EG1181 Application of the three-phase circuit diagram of a typical pure sine wave inverter

This application uses 48V Battery power for the DC bus to EG8030 An inverter control unit, through a half-bridge driver chip EG3012 Driving power MOSFET , A three-phase three-phase full-bridge inverter output SPWM After the three-phase step-up transformer working frequency filtering. Three-phase frequency step-up transformer employed Δ- Y Connection, four-wire output phase voltage 220V , Line voltage 380V Pure sine wave of three-phase power. Required board + 15V Drive power using DC-DC Step-down switching power supply chip EG1181 get on 48V Buck converter. This application EG8030 Work-phase synchronous loop mode regulator, the feedback voltage transformer isolation uses three small samples. Because it is synchronous regulation, the three-phase SPWM Modulation depth of the same, when the unbalanced load, there will be some phase voltage offset. EG8030 With voltage unbalance protection feature that limits the maximum voltage of each phase does not exceed a preset 10% , And when the three-phase voltage imbalance, will take off the protection. Synchronous mode is the closed loop regulator EG8030

The recommended mode of operation, is easy to realize high reliability.

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6.2 Three-phase independent closed loop mode regulation - HVDC inverter output line four-leg structure (test)

(Reserved)

Map 6-2. EG8030 + TLP250 Application of the three-phase circuit diagram of a typical pure sine wave inverter

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7. Electrical Characteristics

7.1 Limit parameters

Unless otherwise indicated, the T Under 25 ℃ A =

symbol	parameter name	Test Conditions	Minimum	Maximum	Unit
VCC	power supply	Vcc with respect to GND Voltage	-0.3	6.5	V
I / O	All input and output ports of all	I / O pins to GND Voltage	-0.3	5.5	V
Isink	The maximum output pins irrigation Electric current	-	-	25	mA
Isource	The maximum output of the pull pin Electric current	-	-	--5	mA
T A	Ambient temperature	-	- 45	85	℃
Tstr	Storage temperature	-	- 65	125	℃

Note: beyond the limits of the parameters listed may cause permanent damage to the chip, running for a long time in extreme conditions may affect reliability.

7.2 Typical parameters

Unless otherwise indicated, the T A = 25 ℃, Vcc = 5V, OSC = 12MHz

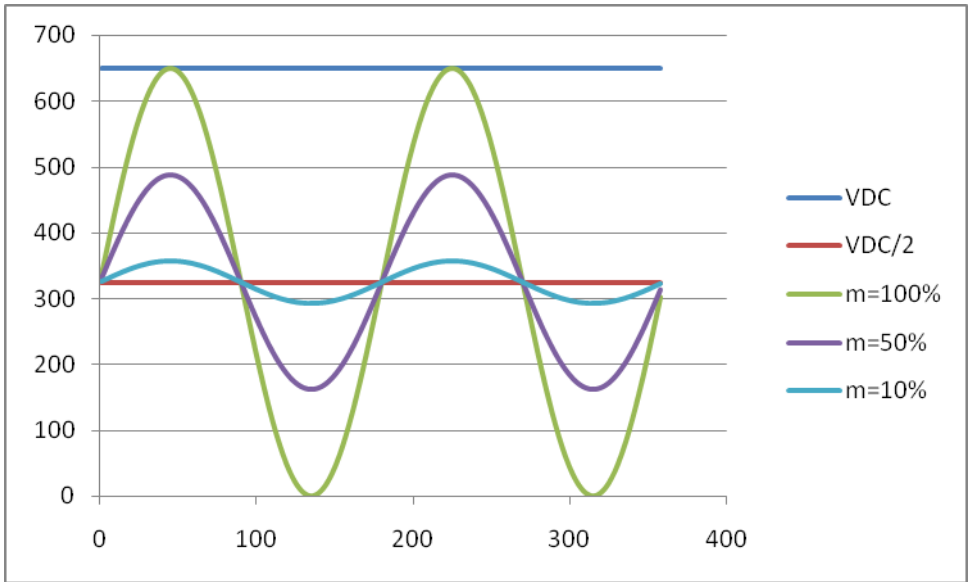
symbol	parameter name	Test Conditions	Minimum	Typical	Maximum	Units
Vcc	power supply	-	3.5	5	5.5	V
VREF	Reference power supply input	-	-	5	- V	
I / O	All input and output	All I / O pin GND of the voltage	0	-	5	V
Icc	Quiescent Current	Vcc = 5V, OSC = 12MHz	-	10	15	mA
V FB	Feedback reference voltage peak	Vcc = 5V	-	3.0	- V	
I FB	Current protection reference voltage	Vcc = 5V	-	0.5	- V	
T FB	The reference voltage temperature protection	Vcc = 5V	-	4.3	- V	
Vin (H)	A logic input signal high potential	Vcc = 5V	2.0	5.0	5.5	V
Vin (L)	Input logic signal low potential	Vcc = 5V	-0.3 0		1.0	V
Vout (H)	Outputs a logic high signal	Vcc = 5V, IOH = -3mA	3.0	5.0	-	V
Vout (L)	A logic low output signal of	Vcc = 5V, IOL = 10mA	-	-	0.45	V
Isink	The maximum output pins irrigation Electric current	-	-	-	20	mA
Isource	The maximum output of the pull pin Electric current	-	-	-	--3	mA

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8. working principle

EG8030 It has four operating modes: namely, an open loop regulating three-phase synchronous, three-phase synchronous loop regulator, three independent open loop voltage, three-phase Independent closed loop regulation. Four operating modes with different features, on demand by the user to choose. Before the introduction of four operating modes, first introduced a bit EG8030 An important parameter voltage control system - **Modulation depth** .

Modulation depth Is defined as: as the difference between the maximum amplitude and the minimum amplitude modulated wave of the current carrier than the maximum amplitude and the minimu He expressed as a percentage. The inverter, the DC bus at the same load and input conditions, SPWM The modulation depth and the output sine wave Amplitude substantially proportional relationship.



DC bus voltage and the modulation depth, the sine wave output relationship diagram

The chart below compares the performance of the image **DC bus voltage** with **Modulation depth, the sine wave output** The relationship between. Figure VDC It represents the DC bus Voltage, m It represents the modulation depth. Under ideal conditions, i.e., the output impedance of the inverter 0 When, when the modulation depth m = 100% Sine wave peak It is exactly equal to the peak voltage of the DC bus. Thus, we can obtain the relationship between the single-phase sinusoidal voltage and the DC bus voltage:

$$VAC_{TOP} = 2 \quad \frac{1}{} * m * VDC$$

$$VAC_{RMS} = 4 \quad \frac{\sqrt{2}}{} * m * VDC$$

E.g:

1) DC bus voltage VDC = 650V , Modulation depth m = 100% , Calculated current effective value of the AC output voltage:

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$$VAC_{RMS} = \frac{\sqrt{2} * 650 * 100\%}{4} = 230V$$

2) DC bus voltage VDC = 650V , Modulation depth m = 50% , Calculated current effective value of the AC output voltage:

$$VAC_{RMS} = \frac{\sqrt{2} * 650 * 50\%}{4} = 115V$$

in EG8030 We have defined three phases SPWM The modulation depth M_A , M_B , M_C .

8.1 Open loop phase synchronous regulator

Phase synchronous mode is an open loop regulator EG8030 The simplest mode of operation. Chip operates in an open loop mode, the user adjusting VOLADJ Three-phase direct control voltage pin SPWM Modulation depth M_A , M_B , M_C And the three-phase modulation depth $M_A = M_B = M_C$. VOLADJ The feet 0-5V Corresponding to the voltage modulation depth M_A of 0-100% . In order to ensure a complete cycle of the waveform is a sine wave, each phase modulated System depth of only refreshed once a week, that is A Phase phase is 0 When ° for VOLADJ Sampling and conversion M_A , M_B , M_C Value.

Open loop phase synchronous regulator can be used in the case of three-phase AC output voltage of less precision. Simply provide a relatively stable high And a three-phase voltage DC power supply output filter, can be adjusted VOLADJ Feet voltage the output voltage reaches a target value. Simple structure, capacity Easy to implement. Less than that, because the actual power inverter is not an ideal voltage source, always present a certain output impedance when the load is increased, Inverter portion of the voltage loss of internal resistance will cause actual output voltage is reduced. Internal resistance voltage drop about the size of the inverter. In addition, The dc power supply will also affect the three-phase output voltage.

Open loop phase synchronous regulator can also be applied in the case of user-created feedback loop, the user can participate in a single piece by a hardware circuit or software implemented Various control algorithms for closed-loop regulation, at this time EG8030 As an actuator, in accordance with VOLADJ Adjusting sine wave input voltage feet Output. This way of working more open chip applications, providing open space for independent play developers. But note that, EG8030 The output adjustment mechanism **By-week adjustment** That changed once per cycle output, in a cycle, VOLADJ The voltage change feet Not be acknowledged.

8.2 Three-phase synchronous closed loop regulator

Phase synchronous loop mode regulator EG8030 Recommended application mode, applicable to the case where the required accuracy of the output voltage. In this kind of work Mode, sampling chip AVFB , BVFB , CVFB Feet and averaged to give a feedback signal a current feedback average three-phase voltage, and then Through internal PI Three-phase regulator operation to give SPWM Modulation depth M_A , M_B , M_C And $M_A = M_B = M_C$ Synchronous phase output adjustment. VOLADJ Decision feedback control threshold current e.g. VOLADJ Feet voltage 2.5V , Then when the feedback voltage is greater than the average 2.5V Time, EG8030 By internal PI Regulator operation gradually reduced M_A , M_B , M_C Value, thereby reducing the output voltage, while the voltage feedback will be with

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The reduced; conversely, when A Phase feedback voltage is less than 2.5V Time, EG8030 By internal PI Synchronous operation regulator reduced M_A , M_B , M_C Value, thereby reducing the output voltage, the feedback voltage also decreases at the same time; thus, it is possible to stabilize the voltage feedback 2.5V ,The output voltage Nature will remain constant.

In this mode, when the DC bus voltage fluctuations or load size changes, the three-phase output voltage can be kept substantially constant. Suitable for transfusion Voltage and the load is not high precision or load balancing difference occasions. When any one phase voltage is greater than the set voltage 110% Or less than the set electric Pressure 90% Time, EG8030 The execution phase unbalance protection off operation.

Phase synchronous loop regulator feedback necessary to sample the high voltage output, it is generally recommended to use a three-phase frequency step-up transformer, and the output It requires the use of three phase voltages with a small feedback transformer isolated buck feedback. Ensure the output AC output DC isolation, and the control circuit AC output isolation. Three-phase frequency step-up transformer recommended Δ- Y Connection, can be four-wire output, and a DC voltage can be improved Utilization. Three-phase high voltage terminal requires frequency transformer and a center line of a small CBB Filter capacitor, to obtain a smooth three phase sine wave.

8.3 Three-phase independent open-loop regulator

Three-phase independent open loop regulating mode EG8030 Further an open loop mode of operation. By adjusting the user AVFB , BVFB , CVFB foot Independent control of the three-phase voltage on SPWM Modulation depth M_A , M_B , M_C . Correspondence is 0-5V correspond 0-100% ,among them AVFB control system M_A , BVFB control M_B , CVFB control M_C . In this mode, VOLADJ Foot function is shielded. In order to ensure a cycle Waveform is a sine wave, the modulation depth of the respective phases is only refreshed once a week, i.e. in the phase of the phase of 0 When the feedback to be taken ° Kind, and conversion M_A , M_B , M_C Value.

Three-phase independent open-loop regulator can be applied to three-phase AC output voltage accuracy is not required, but the three-phase output voltage values different occasions. Simply provide a relatively stable high voltage DC power and a three phase output filter, can be adjusted independently by AVFB , BVFB , CVFB Feet voltage of each phase of the output voltage reaches a different target. Simple structure, easy to implement. Less than that, since no actual power inverter Is an ideal voltage source, always present a certain output impedance when the load is increased, the internal resistance of the inverter portion of the voltage loss will be, resulting in a solid Actual output voltage is decreased. Internal resistance voltage drop about the size of the inverter. Further, fluctuation of the DC power source will also affect the three-phase output voltage.

Three-phase independent open-loop voltage regulator can also be applied in the case of user-created feedback loop, the user can participate in a single piece by a hardware circuit or software impl Various control algorithms for closed-loop regulation, at this time EG8030 As an actuator, in accordance with VOLADJ Adjusting sine wave input voltage feet Output. This way of working more open chip applications based on open-loop synchronous mode regulator on providing an open space from developers The main play space. But note that, EG8030 The output adjustment mechanism **By-week adjustment** That changed once per cycle output, in a cycle in, AVFB , BVFB , CVFB Voltage change will not be acknowledged feet

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8.4 Independent closed loop three-phase voltage regulator

Three-phase independent mode is a closed loop regulator EG8030 A test mode, the output voltage is applied to the field of high-precision, three-phase unbalanced load with Co. This high DC voltage pattern, a complex structure, high reliable as several other modes, it is defined as a test mode, the user may wish to Shen choose to use this mode of operation.

In this mode of operation, the chip sample AVFB , BVFB , CVFB Feet feedback signals, via respective independent of PI Regulator operation, Modulation depth of the respective tanks to give M_A , M_B , M_C . VOLADJ Still decide to feedback control threshold, such as the current VOLADJ Feet voltage for 2.5V Then when A Phase feedback voltage is greater than 2.5V Time, EG8030 By internal PI Reducing regulator operation M_A Value, thereby reducing the output Voltage, while the feedback voltage also decreases; the other hand, when the A Phase feedback voltage is less than 2.5V Time, EG8030 By internal PI Regulator Reduced operation M_A Value, thereby reducing the output voltage, the feedback voltage also decreases at the same time; thus, it is possible to stabilize the voltage feedback 2.5V , Naturally the output voltage is maintained constant. The other two phases also empathy achieve independent regulator.

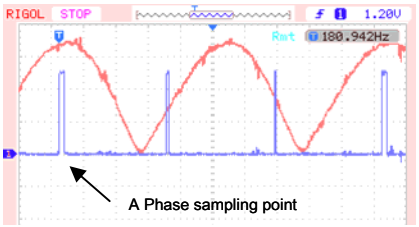
In this mode, when the DC bus voltage fluctuations or load size changes, the three-phase output voltage can be kept substantially constant. Suitable for transfusion Voltage high precision, with the case of three-phase unbalanced loads. This mode requires the use of large capacitors in series two arms composed of the fourth bridge to achieve a three-phase Four output lines, and each can be independently regulated. For further support this mode, will gradually improve.

9. Application Design

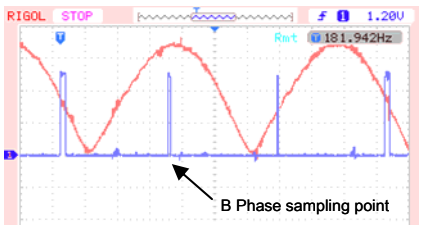
9.1 Voltage feedback

EG8030 Voltage of the chip using the feedback sampling **By-week sampling** , The phase of the sample point determined by the current mode of operation, three-phase independent feedback oper At each sampling point with the formula for the sine-phase peak position, i.e., the phases were 90 Feedback voltage sampled ° phase. Three-phase synchronous operation mode Sampling Point phase was 60 °. chip SPO Sampling the signal output from the signal pin, i.e., SPO Is at high level, the voltage feedback sampling chip.

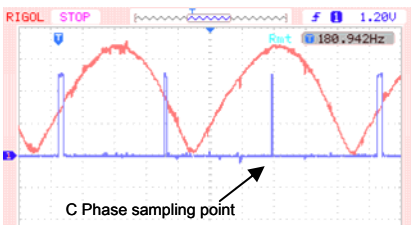
In order to distinguish A , B , C Samples of the three-phase feedback, FIG wide level is A Phase voltage feedback samples, followed later B Phase sampling point C Phase sampling points. When the phase reversal is provided (PHDIR = ' 0 '), The width of the rear power level were C Phase sampling point and B Phase sampling points.



SPO versus VFBA Waveform



SPO versus VFBB Waveform

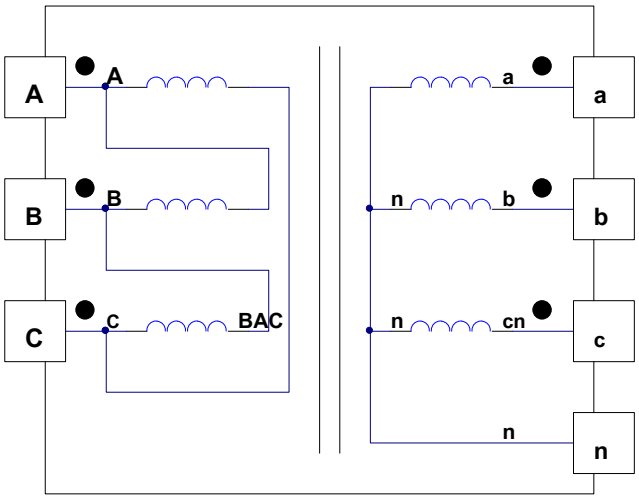


SPO versus VFBC wave

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FIG waveform from the three-phase synchronous loop mode using the power frequency regulator transformer Δ- Y When the feedback waveform type connection. See circuit diagram 6.1 Section, three-phase synchronous loop regulator Typical Application Schematic. AVFB A phase of the sampling points 30 °, since the use frequency transformers Δ- Y Type connection, the input stage AC Dot end corresponding to the output stage an , BA Corresponding to dot end bn , CB Corresponding to dot end cn . A Phase to phase 0 °, C Phase to phase - 120 °, the line voltage AC The phase is - 60 °, the output stage an Phase also - 60 °. Therefore, the phase of 30 ° position just sampled an Peak.

BVFB , CVFB The waveform in turn goes back 120 °. If a phase reversal (PHDIR = ' 0 '), Then BVFB , CVFB The sampling point will be exchanged.



Three-phase frequency transformer Δ- Y Type connection

9.2 Current feedback

EG8030 Chip pins I_{FB} Is a measure of the inverter output load current, mainly for overcurrent detection, the circuit configuration of FIG current 8.1a Sampling a feedback portion of the interior of the peak voltage of the reference pin as 0.5V Overcurrent detection delay time 600mS When the electric load for any reason High flow exceeds the load current of the inverter, EG8030 According pin TYPH , TYPL Setting the output state xHO , xLO To " 0 "or " 1 "Level, turn off all power MOSFET The output voltage to a low level, the main function is to protect the power MOSFET And the load once After entering the over-current protection, EG8030 will be 16S After releasing the power to reopen MOSFET Analyzing loading tube and then an overcurrent condition, the power release opening MOS Duration tube is 100mS, Release 100mS Time and then determine an overcurrent event, if there are still over-current events, EG8030 Then Turn off all power MOSFET The output voltage to a low level, again waiting 16S The release, if certain occasions, such as start-up current is relatively large time Long, not suitable for the application of this feature, you can I_{FB} Pin to ground.

9.3 Temperature Feedback

EG8030 Chip pins T_{FB} Is a measure of the operating temperature of the inverter, it is mainly used for detecting over-temperature protection and control output of the fan, the circuit configuration FIG 8.3a temperature detection circuit, and the NTC thermistor RT1 shown in FIG measuring resistor RF1 form a simple voltage divider circuit, with the divided voltage value The change of temperature change value, the magnitude of the voltage will reflect the size of the NTC resistor to give the corresponding temperature value. Selection NTC 25 ℃

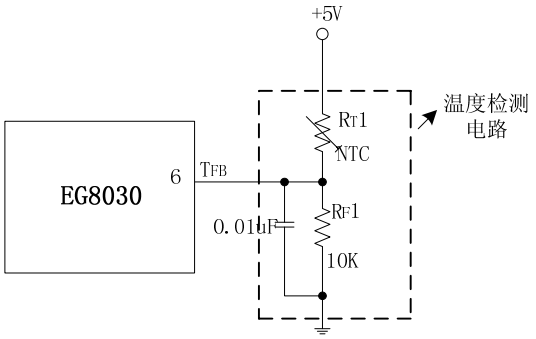
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10K corresponds to the resistance of the thermistor, T_{FB} Pin voltage is set overtemperature 4.3V When the over-temperature protection occurs, EG8030 According pin TYPH ,

TYPL Setting the output state PWMXH , PWMXL To " 0 "or" 1 "Level, turn off all power MOSFET To the output voltage

A low level, once the over-temperature protection after entering, EG8030 The re-determination temperature, if T_{FB} Pin voltage is below 4.0V , EG8030 will

Quit over-temperature protection, the inverter to work. If you do not use over-temperature protection, the pin needs to be grounded.



Map 8.4a EG8030 Temperature detection circuit

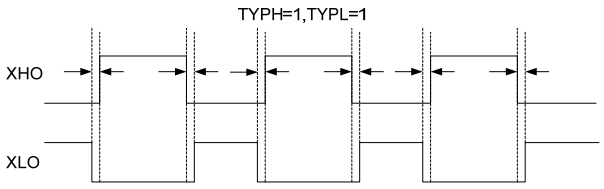
9.4 PWM output type

EG8030 Chip pins TYPH , TYPL Can be set independently PWM Output vertical tube type, to apply to all drives. TYPH , TYPL

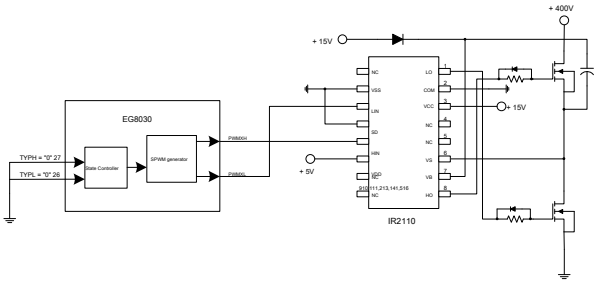
for" 00 ", The output of PWM Type Output deadband applied simultaneously low level applications (such as drive IR2110 or IR2106 And other drive core

Sheet), FIG. 8.4a Yes EG8010 Pin SPWMOUT Output waveform, active high driving power MOS Tube, FIG. 8.4b Yes TYPH ,

TYPL for" 11 "When the driver IR2110 The application circuit.



Map 8.4a THPH = 1, TYPL = 1 When PWM Waveform output

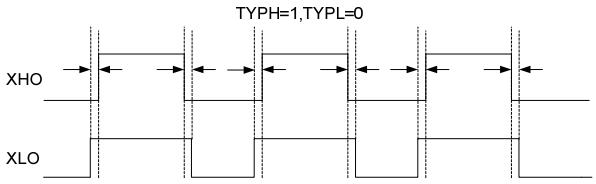


Map 8.4b EG8030 drive IR2110

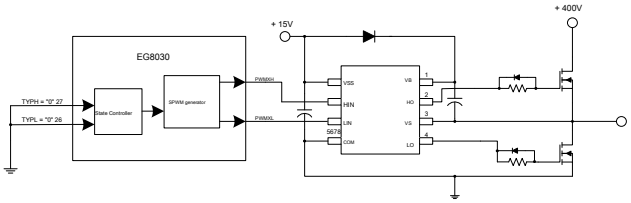
TYPH , TYPL for" 10 ", The output of PWM The type of high output is applied to open the tube, the tube opening is low flooding

Movable circuit (driving IR2103 Driver chips, etc.), FIG. 8.4c Yes EG8030 Pin xHO , xLO The output waveform.

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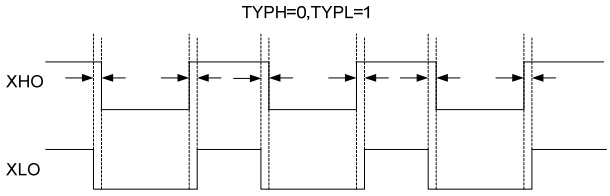
Map 8.4c THPH = 0, TYPL = 1 When PWM Waveform output



Map 8.4d EG8030 drive IR2103

TYPH , TYPL for" 01 ", The output of PWM Output is applied to the tube type opening is low, the drive tube is high open

Movable circuit (such a driving method is not used), FIG. 8.4e Yes EG8030 Pin xHO , xLO The output waveform.



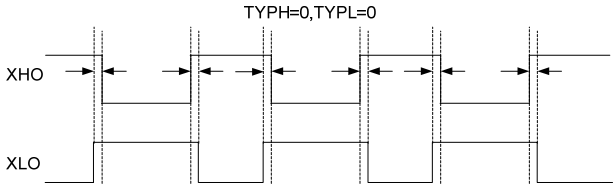
Map 8.4e THPH = 1, TYPL = 0 When PWM Waveform output

TYPH , TYPL for" 11 ", The output of PWM Output type used in pipe, the low driving circuit transistor are open (e.g.

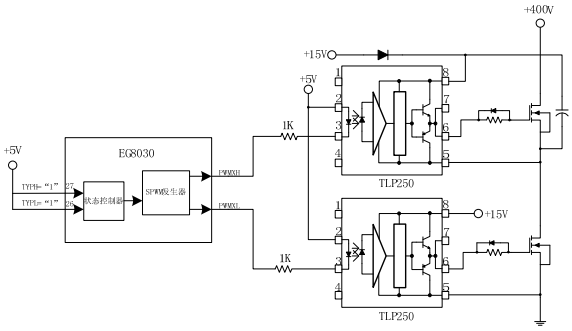
drive TLP250 The cathode of the optocoupler and the like), FIG. 8.4f Yes EG8030 Pin xHO , xLO The output waveform. , Optocoupler driven active low,

High drive power output optocoupler MOS Tube, FIG. 8.4g Yes TYPH , TYPL for" 11 "Time, EG8030 drive TL250 Optocoupler

Application circuit.



Map 8.4f THPH = 0, TYPL = 0 When PWM Waveform output



Map 8.4g EG8030 drive TLP250

9.5 Dead time

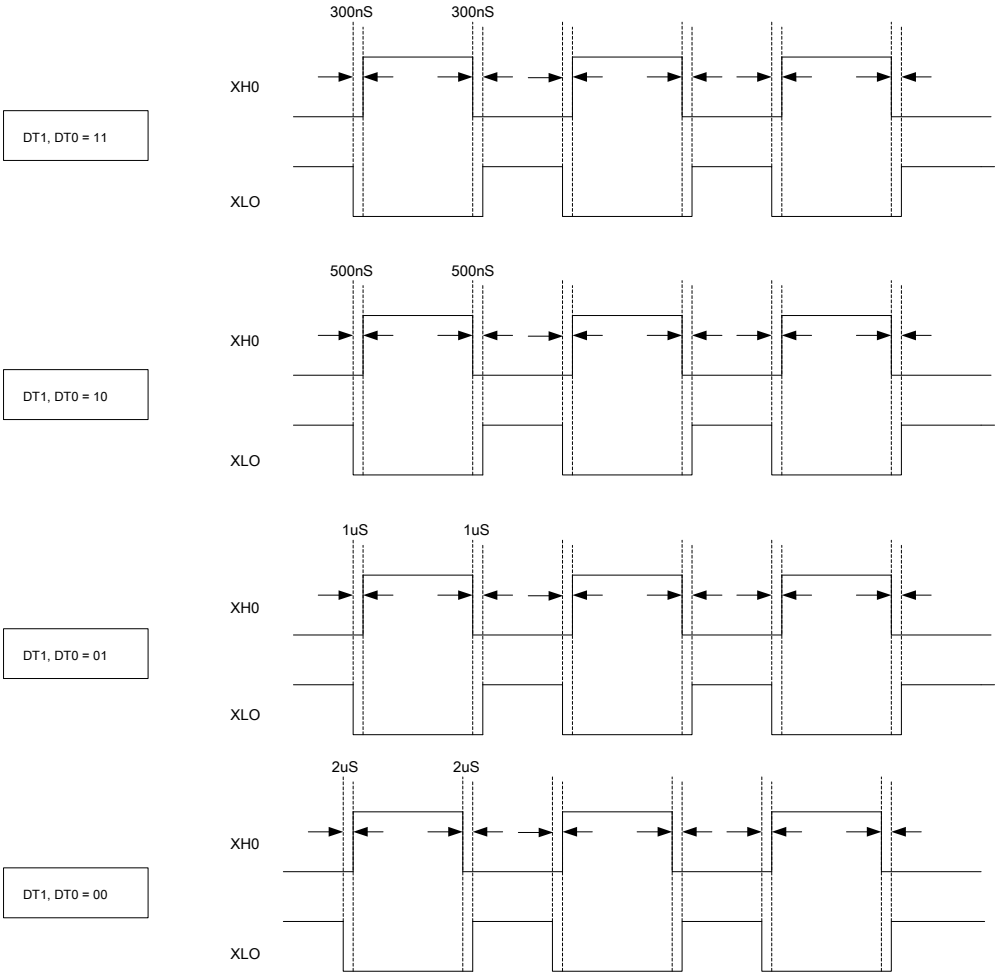
EG8010 Chip pin DT1, DT0 is to control the dead time, dead time control is one of the important parameters of power MOS transistors, if not dead

Time or too small can result in up and down while power MOS MOS transistor is turned on and burned the phenomenon, if the dead too large lead to waveform distortion and power tube hair

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Severe thermal phenomenon, FIG. 8.5a is a dead EG8010 internal control sequence, as shown in FIG pin DT1, DT0 of four kinds to set dead time, "00" is

300nS dead time, "01" is 500nS dead time, "10" is 1uS dead time, "11" is 1.5us dead time.



Map 8.5a EG8010 Deadband control settings

9.6 Frequency setting

EG8030 You can configure two output sine wave frequency by FS0 Pin settings. when FS0 When the pin is left floating or connected to high, EG8030

Will produce 50HZ Sine wave, FS0 Then low pin, EG8030 Will produce 60HZ Sine wave.

Other EG8030 You can also configure four SPWM Modulation frequency, the pin MS1 , MS0 set up.

MS1 , MS0 = 11 : Modulation frequency 20KHz MS1 , MS0 =

10 : Modulation frequency 10KHz MS1 , MS0 = 01 :

Modulation frequency 5KHz MS1 , MS0 = 00 : Modulation

frequency 2.5KHz

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9.7 Soft Start

EG8030 It provides soft-start mode for instant high starting current load. SST Pin through pull-up resistor configured to " 1 "Time,

Enabling this feature. Continued soft start 3S , 3S It automatically enters the state regulator. Set as" 0 "When, prohibit soft start function. EG8030 recommend

Enable the soft start function. Such as soft-start function is enabled, when the chip because EN When the protective function turns off the foot or restart, the chip will still be soft

start up.

9.8 Reverse phase sequence

EG8030 It includes a phase sequence reversed function, adjust the direction of phase sequence, this function PHDIR Pin achieve. when PHDIR for" 1 "When B

Phase A leads phase A 120 °, C phase lag phase A 120 °, when "0" B phase lag phase A 120 °, the phase leads A C 120 °. Reverse phase sequence

Can be used for motor control, in order to prevent the motor is suddenly switched to the reverse rotation caused by the positive impact of high current, output should turn off, the motor stops, etc.

After reversing the phase sequence, then enable output.

9.9 Phase cleared

EG8030 It includes a phase correction function, online synchronous phase sequence. PHCLR Raised the level on pin change triggers the function. After clearing A

Forced clear phase sequence, B Phase C Phase will be based on PHDIR State direction to adjust the phase lead, lag 120 °. Users want the two

When the sheet EG8030 simultaneous use, may be connected to a pin on the FOUT pin PHDIR other sheet, in order to achieve synchronization phases two chips.

9.10 Sinusoidal analog signal output

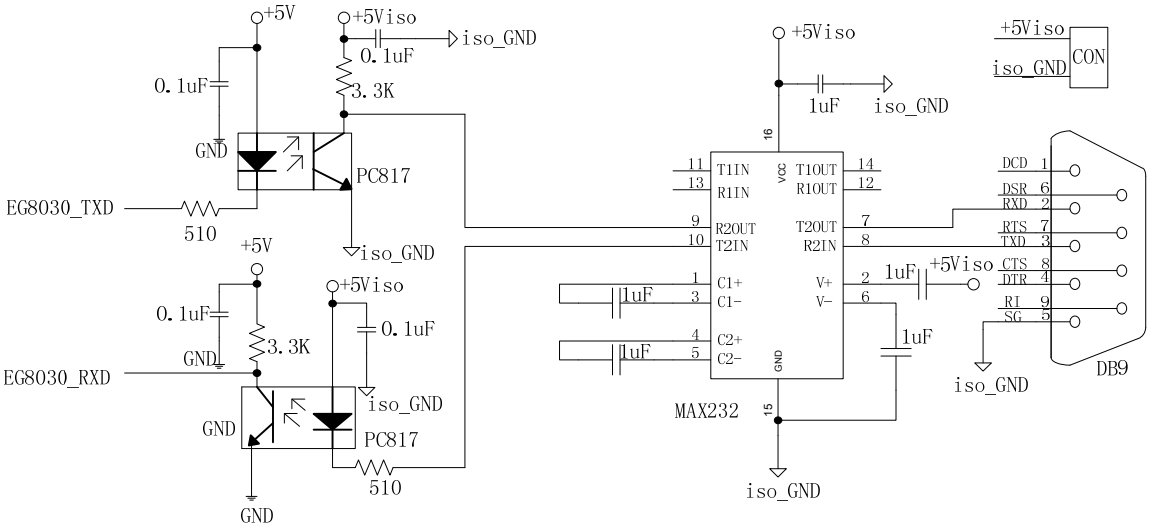
EG8030 Internal integration DA Module, can output A An analog sine wave signals of the same phase.

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10. RS232 Serial Communication Interface

EG8030 Applied RS232 Serial communication interface setting parameters voltage inverter frequency dead zone, opto-isolation communication application requires

Figure 8.9a .



Map 8.9a RS232 Opto-isolation communication circuit

Serial port parameters:

Baud rate: 2400

Data bits: 8

Parity: None

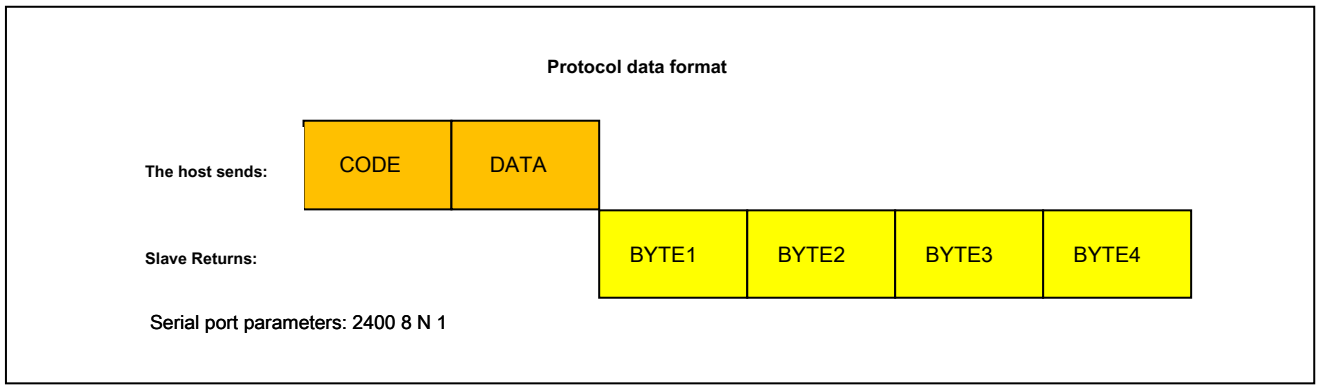
Stop bits: 1

Protocol Description:

Communications, EG8010 as a slave, or the user can use the PC as the host MCU. Upon receiving the command from the host machine sent immediately

Generating a response, response data to the host.

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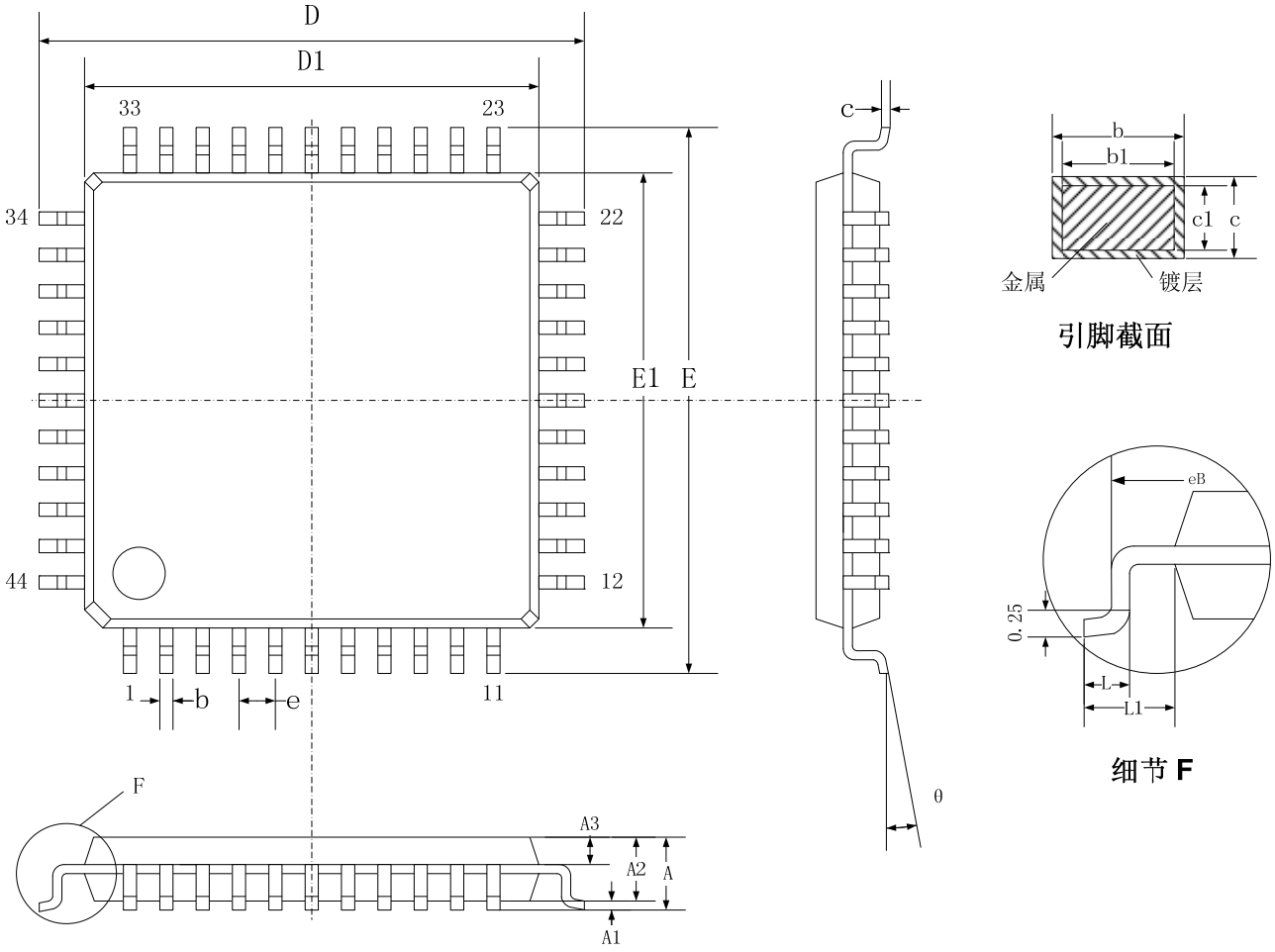
Data format is shown, in one operation, the host sends two bytes of data, the first byte is a command byte, the second byte of data byte. Received from the slave to master word postganglionic, four bytes of data to return immediately.

Format: **(Reserved)**

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11. Package size

LQFP44 Package Size:



symbol	A	A1	A2	A3			b	b1	c	c1	D	D1		E	E1		e	eB	L	L1		θ
MIN	-		0.05	1.35	0.59	0.29	0.28	0.13	0.12	11.80	9.90	11.80	9.90	0.80					11.25	0.45	1.00		0
NOM	-		-	1.40	0.64		-	0.30	-	0.13	12.00	10.00	12.00	10.00				BSC	-	-		BSC	-
MAX	1.60	0.20	1.45	0.69	0.37	0.33	0.18	0.14	12.20	10.10	12.20	10.10							11.45	0.75			7
unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm									o

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